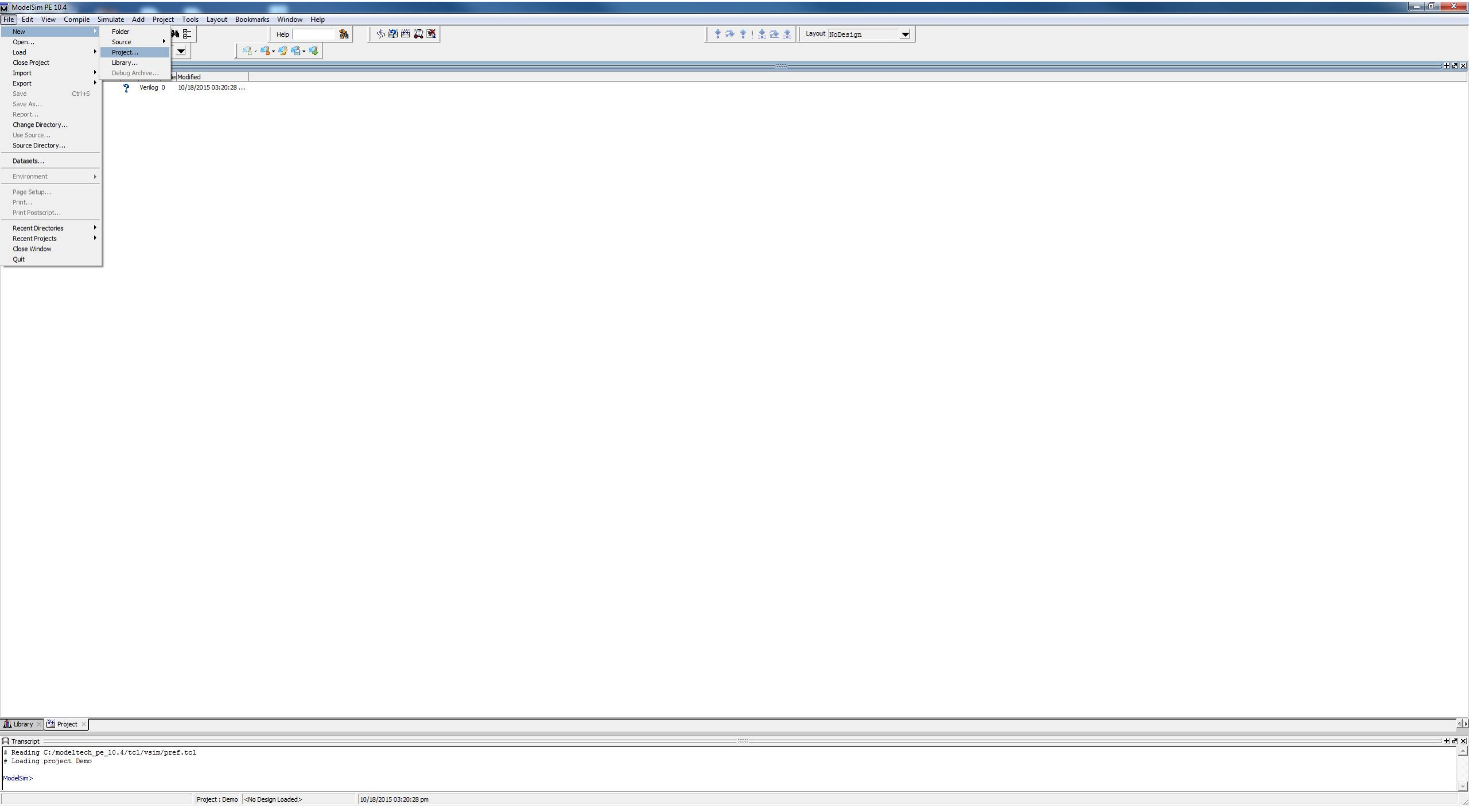
How to use ModelSim

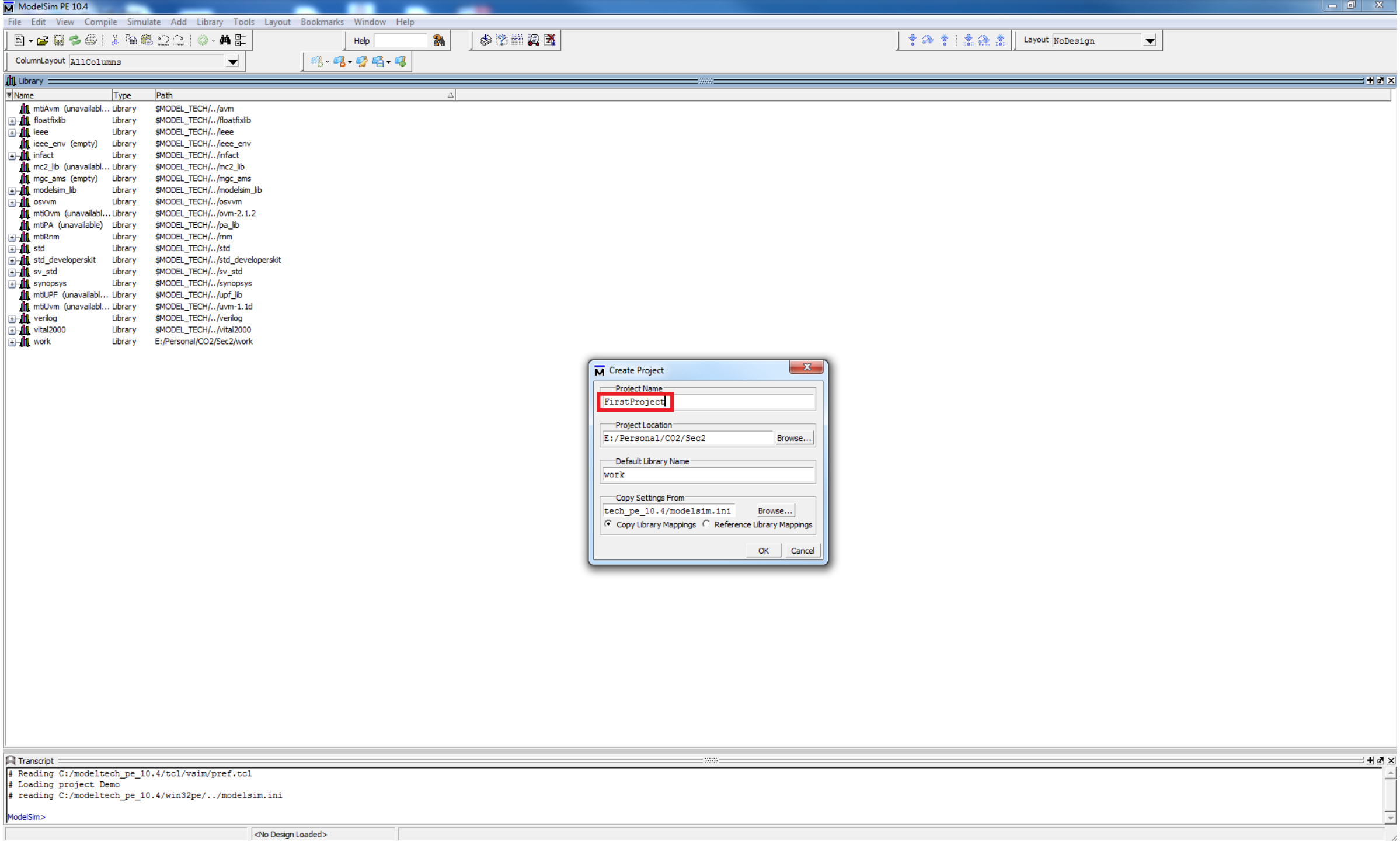
Create a new project:

- File>New>Project


ModelSim PE 10.4
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
New
Open...
Load
Close Project
Import
Export
Save Ctrl+S
Save As...
Report...
Change Directory...
Use Source...
Source Directory...
Datasets...
Environment
Page Setup...
Print...
Print Postscript...
Recent Directories
Recent Projects
Close Window
Quit
Folder
Source
Project...
Library...
Debug Archive...
Help
Layout NoDesign
Modified
Verilog 0 10/18/2015 03:20:28 ...
Library
Project
Transcript
Reading C:/modeltech_pe_10.4/tcl/vsim/pref.tcl
Loading project Demo
ModelSim>
Project : Demo
<No Design Loaded>
10/18/2015 03:20:28 pm

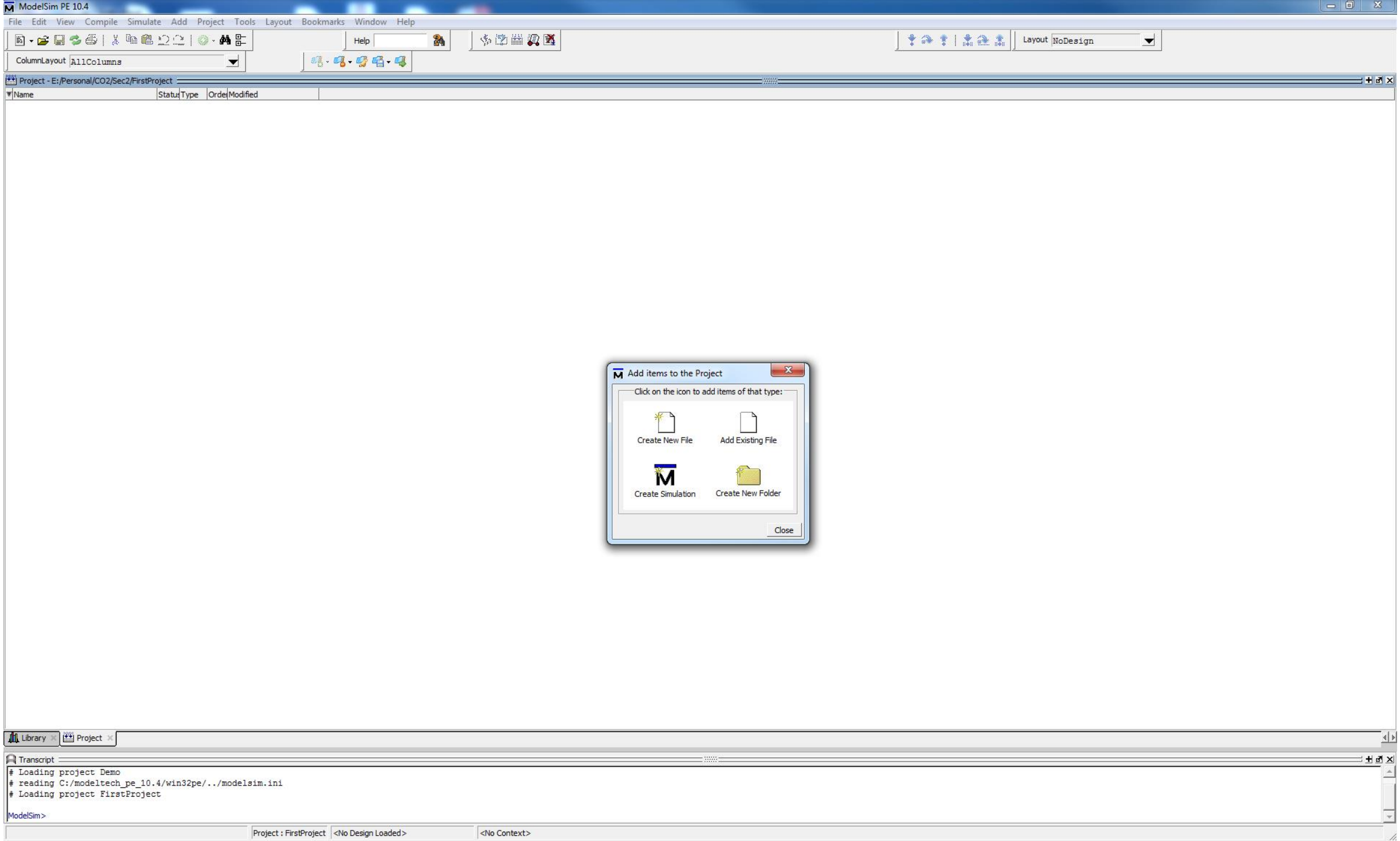
Name the Project:

- Type a name for your project


ModelSim PE 10.4
File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help
Help
Layout NoDesign
ColumnLayout AllColumns
Library
Name Type Path
mtiAvm (unavailabl... Library $MODEL_TECH/../avm
floatfixlib Library $MODEL_TECH/../floatfixlib
ieee Library $MODEL_TECH/../ieee
ieee_env (empty) Library $MODEL_TECH/../ieee_env
infact Library $MODEL_TECH/../infact
mc2_lib (unavailabl... Library $MODEL_TECH/../mc2_lib
mgc_ams (empty) Library $MODEL_TECH/../mgc_ams
modelsim_lib Library $MODEL_TECH/../modelsim_lib
osvvm Library $MODEL_TECH/../osvvm
mtiOvm (unavailabl... Library $MODEL_TECH/../ovm-2.1.2
mtiPA (unavailable) Library $MODEL_TECH/../pa_lib
mtiRnm Library $MODEL_TECH/../rnm
std Library $MODEL_TECH/../std
std_developerskit Library $MODEL_TECH/../std_developerskit
sv_std Library $MODEL_TECH/../sv_std
synopsys Library $MODEL_TECH/../synopsys
mtiUPF (unavailabl... Library $MODEL_TECH/../upf_lib
mtiUvm (unavailabl... Library $MODEL_TECH/../uvm-1.1d
verilog Library $MODEL_TECH/../verilog
vital2000 Library $MODEL_TECH/../vital2000
work Library E:/Personal/CO2/Sec2/work
Create Project
Project Name
FirstProject
Project Location
E:/Personal/CO2/Sec2
Browse...
Default Library Name
work
Copy Settings From
tech_pe_10.4/modelsim.ini
Browse...
Copy Library Mappings
Reference Library Mappings
OK
Cancel
Transcript
Reading C:/modeltech_pe_10.4/tcl/vsim/pref.tcl
Loading project Demo
reading C:/modeltech_pe_10.4/win32pe/../modelsim.ini
ModelSim>
<No Design Loaded>

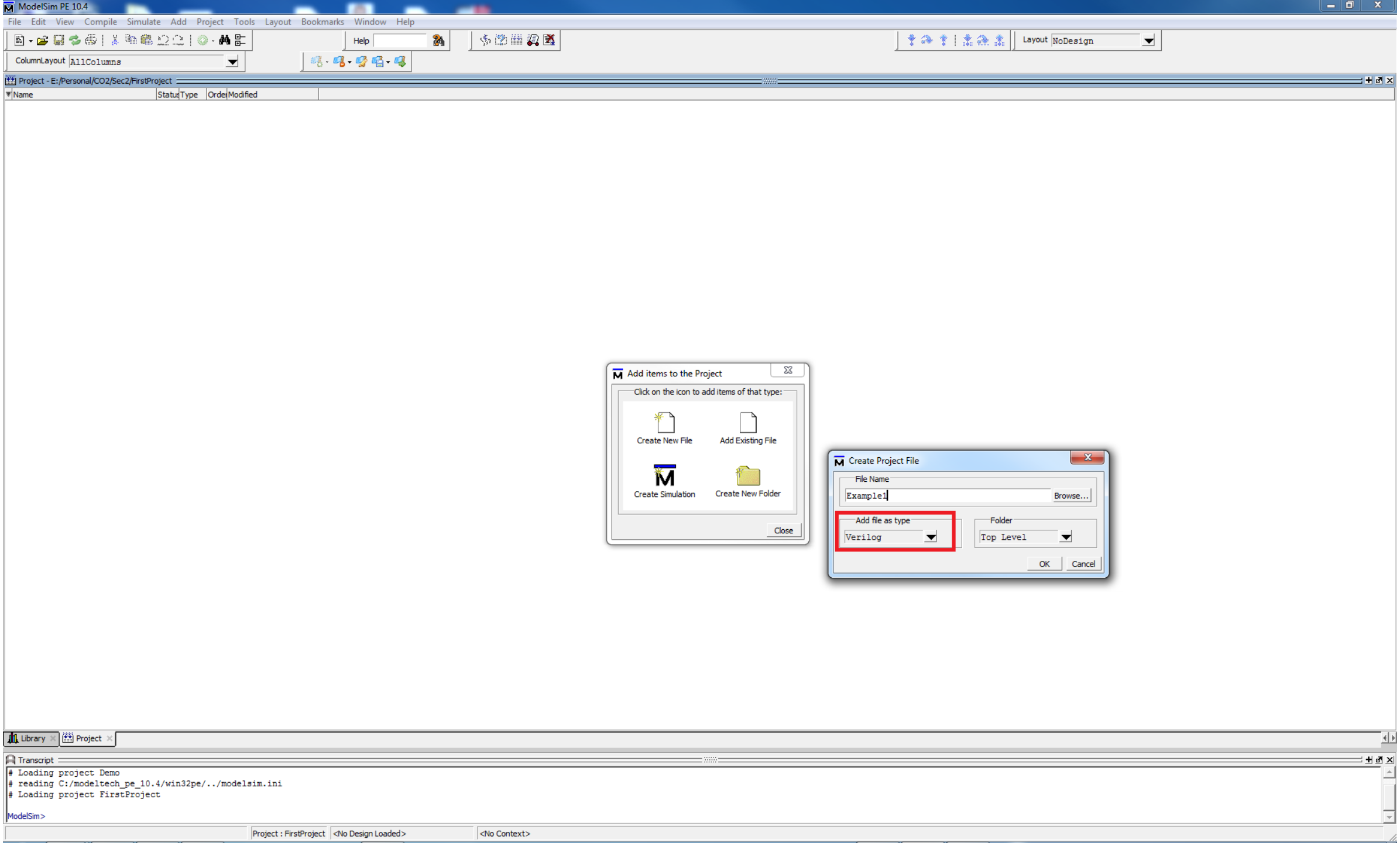
Add Files to the project:

- Click on “Create New File”


ModelSim PE 10.4
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Help
Layout NoDesign
ColumnLayout AllColumns
Project - E:/Personal/CO2/Sec2/FirstProject
Name Status Type Orde Modified
Add items to the Project
Click on the icon to add items of that type:
Create New File
Add Existing File
Create Simulation
Create New Folder
Close
Library
Project
Transcript
Loading project Demo
reading C:/modeltech_pe_10.4/win32pe/../modelsim.ini
Loading project FirstProject
ModelSim>
Project : FirstProject
<No Design Loaded>
<No Context>

Name the file and choose the HDL:

- Make sure to choose Verilog
- Type a name for the new file


ModelSim PE 10.4
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Help
Layout NoDesign
ColumnLayout AllColumns
Project - E:/Personal/CO2/Sec2/FirstProject
Name Status Type Order Modified
Add items to the Project
Click on the icon to add items of that type:
Create New File
Add Existing File
Create Simulation
Create New Folder
Close
Create Project File
File Name
Example1
Browse...
Add file as type
Verilog
Folder
Top Level
OK
Cancel
Library
Project
Transcript
Loading project Demo
reading C:/modeltech_pe_10.4/win32pe/../modelsim.ini
Loading project FirstProject
ModelSim>
Project : FirstProject
<No Design Loaded>
<No Context>

Write your Verilog description:

- Double click on the file name on the left
- You can write your description in the area on the right

ModelSim PE 10.4

File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help

Project - E:/Personal/CO2/Sec2/FirstProject

Name	Status	Type	Order	Modified
Example1.v	?	Verilog	0	10/25/2015 07:07:22 ...

Library Project

E:/Personal/CO2/Sec2/Example1.v - Default

```
1  module circuit (F,A,B,C);
2  input A,B,C;
3  output F;
4
5  not(w1,B);
6  and(w2,w1,A);
7  or(F,C,w2);
8
9  endmodule
10
```

Transcript

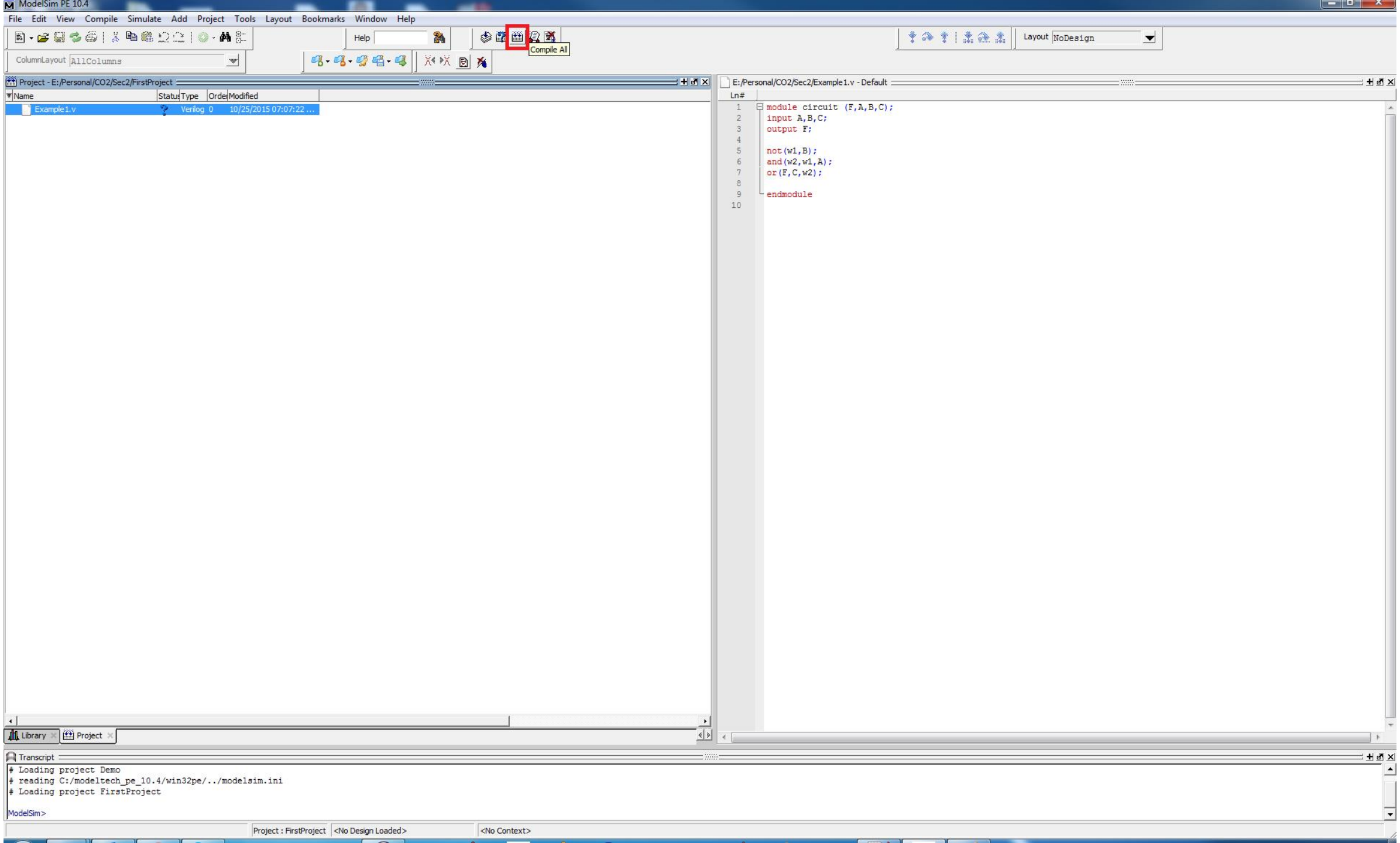
```
# Loading project Demo
# reading C:/modeltech_pe_10.4/win32pe/../modelsim.ini
# Loading project FirstProject

ModelSim>
```

Ln: 7 Col: 11 | Project : FirstProject | <No Design Loaded> | <No Context>

Compile your Verilog description:

- Click on the “Compile all” icon from the toolbar on the top.


ModelSim PE 10.4
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Help
Compile All
Layout NoDesign
ColumnLayout AllColumns
Project - E:/Personal/CO2/Sec2/FirstProject
Name Status Type Order Modified
Example1.v Verilog 0 10/25/2015 07:07:22 ...
E:/Personal/CO2/Sec2/Example1.v - Default
Ln#
1 module circuit (F,A,B,C);
2 input A,B,C;
3 output F;
4
5 not(w1,B);
6 and(w2,w1,A);
7 or(F,C,w2);
8
9 endmodule
10
Library
Project
Transcript
Loading project Demo
reading C:/modeltech_pe_10.4/win32pe/../modelsim.ini
Loading project FirstProject
ModelSim>
Project : FirstProject
<No Design Loaded>
<No Context>

Simulating your Verilog description:

- Click on Simulate>Start Simulation.

ModelSim PE 10.4

File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help

Start Simulation...
Runtime Options...
Run
Step
Restart...
Break
End Simulation

Help

Layout NoDesign

ColumnLayout AllColumns

Project - E:/Personal/CO2/Se

Name | Modified

Example1.v | 10/25/2015 07:07:22 ...

E:/Personal/CO2/Sec2/Example1.v - Default

Ln#

```
1  module circuit (F,A,B,C);
2  input A,B,C;
3  output F;
4
5  not(w1,B);
6  and(w2,w1,A);
7  or(F,C,w2);
8
9  endmodule
10
```

Library Project

Transcript

```
# reading C:/modeltech_pe_10.4/win32pe/../modelsim.ini
# Loading project FirstProject
# Compile of Example1.v was successful.

ModelSim>
```

Project : FirstProject | <No Design Loaded> | <No Context>

Choose the component to be simulated:

- Choose your module to be simulated.
- Press Ok

ModelSim PE 10.4

File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help

Project - E:/Personal/CO2/Sec2/FirstProject

Name	Status	Type	Order	Modified
Example1.v	✓	Verilog	0	10/25/2015 07:16:43 ...

E:/Personal/CO2/Sec2/Example1.v - Default

```
1  module circuit (F,A,B,C);
2  input A,B,C;
3  output F;
4
5  not(w1,B);
6  and(w2,w1,A);
7  or(F,C,w2);
8
9  endmodule
10
11 module Circuit_Tb;
12
13 reg A,B,C;
14 wire F;
15
16 circuit C1 (F,A,B,C);
17
18 initial
19 begin
20 $monitor($time,"%b, %b, %b, %b",A,B,C,F);
21 #2 A=1;B=0;C=0;
22 #2 B=1;
23 #2 A=0;
24 #2 C=1;
25 end
26
27 endmodule
28
```

Start Simulation

Design | VHDL | Verilog | Libraries | SDF | Others

Name	Type	Path
std	Library	$MODEL_TECH/../std
std_developerskit	Library	$MODEL_TECH/../std_developerskit
sv_std	Library	$MODEL_TECH/../sv_std
synopsys	Library	$MODEL_TECH/../synopsys
mtiUPF (unavailabl...	Library	$MODEL_TECH/../upf_lib
mtiUvm (unavailabl...	Library	$MODEL_TECH/../uvm-1.1d
verilog	Library	$MODEL_TECH/../verilog
vital2000	Library	$MODEL_TECH/../vital2000
work	Library	E:/Personal/CO2/Sec2/work
TB	Module	E:/Personal/CO2/Sec2/Demo.v
Circuit_Tb	Module	E:/Personal/CO2/Sec2/Example1.v
circuit	Module	E:/Personal/CO2/Sec2/Example1.v

Design Unit(s): work.Circuit_Tb

Resolution: default

OK Cancel

Library | Project

Transcript

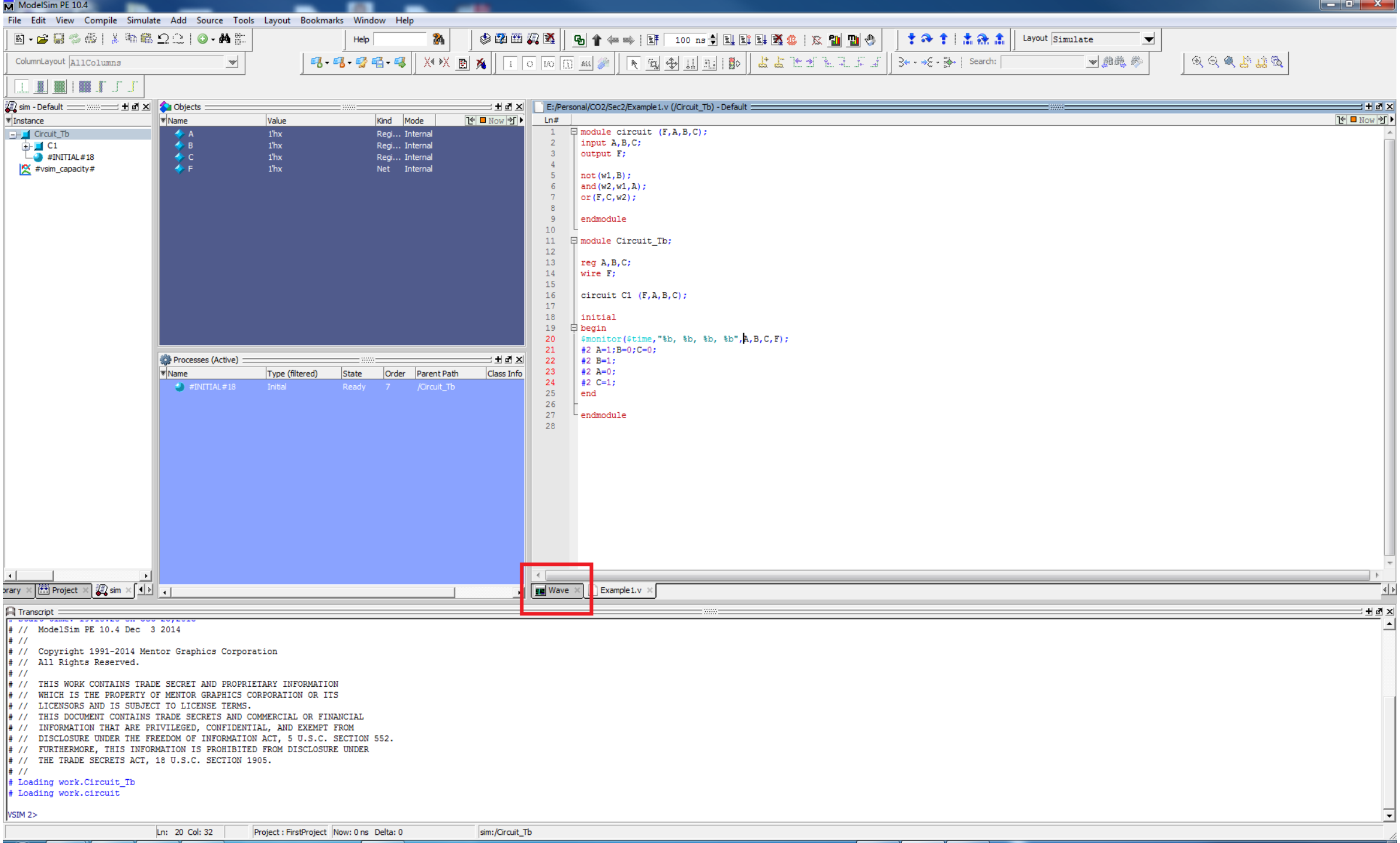
```
# Load canceled
# Compile of Example1.v failed with 1 errors.
# Compile of Example1.v was successful.

ModelSim>
```

Ln: 20 Col: 32 | Project : FirstProject | <No Design Loaded> | $MODEL_TECH/../rnm

View Signal values with time:

- Click on the Wave Tab.


ModelSim PE 10.4
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
sim - Default
Instance
Circuit_Tb
C1
#INITIAL#18
#vsim_capacity#
Objects
Name Value Kind Mode
A 1'hx Regi... Internal
B 1'hx Regi... Internal
C 1'hx Regi... Internal
F 1'hx Net Internal
Processes (Active)
Name Type (filtered) State Order Parent Path Class Info
#INITIAL#18 Initial Ready 7 /Circuit_Tb
E:/Personal/CO2/Sec2/Example1.v (/Circuit_Tb) - Default
1 module circuit (F,A,B,C);
2 input A,B,C;
3 output F;
4
5 not(w1,B);
6 and(w2,w1,A);
7 or(F,C,w2);
8
9 endmodule
10
11 module Circuit_Tb;
12
13 reg A,B,C;
14 wire F;
15
16 circuit C1 (F,A,B,C);
17
18 initial
19 begin
20 $monitor($time,"%b, %b, %b, %b",A,B,C,F);
21 #2 A=1;B=0;C=0;
22 #2 B=1;
23 #2 A=0;
24 #2 C=1;
25 end
26
27 endmodule
28
Wave
Example1.v
Transcript
// ModelSim PE 10.4 Dec 3 2014
//
// Copyright 1991-2014 Mentor Graphics Corporation
// All Rights Reserved.
//
// THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
// WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS
// LICENSORS AND IS SUBJECT TO LICENSE TERMS.
// THIS DOCUMENT CONTAINS TRADE SECRETS AND COMMERCIAL OR FINANCIAL
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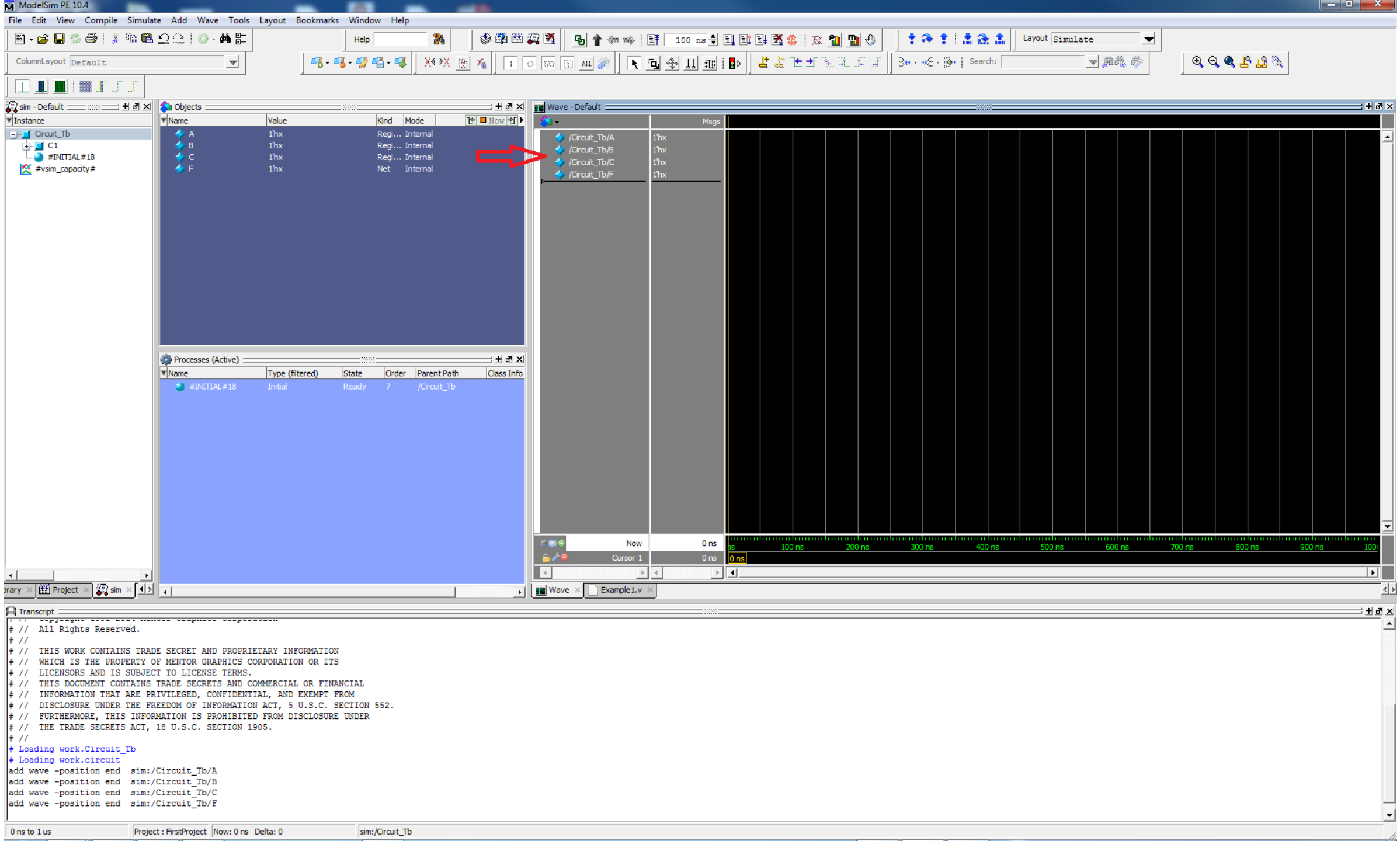
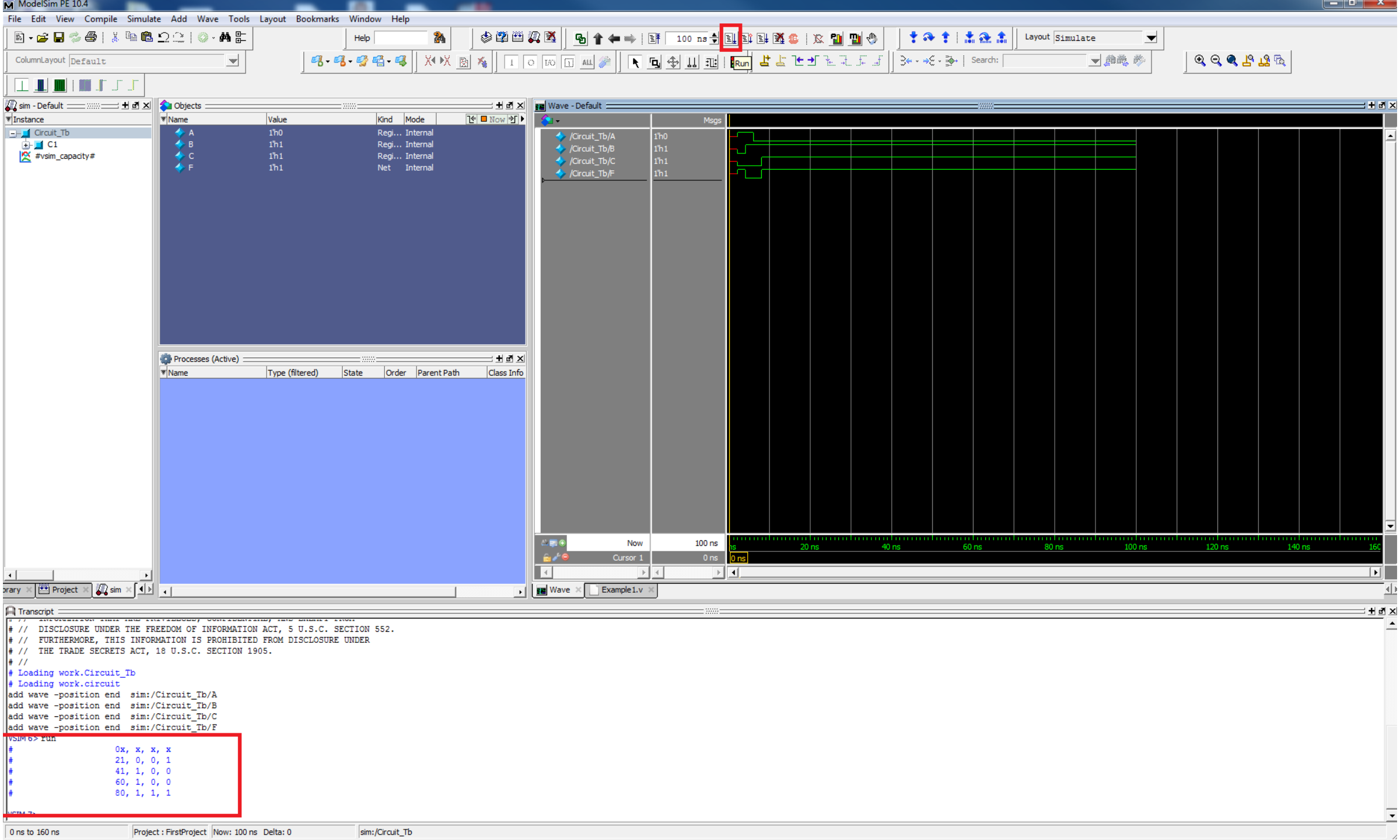
// DISCLOSURE UNDER THE FREEDOM OF INFORMATION ACT, 5 U.S.C. SECTION 552.
// FURTHERMORE, THIS INFORMATION IS PROHIBITED FROM DISCLOSURE UNDER
// THE TRADE SECRETS ACT, 18 U.S.C. SECTION 1905.
//
Loading work.Circuit_Tb
Loading work.circuit
VSIM 2>
Ln: 20 Col: 32
Project : FirstProject
Now: 0 ns Delta: 0
sim:/Circuit_Tb

Drag and drop the Signal to be viewed.


ModelSim PE 10.4
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance
Circuit_Tb
C1
#INITIAL#18
#vsim_capacity#
Objects
Name Value Kind Mode
A 1'hx Regi... Internal
B 1'hx Regi... Internal
C 1'hx Regi... Internal
F 1'hx Net Internal
Processes (Active)
Name Type (filtered) State Order Parent Path Class Info
#INITIAL#18 Initial Ready 7 /Circuit_Tb
Wave - Default
Msgs
/Circuit_Tb/A 1'hx
/Circuit_Tb/B 1'hx
/Circuit_Tb/C 1'hx
/Circuit_Tb/F 1'hx
Now 0 ns
Cursor 1 0 ns
100 ns 200 ns 300 ns 400 ns 500 ns 600 ns 700 ns 800 ns 900 ns
Project
sim
Wave
Example1.v
Transcript
// All Rights Reserved.
//
// THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
// WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS
// LICENSORS AND IS SUBJECT TO LICENSE TERMS.
// THIS DOCUMENT CONTAINS TRADE SECRETS AND COMMERCIAL OR FINANCIAL
// INFORMATION THAT ARE PRIVILEGED, CONFIDENTIAL, AND EXEMPT FROM
// DISCLOSURE UNDER THE FREEDOM OF INFORMATION ACT, 5 U.S.C. SECTION 552.
// FURTHERMORE, THIS INFORMATION IS PROHIBITED FROM DISCLOSURE UNDER
// THE TRADE SECRETS ACT, 18 U.S.C. SECTION 1905.
//
Loading work.Circuit_Tb
Loading work.circuit
add wave -position end sim:/Circuit_Tb/A
add wave -position end sim:/Circuit_Tb/B
add wave -position end sim:/Circuit_Tb/C
add wave -position end sim:/Circuit_Tb/F
0 ns to 1 us
Project : FirstProject
Now: 0 ns Delta: 0
sim:/Circuit_Tb

- Press “Run” from the Toolbar at the top
- The Signal are shown on the Wave window
- The Log is shown below


ModelSim PE 10.4
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance
Circuit_Tb
C1
#vsim_capacity#
Objects
Name Value Kind Mode
A 1'h0 Regi... Internal
B 1'h1 Regi... Internal
C 1'h1 Regi... Internal
F 1'h1 Net Internal
Processes (Active)
Name Type (filtered) State Order Parent Path Class Info
Wave - Default
Msgs
/Circuit_Tb/A 1'h0
/Circuit_Tb/B 1'h1
/Circuit_Tb/C 1'h1
/Circuit_Tb/F 1'h1
Now 100 ns
Cursor 1 0 ns
20 ns 40 ns 60 ns 80 ns 100 ns 120 ns 140 ns
0 ns
Wave
Example1.v
Transcript
// DISCLOSURE UNDER THE FREEDOM OF INFORMATION ACT, 5 U.S.C. SECTION 552.
// FURTHERMORE, THIS INFORMATION IS PROHIBITED FROM DISCLOSURE UNDER
// THE TRADE SECRETS ACT, 18 U.S.C. SECTION 1905.
//
Loading work.Circuit_Tb
Loading work.circuit
add wave -position end sim:/Circuit_Tb/A
add wave -position end sim:/Circuit_Tb/B
add wave -position end sim:/Circuit_Tb/C
add wave -position end sim:/Circuit_Tb/F
VSIM 6> run
0x, x, x, x
21, 0, 0, 1
41, 1, 0, 0
60, 1, 0, 0
80, 1, 1, 1
0 ns to 160 ns
Project : FirstProject
Now: 100 ns Delta: 0
sim:/Circuit_Tb