

Hyeonmin Jeon

HLIM: SHOULD BE DOUBLE-CHECKED SENIOR SEMICONDUCTOR RESEARCHER · INTERCONNECT METALLIZATION SPECIALIST

Seoul, South Korea

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HLIM: Be ambitious and put a catch phrase! Towards Next-Generation Semiconductor Interconnects and Scalable Process Innovation

Summary

HLIM: Poslih the below by yourself! + Convince the other person WHY you want to gain experience in academia after working in industry here. A semiconductor researcher focused on interconnect metallization and advanced process technologies that are essential for next-generation semiconductor scaling. Studying new materials and process innovations to enable reliable interconnect scaling and to improve overall chip performance. An advocate of collaborative research, aiming to accelerate semiconductor technology advancement and contribute to the global microelectronics community. Currently, a researcher at the Samsung Electronics Foundry, Republic of Korea. Previously contributed as a process engineer and R&D specialist in cross-disciplinary teams, leading projects that bridged materials science, process integration, and large-scale manufacturing.

Highlights HLIM: Highlight the expertise you developed at the company.

- Over 6 years of research and development experience in interconnect process technologies at Samsung Electronics Foundry
- Led projects on scaling down interconnect metals through novel materials and advanced fabrication methods
- Improved semiconductor device performance and reliability by optimizing metallization processes
- Collaborated with multidisciplinary teams across materials science, device physics, and process engineering
- Contributed to high-volume manufacturing readiness for advanced process nodes

Field of Interest

MY RESEARCH INTERESTS INCLUDE, BUT ARE NOT CONFINED TO:

- Interconnect metallization and scaling for advanced semiconductor nodes
- Materials engineering for barrier/liner and low-resistivity metals
- Process development for yield and reliability improvement
- Integration of new metallization processes into high-volume manufacturing
- Electrical performance enhancement through optimized interconnect design
- Semiconductor device scaling and manufacturability

Education

KAIST(Korea Advanced Institute of Science and Technology)

Daejeon, S.Korea

M.S. IN MATERIALS SCIENCE AND ENGINEERING

Mar. 2018 - Feb. 2020

- Thesis: Development of earth-abundant $\text{Cu}_2\text{ZnSnSe}_4$ solar cells on flexible titanium substrate
- Advisor: Seokwoo Jeon
- GPA : 3.61/4.3

KAIST(Korea Advanced Institute of Science and Technology)

Daejeon, S.Korea

B.S. IN CHEMICAL AND BIOMOLECULAR ENGINEERING

Mar. 2013 - Feb. 2018

- GPA : 3.56/4.3

Research Experience

SF2 Logic device, M1 24P Task Force

S.Korea

SAMSUNG ELECTRONICS, FOUNDRY

Jun. 2025 - Sep. 2025

- Improved 2nm logic device yield through 24P (13 nm width, 11 nm space) BEOL(Back-End-of-line) process scheme optimization
- Developed SESL(Single Etch stopped layer) scheme in 2nm logic device

SF2 Logic device, BEOL Process Architecture

S.Korea

SAMSUNG ELECTRONICS, FOUNDRY

Jun. 2023 - May. 2025

- Developed SF2 (Samsung Foundry 2nm) Logic device BEOL interconnect part
- Enhanced SF2 logic device performance using CuMn and a thin Co liner
- Enhanced SF2 Logic Device performance with High density Low-k material in interconnection

SF3 Logic device, BEOL Process Architecture

S.Korea

SAMSUNG ELECTRONICS, SEMICONDUCTOR R&D CENTER/FOUNDRY

Mar. 2021 - MAY. 2023

- Replaced ALD barrier metal with reverse-selected barrier metal, reducing resistance and enhancing device performance
- Developed a self-aligned universal patterning process for the first, second, and third narrow-width BEOL metal layers

SF4 Logic device, BEOL Technology development

SAMSUNG ELECTRONICS, SEMICONDUCTOR R&D CENTER

S.Korea

Mar. 2020 - Feb. 2021

- Improved SF4 Logic device yield by Litho–Etch–Litho–Etch process combined with cut patterning
- Enhanced SF4 Logic device performance with ALD Barrier metal process

Cu₂ZnSnSe₄ Solar Cell

KAIST, KOREA INSTITUTE OF ENERGY RESEARCH (KIER)

Daejwon, S.Korea

Mar. 2018 - Feb. 2020

- Development of earth-abundant Cu₂ZnSnSe₄ solar cells on flexible titanium substrate
- effects of Film Growth Temperatures on Device Performances

Publications

* denotes co-first authors, and † denotes co-corresponding authors

INTERNATIONAL JOURNAL

1. Muhammad Rehan, **Hyeonmin Jeon**, Yuna Cho, Ara Cho, Kihwan Kim, Jun-Sik Cho, Jae Ho Yun, Seungkyu Ahn, Jihye Gwak, Donghyeop Shin, “Fabrication and Characterization of Cu₂ZnSnSe₄ Thin-Film Solar Cells Using a Single-Stage Co-Evaporation Method: Effects of Film Growth Temperatures on Device Performances,” *Energies*, vol. **HLIM: vol num**, no. **HLIM: no num**, pp. **HLIM: from–HLIM: to**, Jan. 2020.

INTERNATIONAL CONFERENCE

1. **Hyeonmin Jeon**, **HLIM: fill other co-authors**, “Effect of CdS Air-Annealing on the Performance of CZTSe Solar Cells,” *Global Photovoltaic Conference*, Poster presentation, 2019.

Patents

Semiconductor device having via

SAMSUNG ELECTRONICS

S.Korea

Dec. 2022

- Patent No. 1020220173047

Honors & Awards

- 2026- **SAMSUNG**, Full funding for graduate school
- 2019 **KAIST**, KAIST support scholarship
- 2018 **KAIST**, KAIST support scholarship
- 2017 **KAIST**, KAIST support scholarship
- 2014-2016 **KAIST**, Merit-based KAIST support scholarship
- 2013 **KAIST**, KAIST support scholarship