Hyeonmin **Jeon**

Software Engineer
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Currently Employed Samsung Electronics Foundry

Education

KAIST(Korea Advanced Institute of Science and Technology) *Daejeon, S.Korea*

M.S. in Materials Science and Engineering *Mar. 2018 - Feb. 2020*

- Thesis: Development of earth-abundant $Cu_2ZnSnSe_4$ solar cells on flexible titanium substrate
- Advisor: Seokwoo Jeon
- GPA : 3.61/4.3

KAIST(Korea Advanced Institute of Science and Technology) *Daejeon, S.Korea*

B.S. in Chemical and Biomolecular Engineering *Mar. 2013 - Feb. 2018*

- GPA : 3.56/4.3

Research Interest

Neuromorphic Devices, Heterogeneous Integration, Nanoelectronics

Research Experience

SF2 Logic device, M1 24P Task Force *S.Korea*

Samsung Electronics, Foundry *Jun. 2025 - Sep. 2025*

- Improved 2nm logic device yield through 24P (13 nm width, 11 nm space) BEOL(Back-End-of-line) process scheme optimization
- Developed SESL(Single Etch stopped layer) scheme in 2nm logic device

SF2 Logic device, BEOL Process Architecture *S.Korea*

Samsung Electronics, Foundry *Jun. 2023 - May. 2025*

- Developed SF2 (Samsung Foundry 2nm) Logic device BEOL interconnect part
- Enhanced SF2 logic device performance using CuMn and a thin Co liner
- Enhanced SF2 Logic Device performance with High density Low-k material in interconnection

SF3 Logic device, BEOL Process Architecture *S.Korea*

Samsung Electronics, Semiconductor R&D Center/Foundry *Mar. 2021 - MAY. 2023*

- Replaced ALD barrier metal with reverse-selected barrier metal, reducing resistance and enhancing device performance
- Developed a self-aligned universal patterning process for the first, second, and third narrow-width BEOL metal layers

SF4 Logic device, BEOL Technology development *S.Korea*

Samsung Electronics, Semiconductor R&D Center *Mar. 2020 - Feb. 2021*

- Improved SF4 Logic device yield by Litho–Etch–Litho–Etch process combined with cut patterning
- Enhanced SF4 Logic device performance with ALD Barrier metal process

$Cu_2ZnSnSe_4$ Solar Cell *Daejwon, S.Korea*

KAIST, Korea Institute of Energy Research (KIER) *Mar. 2018 - Feb. 2020*

- Development of earth-abundant $Cu_2ZnSnSe_4$ solar cells on flexible titanium substrate
- effects of Film Growth Temperatures on Device Performances

Publications

Fabrication and Characterization of $Cu_2ZnSnSe_4$ Thin-Film Solar Cells Using a Single-Stage Co-Evaporation Method: Effects of Film Growth Temperatures on Device Performances

energies *Jan. 2020*

- Muhammad Rehan, Hyeonmin Jeon, Yunae Cho, Ara Cho, Kihwan Kim, Jun-Sik Cho, Jae Ho Yun, Seungkyu Ahn, Jihye Gwak, Donghyeop Shin

Patents

Semiconductor device having via *S.Korea*

SAMSUNG ELECTRONICS *Dec. 2022*

- Patent No. 1020220173047

Conferences

GPVC (Global Photovoltaic Conference) *Gwangju, S.Korea*

Poster *Mar. 2019*

- Effect of CdS Air-Annealing on the Performance of CZTSe Solar Cells

Honors & Awards

2026- **SAMSUNG,** Full funding for graduate school

2019 **KAIST,** KAIST support scholarship

2018 **KAIST,** KAIST support scholarship

2017 **KAIST,** KAIST support scholarship

2014-2016 **KAIST,** Merit-based KAIST support scholarship

2013 **KAIST,** KAIST support scholarship