```
module partA(
    input wire[3:0] a,
    input wire[3:0] b,
    input wire      c_in,

    output wire P;
    output wire G;
    output wire[3:0] sum
)
    wire p0, p1, p2, p3, g0, g1, g2, g3;
    assign  g0 = a[0]&b[0];
            g1 = a[1]&b[1];
            g2 = a[2]&b[2];
            g3 = a[3]&b[3];

    assign  p0 = a[0]|b[0];
            p1 = a[1]|b[1];
            p2 = a[2]|b[2];
            p3 = a[3]|b[3];

    assign P = p3 & p2 & p1 & p0;
           G = g3 | (p3&g2) | (p3&p2&g1) | (p3&p2&p1&g0);

    wire c1, c2, c3, c4;
    assign  c1 = g0 | (p0&c_in);
            c2 = g1 | (p1&g0) | (p1&p0&c_in);
            c3 = g2 | (p2&g1) | (p2&p1&g0) |
(p2&p1&p0&c_in);
            c4 = g3 | (p3&g2) | (p3&p2&g1) |
(p3&p2&p1&p0&c_in);

    assign  sum[0] = a[0] ^ b[0] ^ c[0];
            sum[1] = a[1] ^ b[1] ^ c[1];
            sum[2] = a[2] ^ b[2] ^ c[2];
            sum[3] = a[3] ^ b[3] ^ c[3];
endmodule
```

```
module partB(
    input wire p0,
    input wire g0,
    input wire p1,
    input wire g1,
    input wire p2,
    input wire g2,
    input wire p3,
    input wire g3,
    input wire      c_in,

    output wire     c1,
    output wire     c2,
```

```
    output wire     c3
)
    assign  c1 = g[0] | (p[0]&c_in);
            c2 = g[1] | (p[1]&g[0]) | (p[1]&p[0]&c_in);
            c3 = g[2] | (p[2]&g[1]) | (p[2]&p[1]&g[0]) |
(p[2]&p[1]&p[0]&c_in);

endmodule
```

```
module whole(
    input wire[15:0]    a,
    input wire[15:0]    b,
    input wire          c_in,

    output wire[15:0]   sum
)
    wire p0, g0, p1, g1, p2, g2, p3, g3;
    wire c1, c2, c3;

    partA partA_0(.a(a[3:0]), .b(b[3:0]), .c_in(c_in),
.P(p0), .G(g0), .sum(sum[3:0]));

    partA partA_1(.a(a[7:4]), .b(b[7:4]), .c_in(c1),
.P(p1), .G(g1), .sum(sum[7:4]));

    partA partA_2(.a(a[11:8]), .b(b[11:8]), .c_in(c2),
.P(p2), .G(g2), .sum(sum[11:8]));

    partA partA_3(.a(a[15:12]), .b(b[15:12]), .c_in(c3),
.P(p3), .G(g3), .sum(sum[15:12]));

    partB partB_0(.p0(p0), .g0(g0), .p1(p1), .g1(g1),
.p2(p2), .g2(g2), .p3(p3), .g3(g3)
                  .c_in(c_in), .c1(c1), .c2(c2), .c3(c3));
endmodule
```