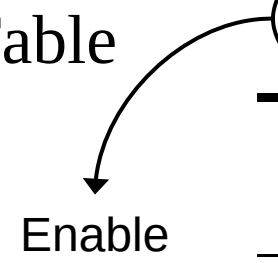
2-to-4 Decoder with Enable, 3-to-8 Decoder.

CVLSI
601系統晶片實驗室

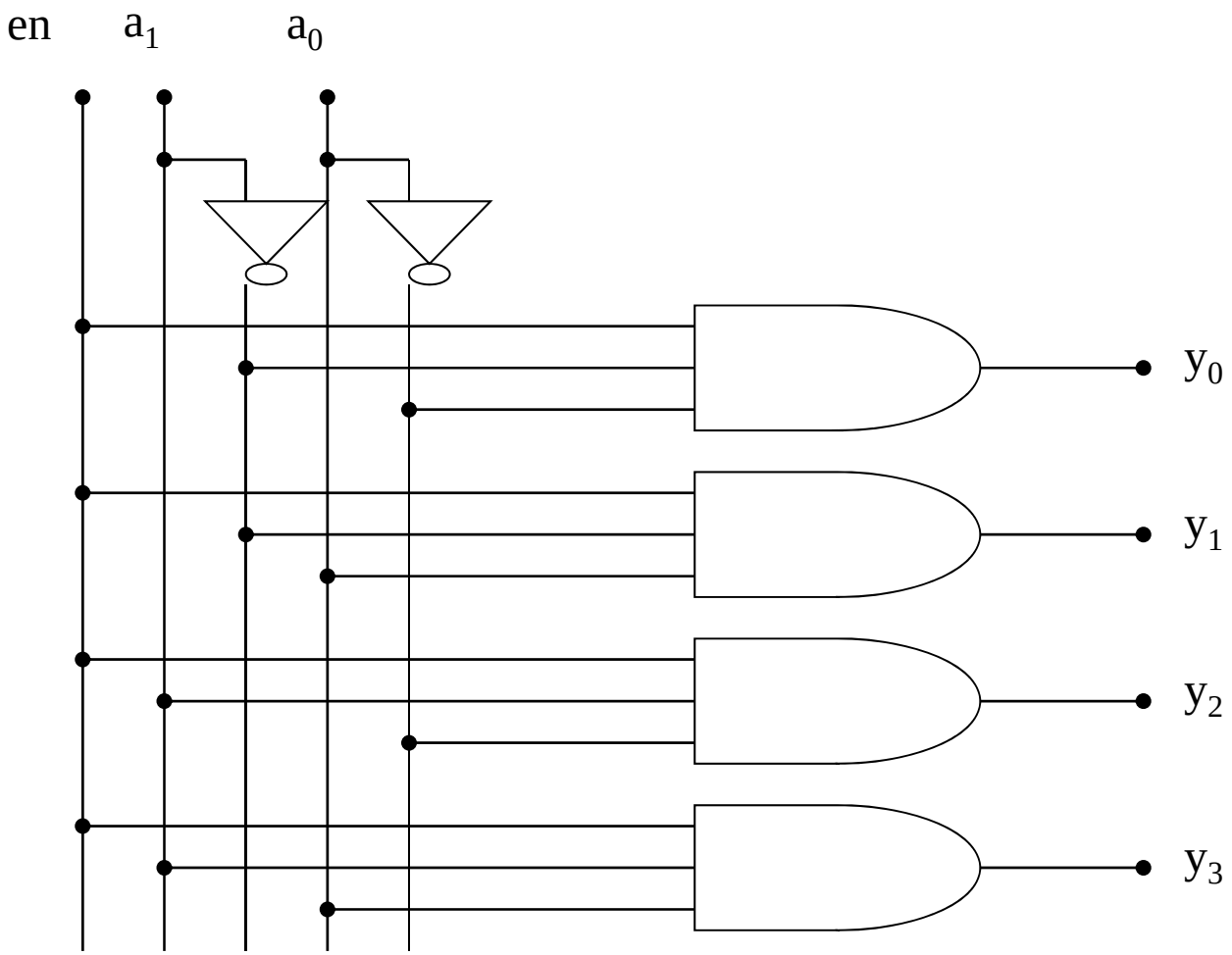
2:4 Decoder with Enable

- Truth Table



en	a_1	a_0	y_3	y_2	y_1	y_0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

2:4 Decoder with Enable

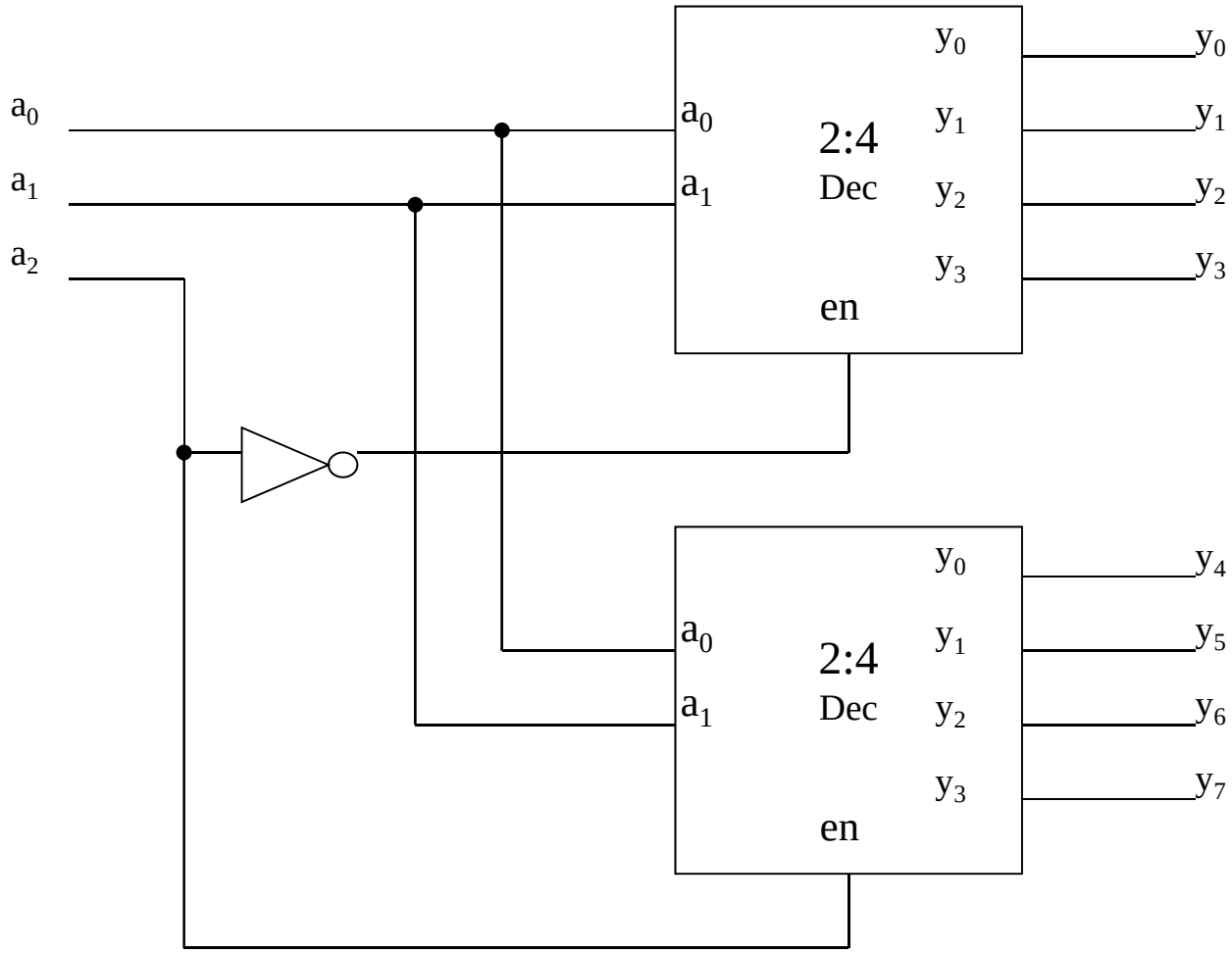


3:8 Decoder

- Truth Table

a_2	a_1	a_0	y_7	y_6	y_5	y_4	y_3	y_2	y_1	y_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

3:8 Decoder


a0
a1
a2
a0
a1
2:4
Dec
en
y0
y1
y2
y3
y0
y1
y2
y3
a0
a1
2:4
Dec
en
y0
y1
y2
y3
y4
y5
y6
y7