16:4 Encoder, & 7-Segment Display Decoder

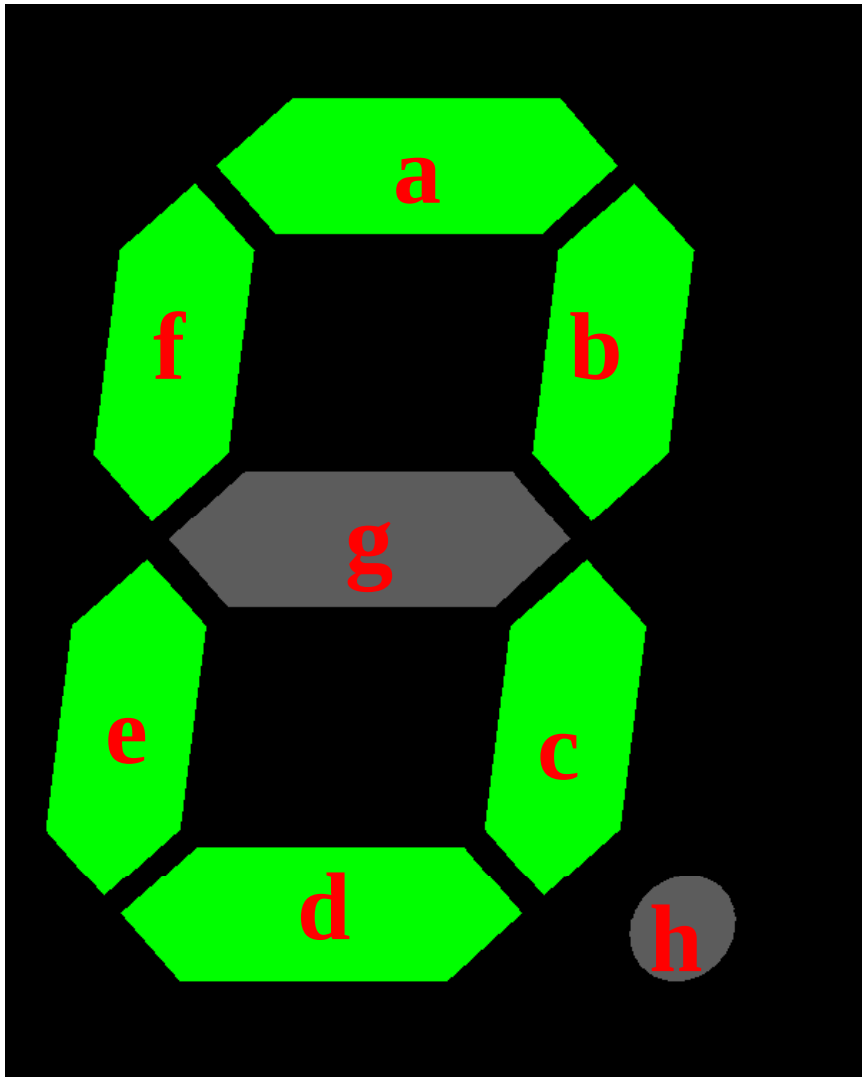
CVLSI

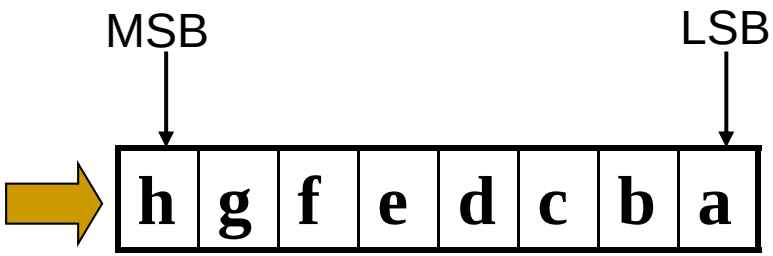
601系統晶片實驗室

16-to-4 Encoder: Truth Table

Input																Output			
I_{15}	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	O_3	O_2	O_1	O_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Seven-Segment Display

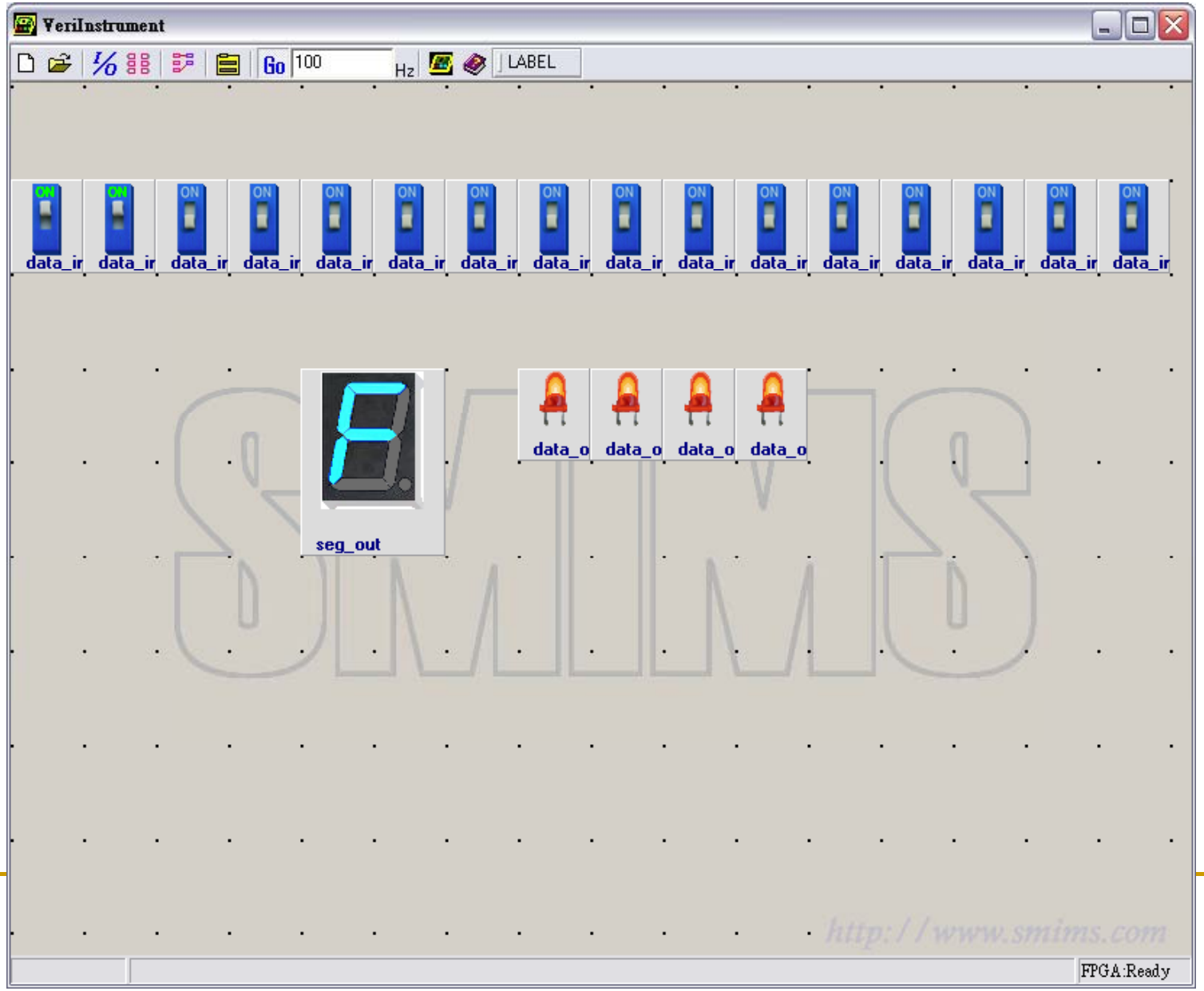




Seven-Segment Display Decoder

Input					Output						
I_3	I_2	I_1	I_0		g	f	e	d	c	b	a
0	0	0	0	0	0	1	1	1	1	1	1
0	0	0	1	1	0	0	0	0	1	1	0
0	0	1	0	2	1	0	1	1	0	1	1
0	0	1	1	3	1	0	0	1	1	1	1
0	1	0	0	4	1	1	0	0	1	1	0
0	1	0	1	5	1	1	0	1	1	0	1
0	1	1	0	6	1	1	1	1	1	0	1
0	1	1	1	7	0	0	0	0	1	1	1
1	0	0	0	8	1	1	1	1	1	1	1
1	0	0	1	9	1	1	0	1	1	1	1
1	0	1	0	A	1	1	1	0	1	1	1
1	0	1	1	b	1	1	1	1	1	0	0
1	1	0	0	C	0	1	1	1	0	0	1
1	1	0	1	d	1	0	1	1	1	1	0
1	1	1	0	E	1	1	1	1	0	0	1
1	1	1	1	F	1	1	1	0	0	0	1

Result on VeriInstrument



Seven-Segment Display: 10~15

E
01111001

C
00111001

A
01110111

F
01110001

d
01011110

b
01111100

Top Module

- Schematic: