4-bit DFF Counter with Asynchronous Clock.

CVLSI
601系統晶片實驗室

D-Flip-Flop with Clock Negative Edge Triggle. (時脈負緣觸發的D型正反器)

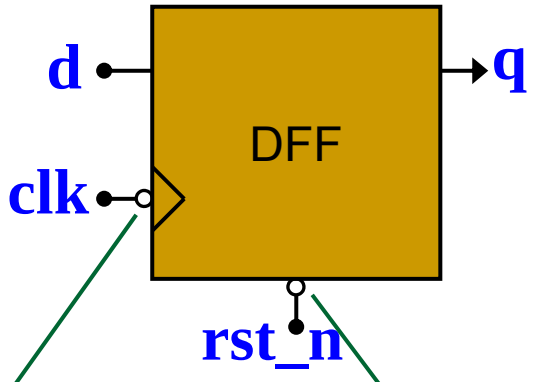
Truth Table:

Clock	D	$Q_{current}$	
↓	0	0	(Load)
↓	1	1	(Load)
–	X	$Q_{presous}$	(Hold)

(Negative Edge Triggle)

(Clock non-change)

(Don't care)

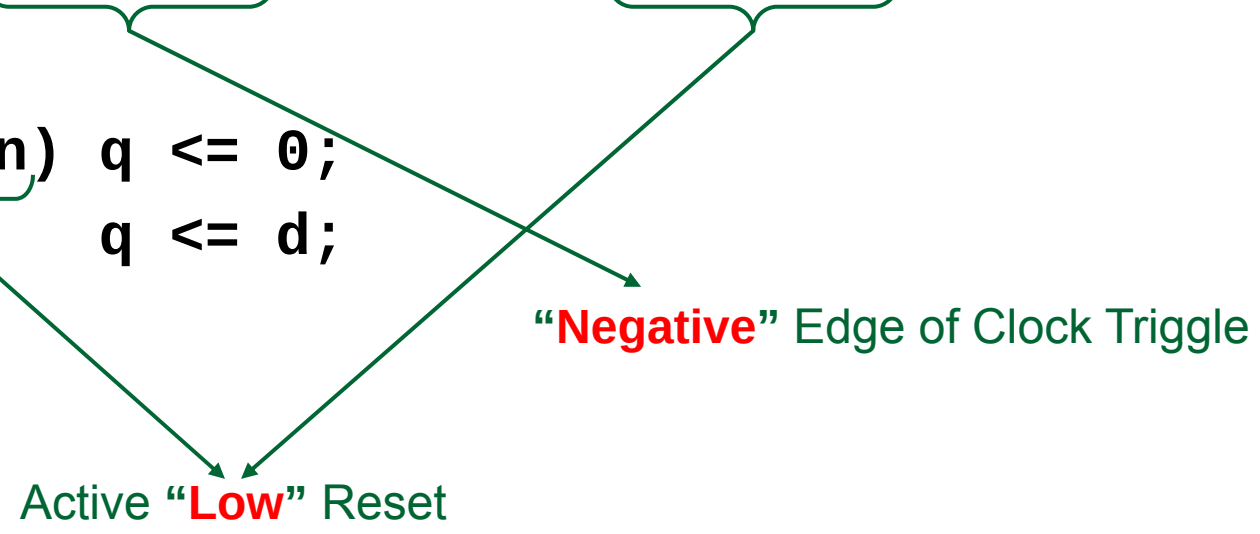


"Negative" Edge of Clock Triggle

Active "Low" Reset

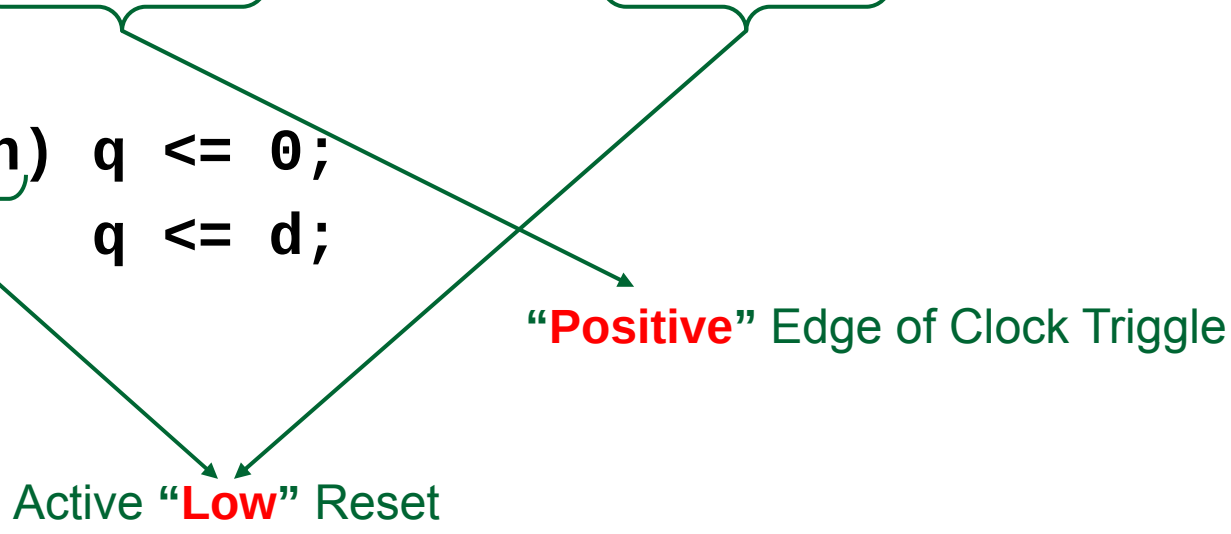
D-Flip-Flop with Clock Negative Edge Triggle. (Behavioral-level module) for "上數"

```
module dff(q, d, clk, rst_n);
  output reg q;
  input      d, clk, rst_n;
  always @(negedge clk or negedge rst_n)
  begin
    if (~rst_n) q <= 0;
    else        q <= d;
  end
endmodule
```

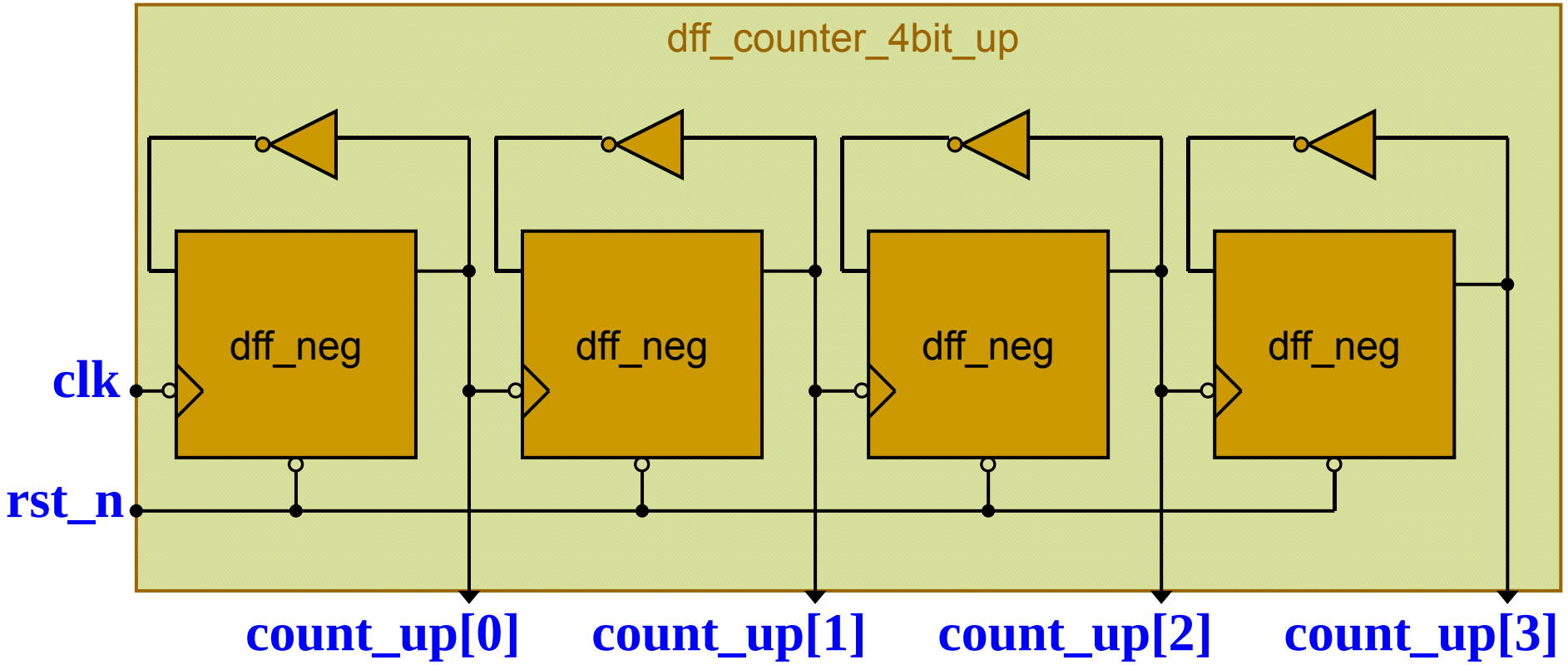


D-Flip-Flop with Clock Positive Edge Triggle. (Behavioral-level module) for "下數"

```
module dff(q, d, clk, rst_n);
  output reg q;
  input      d, clk, rst_n;
  always @(posedge clk or negedge rst_n)
  begin
    if (~rst_n) q <= 0;
    else        q <= d;
  end
endmodule
```



4-bit DFF Counter with Asynchronous Clock.
(四位元D型正反器式非同步計數器)

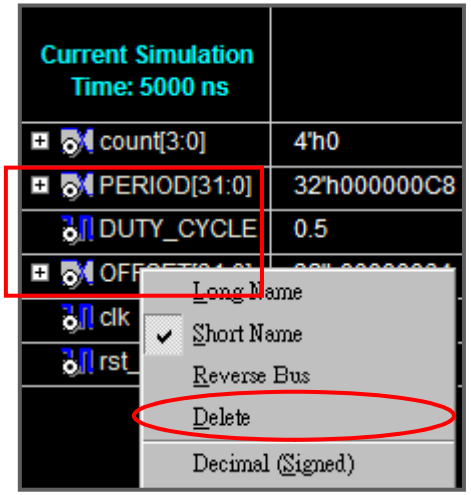


Caution: the “Clock Edge”.

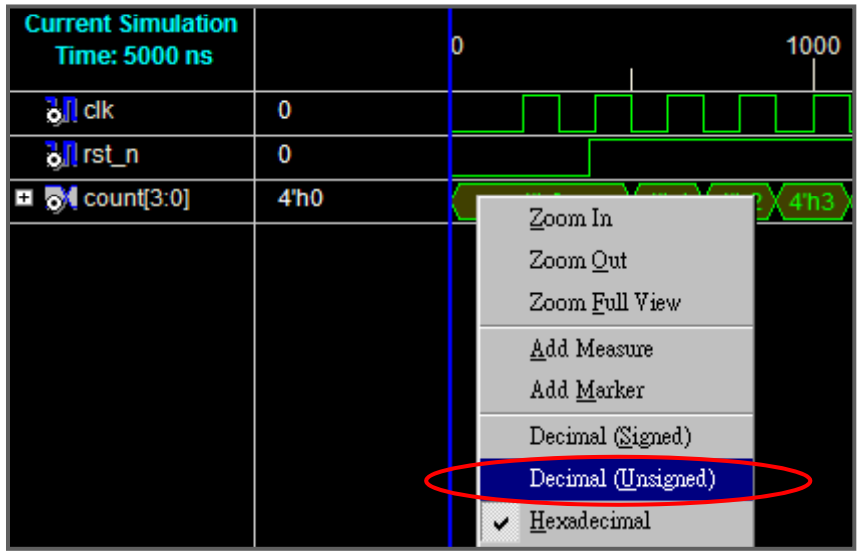
- If DFF is clock “Negative” edge triggle,
  - then the 4-bit DFF counter would be counted “Up”.
- If DFF is clock “Posedge” edge triggle,
  - then the 4-bit DFF counter would be counted “Down”.

Q1: Simulation by Xilinx ISE Simulator.

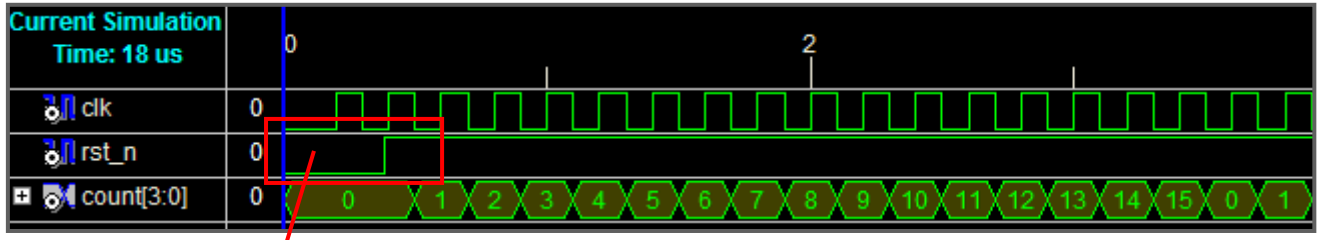
1st : Delete unwanted entrys, and re-order these entrys.



2nd : Change display format. (Hex → Unsiged Decimal)

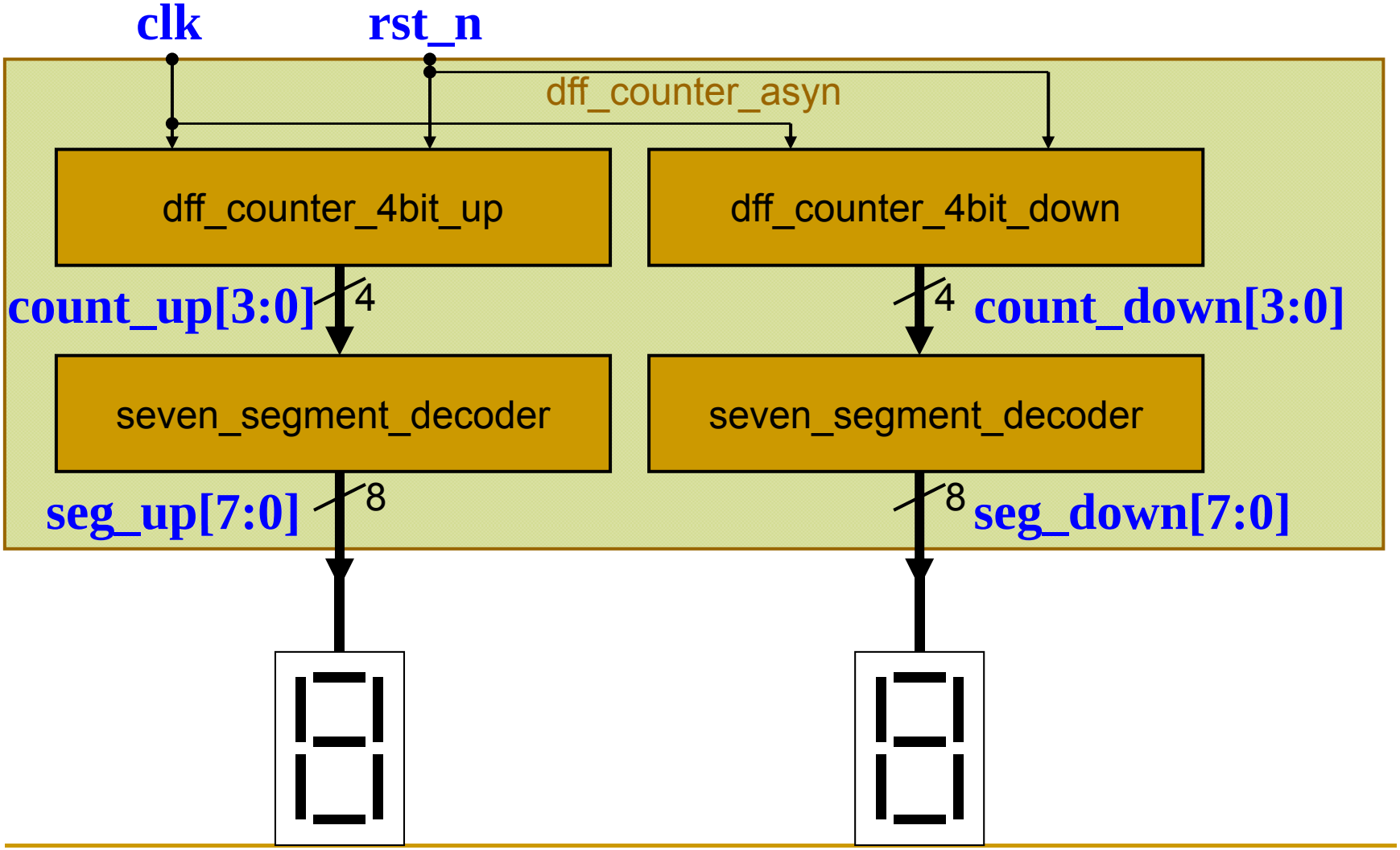


3nd : Final View.



Because active “Low” reset.

Top Module. (included 7-Seg Decoder)



Q2: Emulation by VeriInstrument.