

#1 (a) ASIC: Design for specific function

Pro: can have better PPA

Cons: cost more time and money

FPGA: Is programmable on FPGA board, use switch to connect the gate.

Pro: Much faster than ASIC, can compile many times.

Cons: The total area can't be optimized, since the FPGA chip is already exist.

001010 (41.5)

(c) "==" compare the value of LHS & RHS, Good.

"==" will compare LHS & RHS element bit by bit.

(d) wire X;

assign X = Y + 1; (1)

combinational loop will have latch.

Why latch should be prevent

(e) 1. RTL Design : Design the function of chip (8)

2. Synthesis : Choose suitable predesign cell library (e.g. tsmc, umc) to produce the synthesized netlist file.

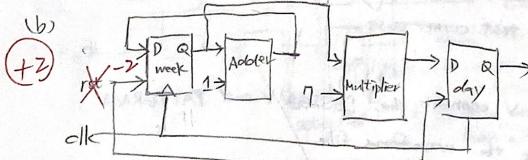
3. Place and Route : physical design to put each cell and net in to the chip.

4. Fabrication : Produce the real chip by fab (tsmc, umc)

#2.

(a) ① posedge clk ✓

② rst



(b) asynchronous reset

Pros: can use without clk. ✓

Cons: larger area, noise cause unwanted reset ✓

synchronous reset

Pros: small area, more stable. ✓

Cons: can't use without clk. ✓

(d)

No, since the "week" reg input is also "week" ✓
so if remove line 5, the first clk will be unknown.

#3. (9)

To dump the waveform of each reg and wire
MDA & memory -

(b) To read the sbf file generated by synthesis stage.

Standard Delay Format file describle the delay of each gate
if we not read the sof file in gate level simulation
will use the default delay. Then it may cause the warning
of timing violation.

② Directed method. and random method.

The random method can fast cover the case near to 100%.

④ But if we want to reach 100% coverage, we need to directed method. to test corner case.

③ TESTBENCH.V connect the DESIGN.V and PATTERN.V

then generate the waveform file

⑥ PATTERN.V generate the test data and verify RTL.V is correct or not.
RTL.V is the design of the chip.

④ Timescale 1ns/XXX ps

(a) 1ns means the unit

XXX ps is precision

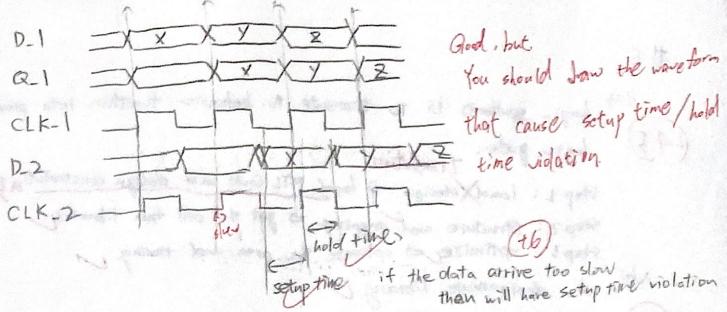
b) $XXX = 10^3$

CYCLE will be 2.45 ns.

#4.

(a) setup time violation is the time the signal should arrive and stable before the clock trigger less than t_{setup}

hold time violation is the time the signal should retain after the clock trigger less than t_{hold} .



⑥ Since the data arrive to from combinational logic will be stable

if the input of combinational logic is stable. So hold time will usually be MET.

(d) //translate off
//include "DW02_mult.v"
//translate on

#5 (1)~(3) ab6 v3 of stand by : the SRAM is standby and won't write and re

(4)~(6) bbb, (14) h write : write the data into SRAM

(11)~(13) bab v3 e read : read the data from SRAM

(15)~(17) 0ca f high-2 : the SRAM will not affect.

⑦ Memory.v file are unsynthesize behavior function, we used it in simulation what simulation? -1

(x3) Memory lib file contain the delay of memory, it used it in synthesis and area

(c) input pin 16 \Rightarrow input [3:0]

(x2) address pin 17 \Rightarrow address [17:0]

(d) Soft IP : RTL design, need verification

(x3) Hard IP : (EDSII) format, technology demand

Firm IP : behaviour design

-2

#6.

- (a) Logic synthesis is to translate behavior function into predesign logic gate.

+4.5

Step 1: load ~~ofdesign~~ \Rightarrow load RTL code and design constraint a5

Step 2: structure and mapping \Rightarrow get the cell from libraries ✓

Step 3: optimize \Leftrightarrow optimize the area and timing ✓

- (b)
- A. designware library ✓

+1

- B. Xtechnology process library.

- c. Xgeneric technology library

+10

- (c)
- (d)

- a. Compile-once dont touch

+5

- b. ungroup ✓

- c. ungroup.