ICLab-Lab11 Sharing

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Minimize the number of pad

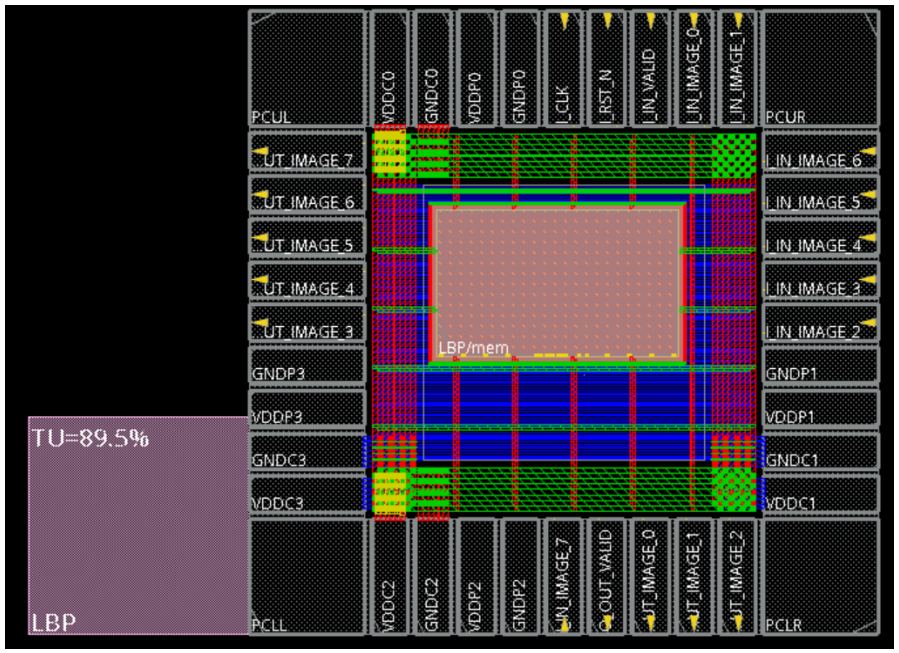
- Use as less pads as possible without any violation

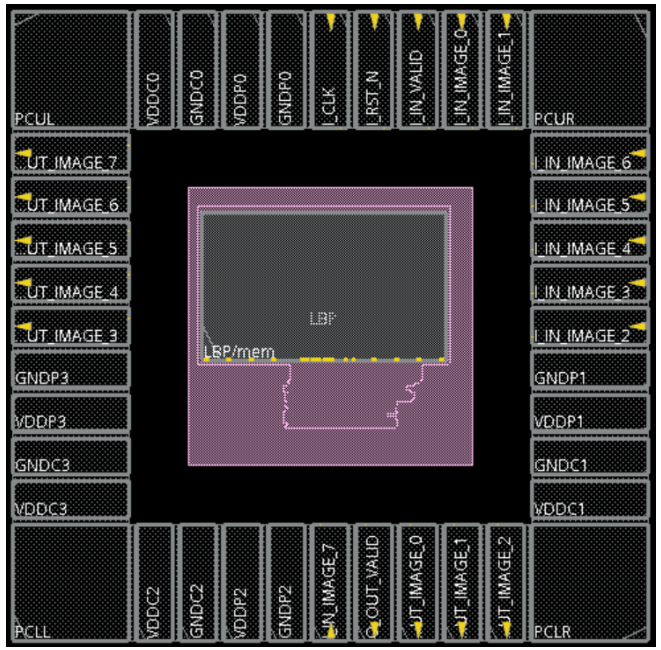
```
PVDDR VDDP0 ();
PVSSR GNDP0 ();
PVDDR VDDP1 ();
PVSSR GNDP1 ();
PVDDR VDDP2 ();
PVSSR GNDP2 ();
PVDDR VDDP3 ();
PVSSR GNDP3 ();
PVDDR VDDP4 ();
PVSSR GNDP4 ();
PVDDR VDDP5 ();
PVSSR GNDP5 ();
PVDDR VDDP6 ();
PVSSR GNDP6 ();
PVDDR VDDP7 ();
PVSSR GNDP7 ();
```

```
PVDDR VDDP0 ();
PVSSR GNDP0 ();
PVDDR VDDP1 ();
PVSSR GNDP1 ();
PVDDR VDDP2 ();
PVSSR GNDP2 ();
PVDDR VDDP3 ();
PVSSR GNDP3 ();
```

Finetuning the core utilization

- The higher of core utilization, the lower of core area
- Finetune it by manually attempt
- The core area should still be able to fit the macro block





Other attempts

- Reordering the pads
  - Uniformly distributing the pads could help avoid violations
  - Not sure whether it affects performance much
- Minimize the clock period after APR to further enhance performance