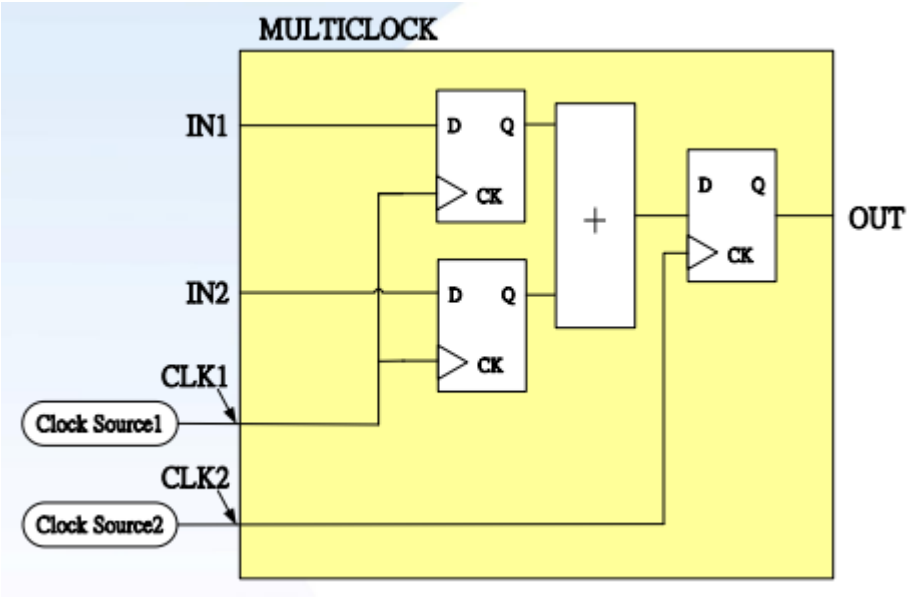
IC Lab Final Exam
2022 Spring

Name:_____ Student ID:_____ Account: iclab_____

Total score: 100%

1. [17%] Lab07

   (1) Multicycle [8%]



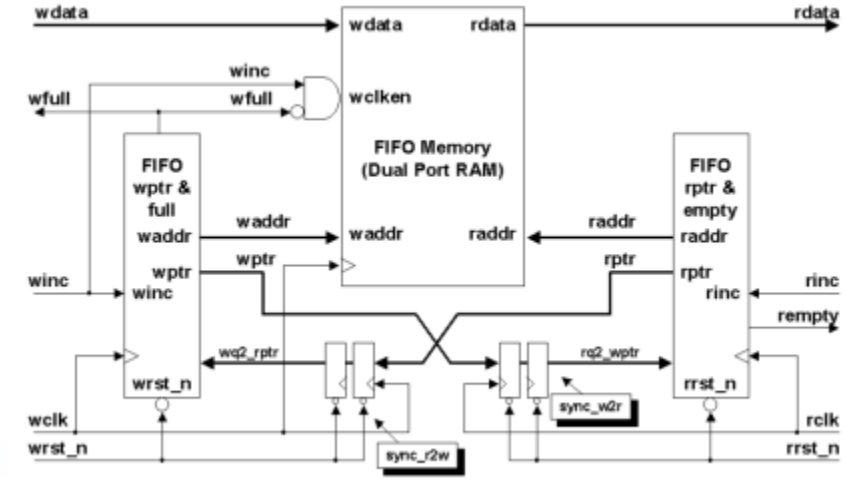
Clock 1 period is 16 ns. Clock 2 period is 8 ns. The operation needs 30 ns.

(a) Please write down the multicycle command to let the setup time check and hold time check can pass. (using the -start option) Just fit the design, don't use too many cycles.

(b) Please write down the multicycle command to let the setup time check and hold time check can pass. (using the -end option) Just fit the design, don't use too many cycles.

(Hint: set_multicycle_path X (-hold) (-end) -from CLK1 -to CLK2)

(2) Asynchronous FIFO [9%]



(a) How does this design deal with the full/empty problem?

(b) Why this design's pointer using gray code?

(c) Why we need to set_dont_touch the synchronizer at synthesis stage?

2. [16%] Lab08

(1) SystemVerilog [6%]

(a) What's the difference between program and module?

(b) What's the difference between structure and union?

(2) Please use the following template to implement the function:

When **enable** is 0, **ans** should be 0

When **mode** is 0 and **enable** is 1, **ans** is the random number ranged from 1~31

When **mode** is 1 and **enable** is 1, **ans** is the random number ranged from 32~63

All signals are triggered when posedge clk.

```
program automatic RAND_NUM(input clk, INF.RAND_NUM inf);

//This is part of the code in INF
/*
logic enable, mode;
logic[5:0] ans;
modport RAND_NUM(
    input enable, mode,
    output ans
);
*/

class random_num;
    //Complete the code here
endclass

//Complete the code here

endprogram
```

3. [16%] Lab09

(1) Covergroup [6%]

If we want to create a covergroup *cg* and sample the value of signals at negedge clk when the out_valid is high. What is the problem when using the code below? How can we correct it?

```
module Checker(input clk, INF.CHECKER inf);
//INF.CHECKER includes out_valid

covergroup cg@(negedge clk iff inf.out_valid);
    //Suppose the code here is correct
    ''''''
endgroup

cg cg_inst = new();
always_ff @(negedge clk)begin
        if(inf.out_valid)begin
                cg_inst.sample();
        end
end

endmodule
```

(2) Assertion [10%]

If we want to check whether our design hits the specification, we can write the assertion in the checker.sv file. There are two signals, A and B in the design, and two signals are triggered when posedge clk. Please finish the two assertions below. Notice that you cannot use always block here.

(a) If A is 0, then 2 or more cycles later, B should be high.

(b) If A is 1, 5 clock cycles ago, B should be 1 for 2 cycles.

Assertion1: assert property (@(posedge clk) ……);
Assertion2: assert property (@(posedge clk) ……);

4. [18%] Lab10

(a) How to reduce static & dynamic power dissipation? Please list 2 methods respectively and describe how these methods can help to reduce power dissipation. [1.5%*4]

(b) The clock gating design could be implemented by either AND-gating or OR-gating. Why OR-gating is better than AND-gating? [4%]

(c) What's the difference between SAIF and VCD file used to evaluate power consumption? If we want to do peak power analysis, which file should we use? Why? [8%]

5. [17%] Lab11
   (1) Why we don't check the hold time before CTS? [3%]
   (2) Please list 2 routing-based SI prevention. [4%]
   (3) Please write down the correct order of APR flow. (e.g. (i) → (ii) → (iii) → (iv) → (v)) [10%]
      (a) Before CTS: (i) Pre-CTS Optimization (ii) IO, P/G Placement (iii) Standard Cell Placement (iv) floorplan/powerplan (v) Timing Analysis
      (b) After CTS: (i) Add PAD filler (ii) Add CORE Filler Cells (iii) Post-Route Timing Analysis (iv) Route (v) Post-CTS Timing Analysis

6. [8%] Lab12
   (a) What is the root cause of IR drop? (Please list 2 methods to solve it.) [4%]
   [hints] Adopt some methods that could shorten the path from cell to power supply.
   (b) What is rail analysis? What is power analysis? [4%]
7. [8%] SEC
   (a) Explain how the SEC can help us check the equivalency between RTL design (specification) and optimized RTL design (implementation)? [4%]
   (b) What does "waive" mean and when will we use this command? [4%]