Course Schedule:

Week	Date	Course Content	TA
1	02/16	00、Introduction + Environment Setting	林文約
2	02/23	01、Cell Based Design Methodology + Verilog Combinational Circuit Programming	洪子軒
3	03/02	02、Finite State Machine + Verilog Sequential Circuit Programming	劉恆宇
4	03/09	03、Verification & Simulation + Verilog Test Bench Programming	盧昱偉
5	03/16	04、Sequential Circuit Design II (STA + Pipeline)	洪子軒
6	03/23	05、Memory & Coding Style (Memory Compiler + SuperLint)	盧昱偉
7	03/30	06、Synthesis Methodology (Design Compiler + IP Design)	劉恆宇
8	04/06 04/09	No class : Study Days **Midterm Exam (Online Test) (Sat. Afternoon, about 6h)**	x
9	04/13	07、Timing: Cross Clock Domain + Synthesis Static Time Analysis	張弘坤
10	04/20	08、System Verilog (Design)	彭志偉
11	04/27	09、System Verilog II (Verification)	彭志偉
12	05/04	(Bonus) System Verilog (Formal Verification)	林文約
13	05/11	10、Power: Low Power Design	許毓倫
14	05/18	11、APR I : From RTL to GDSII	張弘坤
15	05/25	12、APR II : IR-Drop Analysis	許毓倫
16	06/01	**Final Exam**	x
18	06/12	**Final Project Deadline (2nd demo @06/19, 3rd demo @06/22)**	