Lab07 Design Consideration

Tz-Hsi, Lin

2022/05/18

Agenda

- Strategies
- Implementations

Strategies

Things about the Performance Definition

- The performance is defined as $(clk1) \times (total\ latency)^{1.3} \times (area)$.
- We can find that the period of clk2 is meaningless.
- Put the calculation part in the clk2 domain.
- Hence, the period of clk1 can be quite small. The only thing that happened in the clk1 domain is putting the input data into the register.

Strategies

Things about the Performance Definition

- Here comes the trade-off between area and clock period.

  (1) 1 * AFIFO, calculation in the clk1 domain

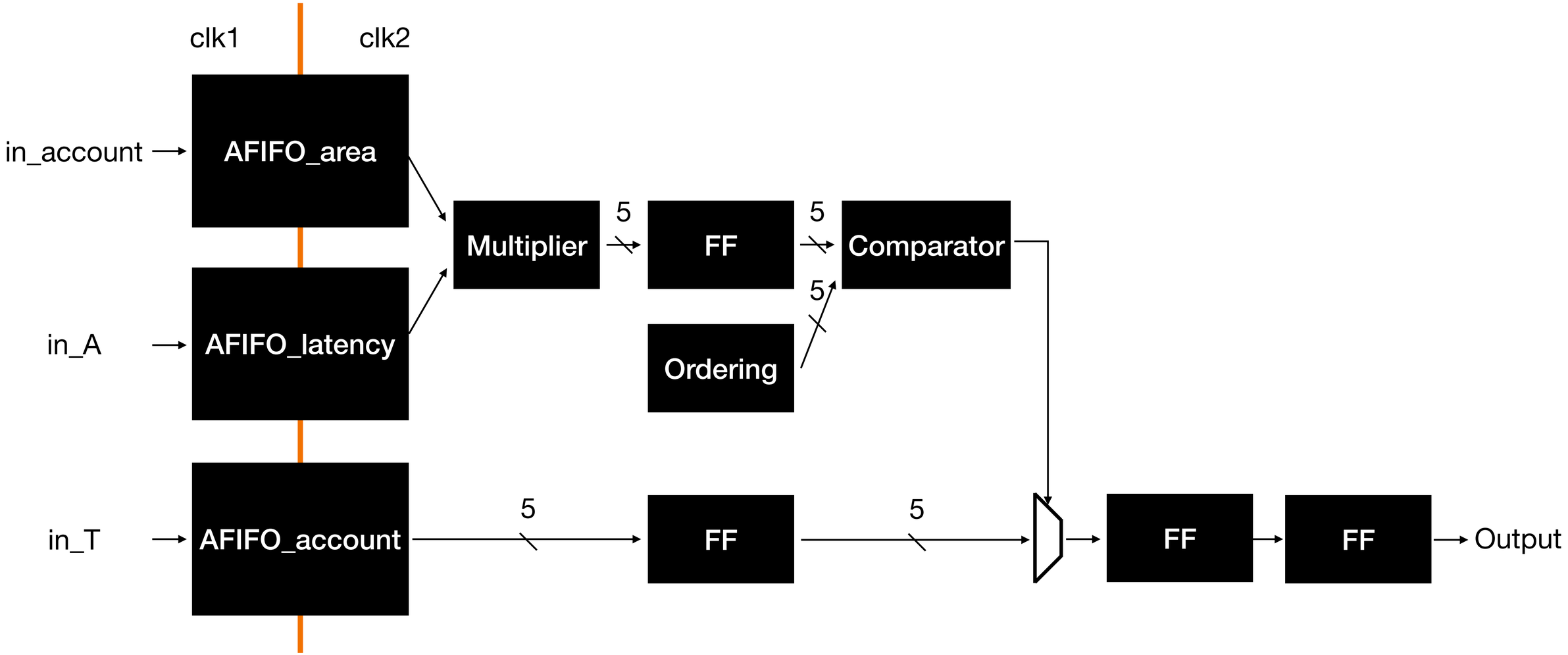
  (2) 3 * AFIFO, calculation in the clk2 domain

- I had implemented both of them, and I found that the second one is a better solution for my design.

- So, we'll focus on the second one.

Strategies

Structures

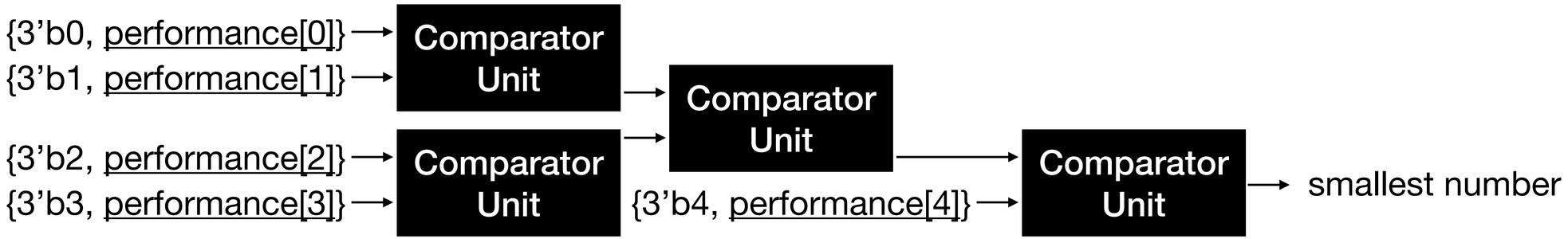


Implementations

Comparator

performance[0]	performance[1]	performance[2]	performance[3]	performance[4]

account[0]	account[1]	account[2]	account[3]	account[4]

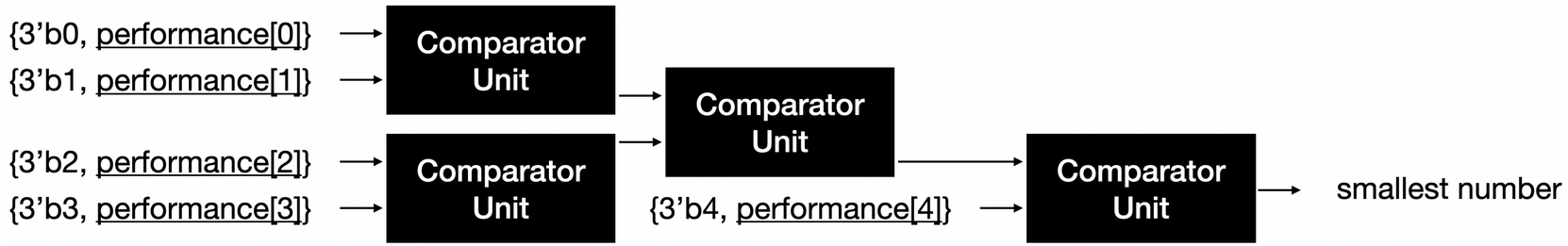


Implementations

Code

```
module SMALLEST #(parameter DSIZE = 8)(A, B, C, D, E, smallest);
    input [DSIZE * 2 - 1: 0] A, B, C, D, E;
    output [2: 0] smallest;

    wire [DSIZE * 2 + 2: 0] tempA, tempB, tempC, tempD, tempE;
    wire [DSIZE * 2 + 2: 0] L1, L2, L3, L4;

    assign tempA = {3'd0, A};   assign tempB = {3'd1, B};
    assign tempC = {3'd2, C};   assign tempD = {3'd3, D};   assign tempE = {3'd4, E};

    COMP #(.DSIZE(DSIZE)) C0(.A(tempA), .B(tempB), .smaller(L1));
    COMP #(.DSIZE(DSIZE)) C1(.A(tempC), .B(tempD), .smaller(L2));
    COMP #(.DSIZE(DSIZE)) C2(.A(L1),    .B(L2),    .smaller(L3));
    COMP #(.DSIZE(DSIZE)) C3(.A(L3),    .B(tempE), .smaller(L4));

    assign smallest = L4[DSIZE * 2 + 2: DSIZE * 2];
endmodule
```

```
module COMP #(parameter DSIZE = 8)(A, B, smaller);
    input [DSIZE * 2 + 2: 0] A, B;
    output [DSIZE * 2 + 2: 0] smaller;

    assign smaller = (A[DSIZE * 2 - 1: 0] <= B[DSIZE * 2 - 1: 0])? A: B;
endmodule
```



Tz-Hsi Lin presented

hsicc.ee10@nycu.edu.tw

2022/05/18