NCTU-EE IC Design LAB – 2022 Spring

Course Rule

I. Grading Policy (Subject to changes)

Weekly Lab Exercise * 12	(60%)	
Midterm Project	(10%)	
Midterm Exam	(8%)	
Online Test	(6%)	
Final Project	(10%)	
Final Exam	(8%)	
Bonus (Formal Verification)	(3%)	

II. Lab Exercise Demo

▶ Lab Score: Functionality (70%) + Performance (30%) (May vary between labs)

Functionality:

Three demo chance for each lab, either "Pass" or "Fail" the functionality part.

Performance:

- 1. Calculate FOM using Area, timing, power etc., and score it according the rank in the class
- 2. You must "Pass" Functionality to have performance score

1st demo: Lab Score * 1, 2nd demo: Lab Score * 0.7, 3rd demo: 35% point

- **Demo time (Reference: 2022 Spring ICLAB Agenda.xlsx):**
 - Tue. 12:00 announce 1st demo result (upload your answer before Sun. 23:59 to New E3)
 TA will upload TA's pattern after the announcement of 1st demo result
 If you pass the announced pattern, you will pass the demo
 - 2. If you "Fail" 1st demo, upload your modified answer before Fri. 23:59 to New E3
 - 3. If you still haven't pass 2nd demo, please upload your answer before 6/22 for 3rd demo
- **➣** The lab score will be announced after 2nd demo
- > TA use Demo script to demo, so make sure the naming of each file is right
- > The best design will be released for everyone. We would invite the author to share his/her development in the next course (As an encouragement, for those students willing to share the best design, he/she could earn 1 semester score as bonus.)

- > If you're in emergency, please notice your TA at least one day in advance for no attendance of 1st and 2nd demo. You can postpone your demo but the exercise score will be counted as 45% points. Each student has only one chance to postpone his or her demo.
- > Everyone should finish the exercises on your own. The TAs would compare the source codes in each exercise. Once cheating is found, you would fail in this class.
- ➤ Notice that TA will compare the source code after midterm exam!

III. Questions and Announcements

- The related course notification will also be announced on new e3 campus platform (https://e3.nycu.edu.tw/). Please check your e-mail registered on e3 campus is AVAILABLE!
- > The lecture notes can be downloaded from e3 campus on Wednesday and exercise assignments can be downloaded at 12:00 at noon on Wednesday.
- > The discussion board is at Facebook 2022 Spring IC Lab Student Please join the Facebook group after the first class www.facebook.com/groups/939092310144637/
- > If you have questions to the course contents or the exercises details, please go to the discussion board on Facebook. The questions should be CLEAR (as template in the discussion board) and remember the TAs are not responsible for DEBUG.
- > Do not contact TA through FB messenger, please ask your question on the discussion board.
- > Only contact TA through e3 e-mail system when there's an emergency condition or personal issue, DO NOT CONTACT TA THROUGH FB MESSENGER.
- > Do not barge into TA's office without making a proper appointment.

IV. Webinar Online Course

Webex (https://nycu.webex.com/nycu/j.php?MTID=m81d7cdaf599b6450f38abe76aab10660)

V. ED415 Workstation

Workstation ED415 connection: (need NCTU IP, i.e.140.113.x.x) ssh (port = 22) to ee??.ee.nctu.edu.tw (?? = 01 ~ 06) or linux??.ee.nctu.edu.tw (?? = 02 ~ 35)

Do not use linux01

▶ Regulation for Room ED415:

> You are not allowed:

- 1. to restart or shutdown any computers in ED415.
- 2. to lock the screen of the computers.
- 3. to use the resource with no limitation.
- 4. to lend your ID account to other students.
- 5. to use the resource and equipment of ED415 for education-independent purpose.
- 6. to damage the equipment of ED415.
- 7. to hack other's ID account.
- 8. to do the illegal things that are not allowed and has been announced in the class or on the discussion forum.

Punishment :

- 1. If you have any illegal behavior consists of the point 1,2,3 listed above in the first time, your account will be suspended for 2 weeks. If you are a repeated offender, the account will be canceled.
- 2. If you have any illegal behavior consists of the point 4,5,6,7 listed above, your account will be canceled right away. In addition, you will not have any accounts in ED415 for any other course, either.
- 3. The punishment of the point 8 will be announced.

Please pay attention to :

- 1. Turn off the lock screen setup when you leave.
- 2. Do not bring foods into ED415.
- 3. Logout your ID account when you leave.

> Avoiding plagiarism

- 1. Any form of plagiarism is not allowed in this class. Plagiarism will lead to failure in this class.
- 2. Do not look at classmates' code or your senior's code.
- 3. Discussion between classmates is recommended, but do not discus on very specific details of your design and algorithm. This may lead to some misunderstanding between plagiarism or algorithm discussion.
- 4. Professor & TAs has the very right to ask you explain your codes/reports.
- 5. Do not copying codes from the internet, your classmates or your senior.

> ID Assignment for ED415 Workstation and Demo Group

- 1. Please use command passwd to change your password ASAP.
- 2. Please see the details on New e3 campus site (https://e3.nycu.edu.tw/)

VI. About TA

Every Student will be assigned to one TA after the first class:

- 1. Course content problems \rightarrow TA responsible for that Lab
- 2. Exercise problems → TA responsible for that Lab
- 3. Coding Style problems → Your TA
- 4. Demo result problems → Your TA and TA responsible for that Lab
- 5. Course arrange problems and other problems → Main TA

If the question is personal, student can use either New E3 or personal mail to sent email to the corresponding TA, remember to CC the email to Main TA!

If the question is general, please asked the question on Facebook group

Student cannot ask question through Messenger

Name	Email	Lab	Office
Wen-Yue Lin 林文約 (Main TA)	kenlin.ee09@nycu.edu.tw	Lab00, Bonus lab	ED430
Chih-Wei Peng 彭志偉	epeng.ee10@nycu.edu.tw	Lab 09, 10	ED430
Heng-Yu Liu 劉恆宇	nine87129.ee10@nycu.edu.tw	Lab 02, 06	ED430
Tzu-Hsuan Hung 洪子軒	davidhung.c@nycu.edu.tw	Lab 01, 04	ED430
Yu-Wei Lu 盧昱偉	ywlu1015.st10@nycu.edu.tw	Lab 03, 05	ED430
Yu-Lun Hsu 許毓倫	kimi870928.ee06@nctu.edu.tw	Lab 08, 12	ED317A
Hung-Kun Chang 張弘 坤	owwwojeff@gmail.com	Lab 07, 11	ED317A

Instructor:

• Chen-Yi Lee, National Yang Ming Chiao Tung University

Office: ED538Tel: 03-5731849

Mail: cylee@si2lab.org

Lecture:

3EF (13:30 ~ 15:30, Wednesday) @ Webex

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TA List:

Name	Email	Ext	Office
林文約	kenlin.ee09@nycu.edu.tw	54238	ED430
彭志偉	epeng.ee10@nycu.edu.tw	54238	ED430
劉恆宇	nine87129.ee10@nycu.edu.tw	54238	ED430
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許毓倫	kimi870928.ee06@nctu.edu.tw	54246	ED317A
張弘坤	owwwojeff@gmail.com	54246	ED317A

TA Time:

> 1EF (13:30 ~ 15:30, Monday) @ ED415 for Lab1~Lab4

Prerequisites:

Introduction to VLSI, Logic Design, Digital System Design, Computer Organization (opt)

Course Objectives:

This course aims to convey the senior and graduated EE students techniques to design the VLSI chips using state-of-the-art CAD tools. In addition to learning CAD tools for performance-driven and cost-effective IC designs, a top-down design flow and related environment will also be addressed. Upon completion of the course, the student will be able to design the integrated circuits and systems based on standard cell library as well as full-custom layout approaches. As such he/she will be able to work in a team of designers or stand alone.

Course Schedule:

Week	Date	Course Content	TA
1	02/16	00 · Introduction + Environment Setting	林文約
2	02/23	01 · Cell Based Design Methodology + Verilog Combinational Circuit Programming	洪子軒
3	03/02	02 · Finite State Machine + Verilog Sequential Circuit Programming	劉恆宇
4	03/09	03 · Verification & Simulation + Verilog Test Bench Programming	盧昱偉
5	03/16	04 · Sequential Circuit Design II (STA + Pipeline)	洪子軒
6	03/23	05 · Memory & Coding Style (Memory Compiler + SuperLint)	盧昱偉
7	03/30	06 · Synthesis Methodology (Design Compiler + IP Design)	劉恆宇
8	04/06 04/09	No class : Study Days Midterm Exam (Online Test) (Sat. Afternoon, about 6h)	Х
9	04/13	07 · Timing: Cross Clock Domain + Synthesis Static Time Analysis	張弘坤
10	04/20	08 · Power: Low Power Design	許毓倫
11	04/27	09 · System Verilog (Design)	彭志偉
12	05/04	10 · System Verilog II (Verification)	彭志偉
13	05/11	(Bonus) System Verilog (Formal Verification)	林文約
14	05/18	11 · APR I : From RTL to GDSII	張弘坤
15	05/25	12 · APR II : IR-Drop Analysis	許毓倫
16	06/01	Final Exam	Х
18	06/12	Final Project Deadline (2 nd demo @06/19, 3 rd demo @06/22)	

Grading Policy

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Total: 105%