ICLAB 2022-SPRING Midterm Project Pre-Released

Presenter: Wen-Yue, Lin

Advisor: Chen-Yi Lee

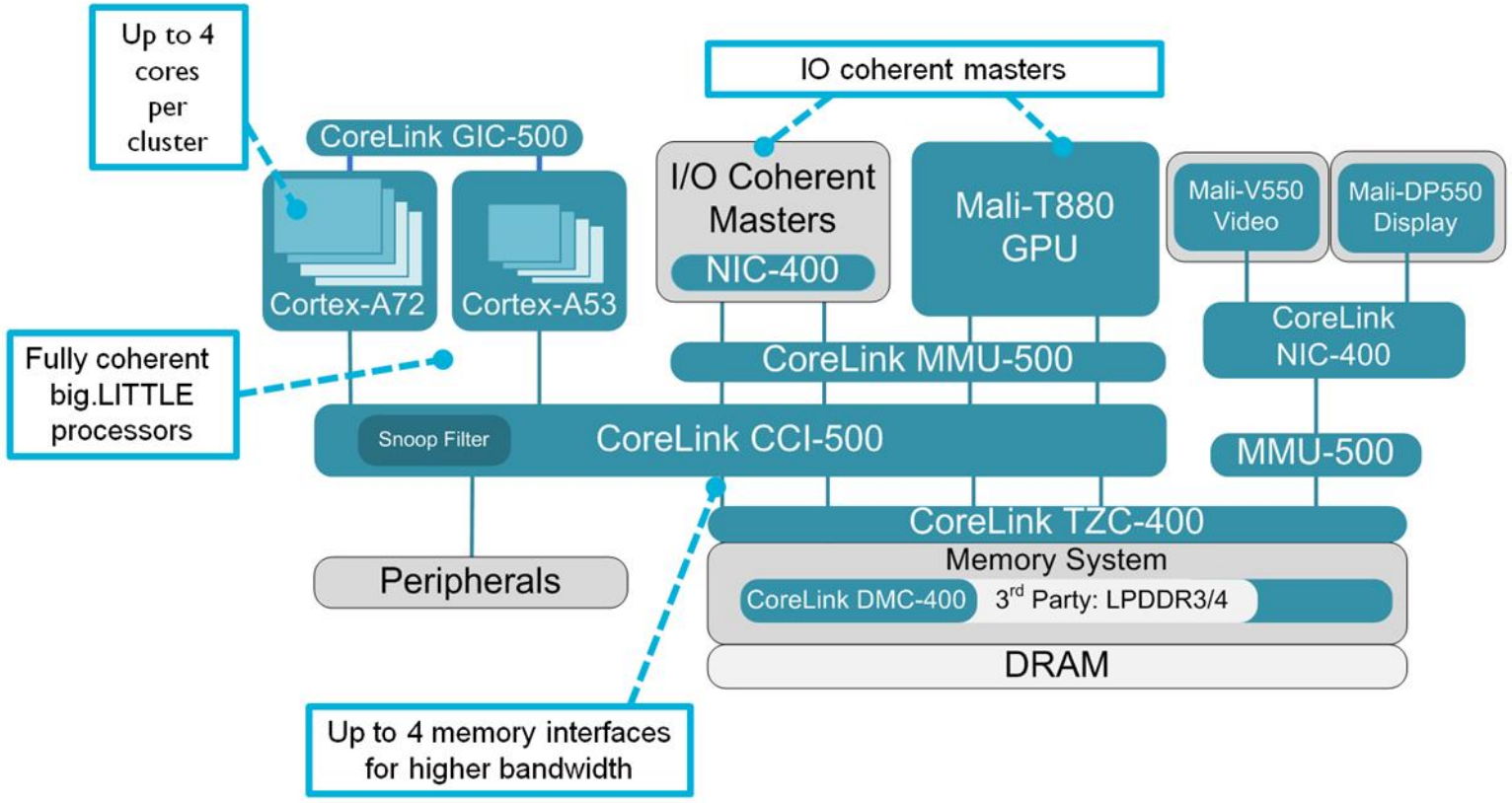
Outline

- **AMBA Brief History**
- **AXI 4 Introduction**
  - Handshake Process
  - AXI Signal Description in Midterm Project

AMBA Brief History

AMBA (Advanced Microcontroller Bus Architecture)

What is Bus Architecture ?



What is Bus Architecture ?

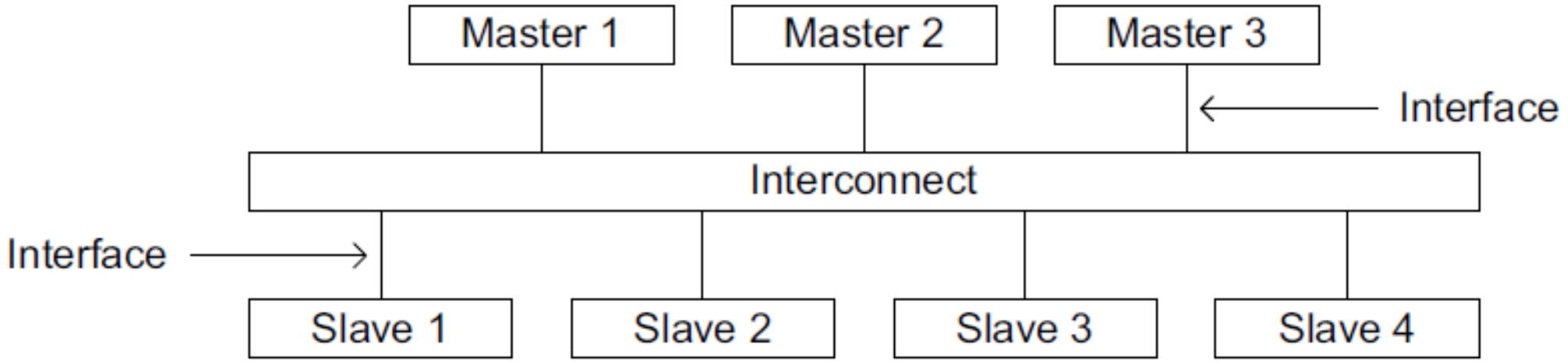
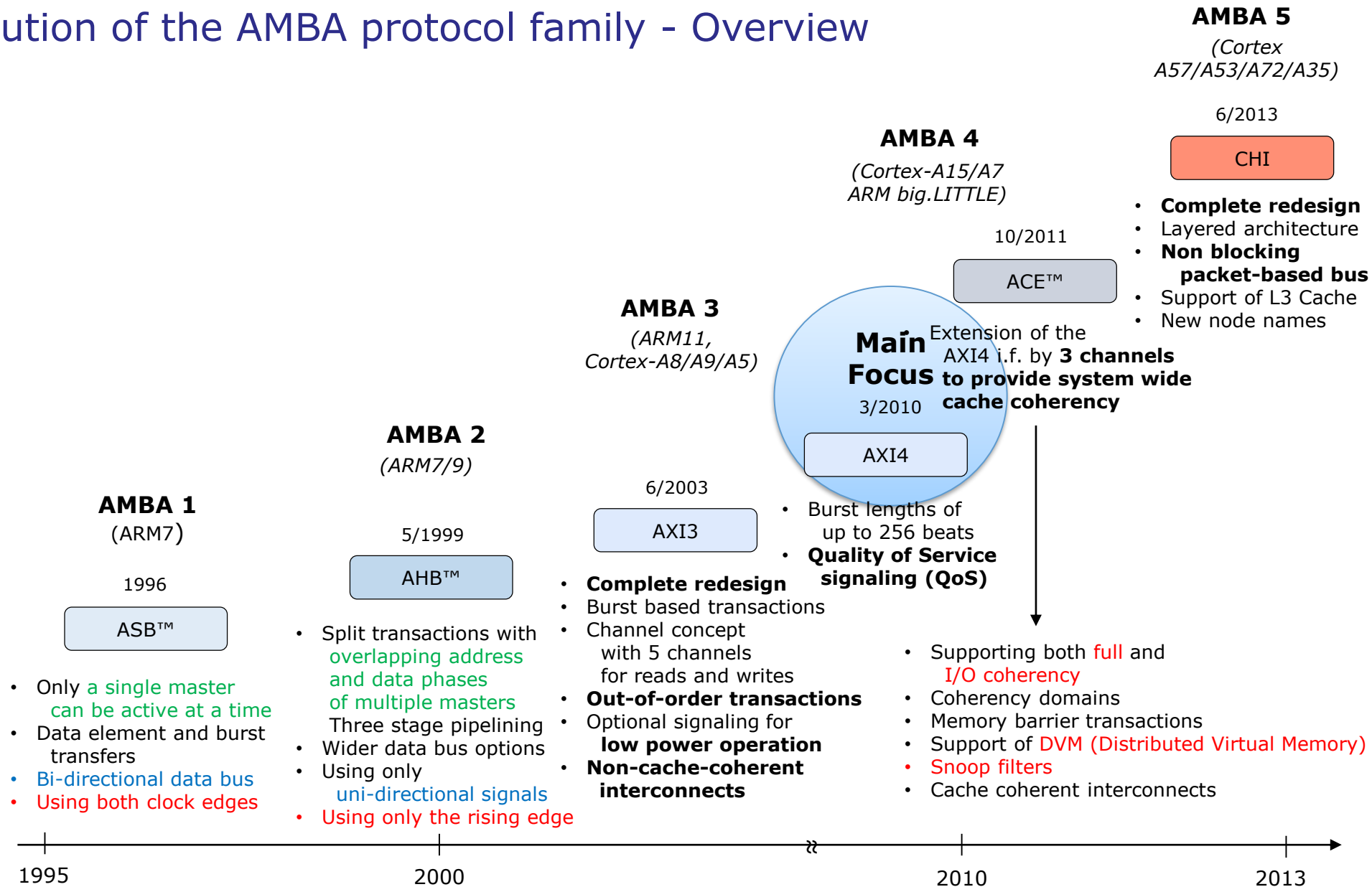


Figure A1-3 Interface and interconnect

AMBA

Evolution of the AMBA protocol family - Overview



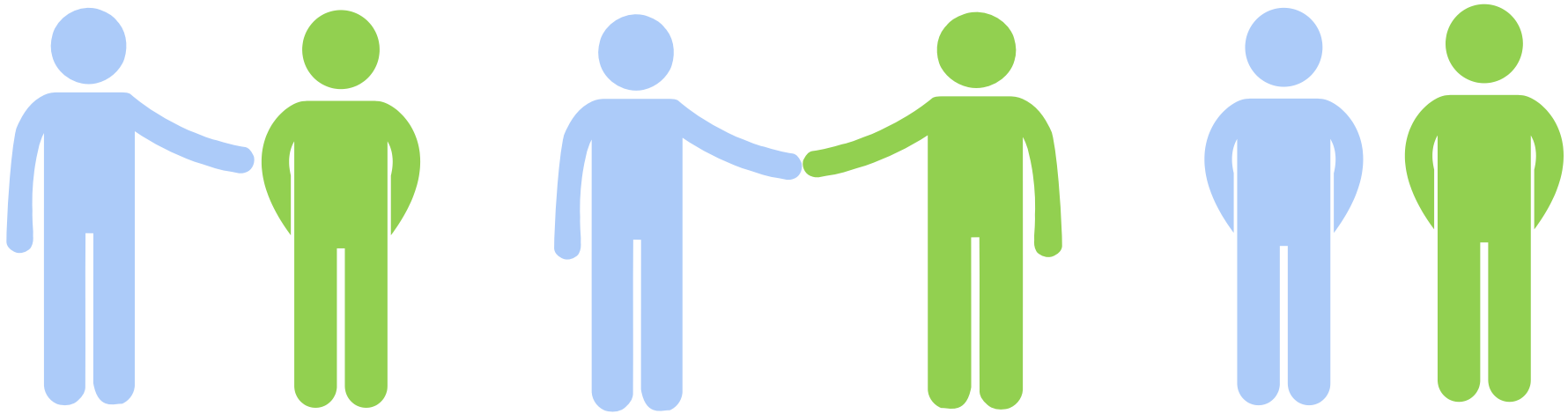
Ref [1]

AXI 4 Introduction

Handshake Process

Handshake Process Scenario 1

- **Slave: Valid** **Master: Ready**



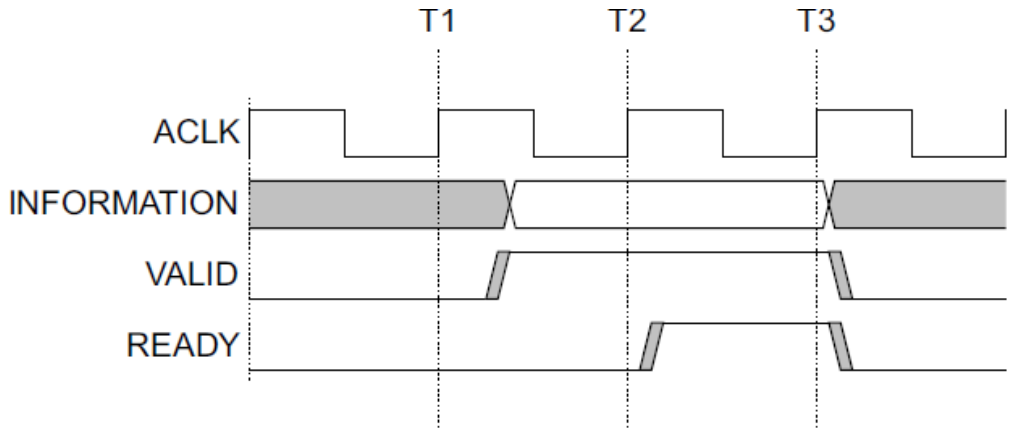
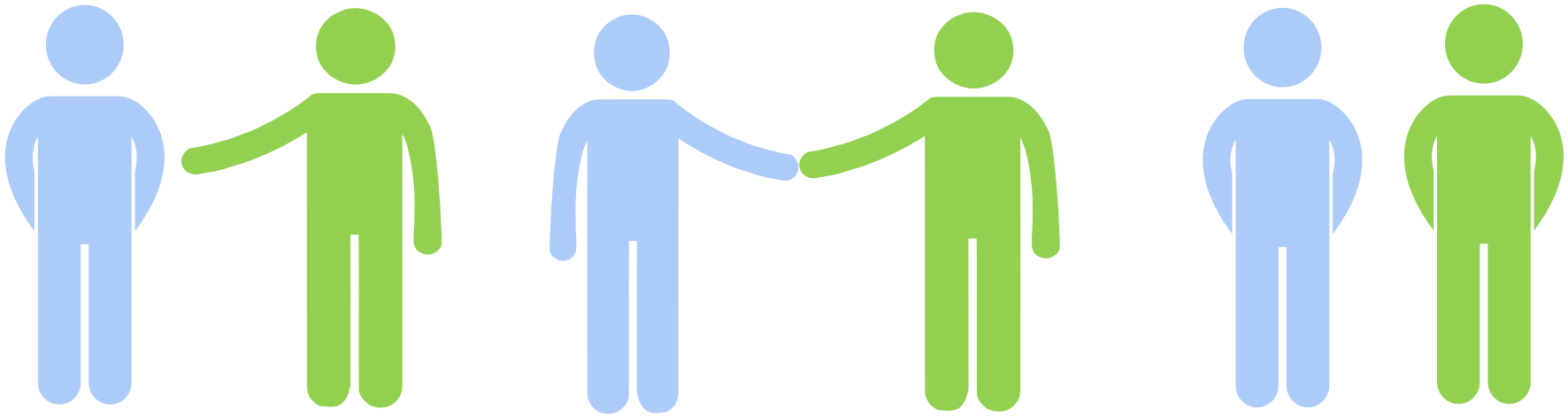


Figure A3-2 VALID before READY handshake

Handshake Process Scenario 2

- **Slave: Valid** **Master: Ready**



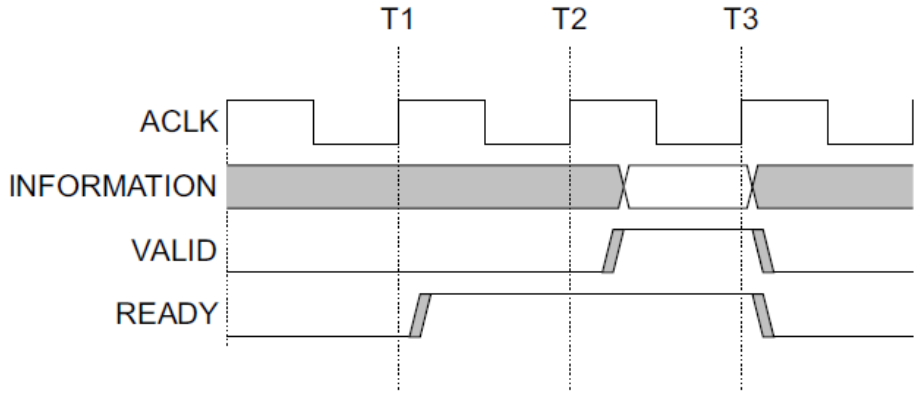
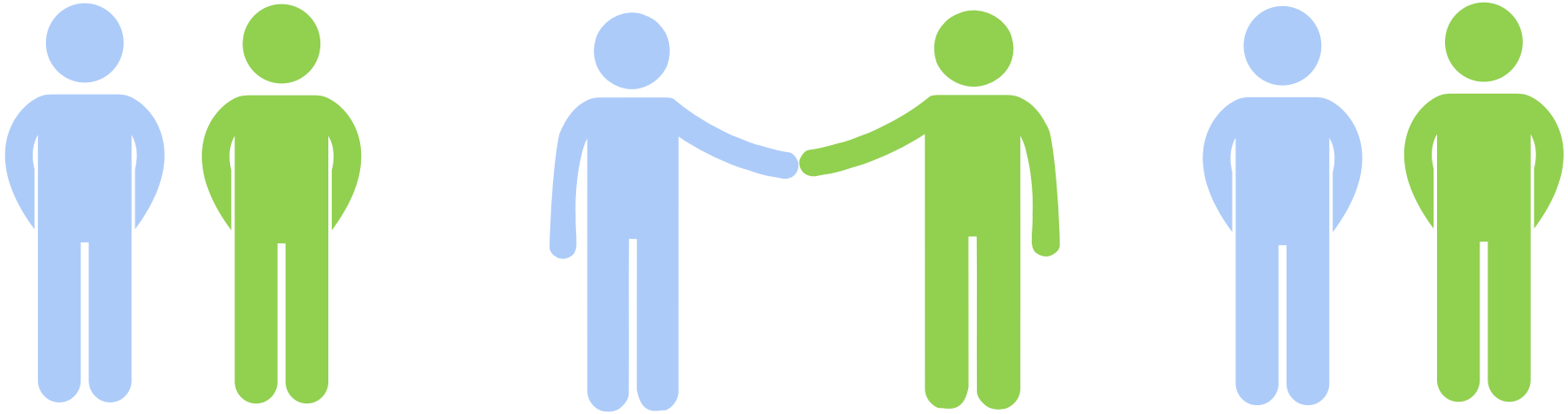


Figure A3-3 READY before VALID handshake

Handshake Process Scenario 3

- **Slave: Valid** **Master: Ready**



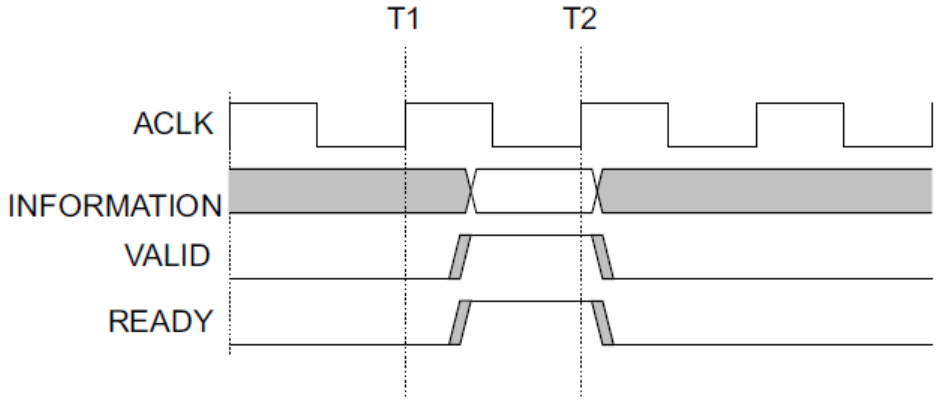


Figure A3-4 VALID with READY handshake

Handshake Process

- the VALID signal of one AXI component must not be dependent on the READY signal of the other component in the transaction.
- the READY signal can wait for assertion of the VALID signal.

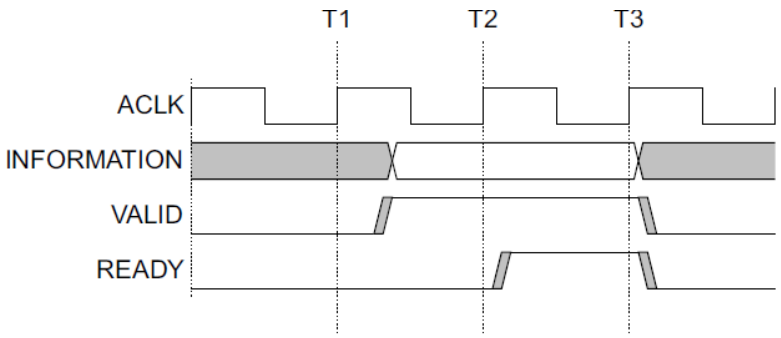


Figure A3-2 VALID before READY handshake

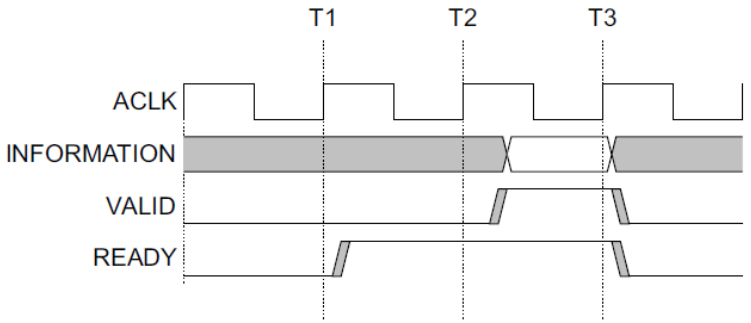


Figure A3-3 READY before VALID handshake

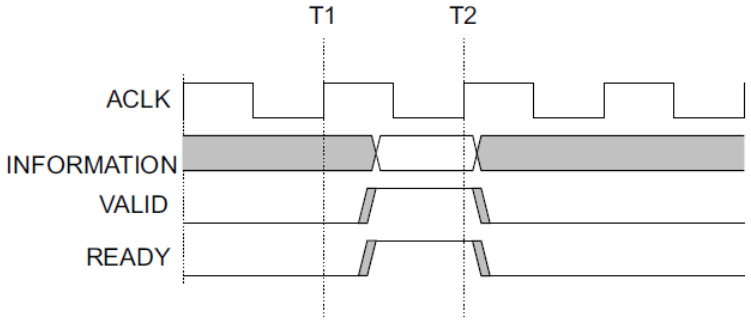


Figure A3-4 VALID with READY handshake

AXI 4 Introduction

AXI Signal Description(in this project)

AXI 4 Basic Transaction

Read Transaction

- Read Address Channel
- Read Data Channel

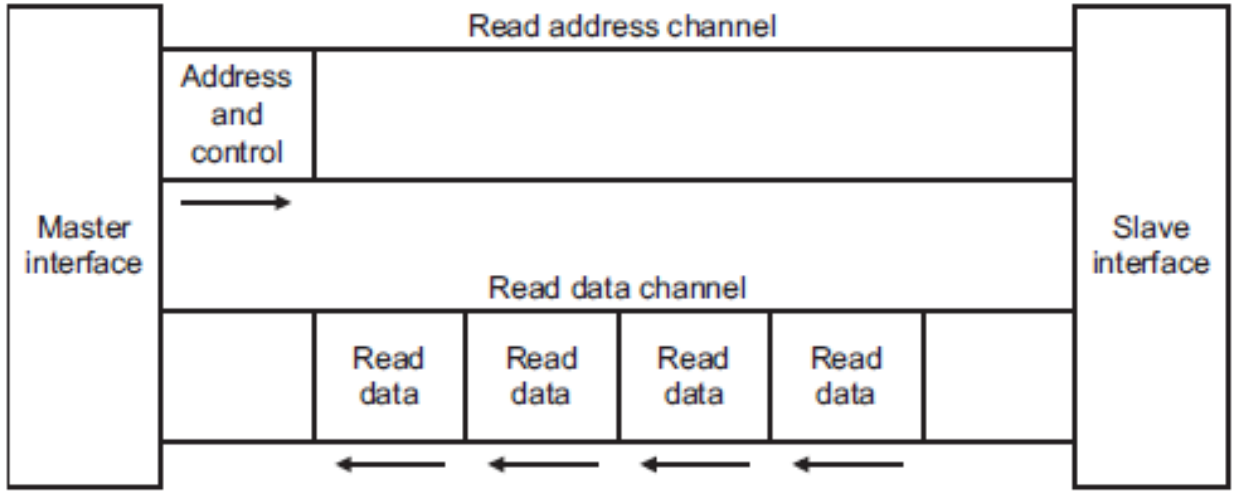


Figure 1-1 Channel architecture of reads

Each channel have valid-ready pair for handshaking process

Ref [2]

AXI 4 Basic Transaction

Write Transaction

- Write Address Channel
- Write Data Channel
- Write Response Channel

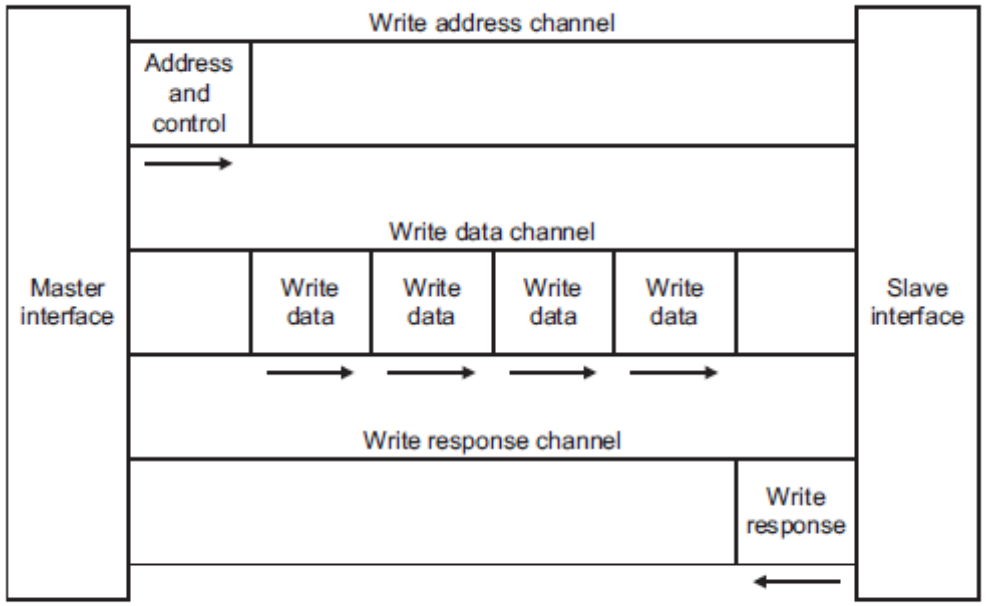


Figure 1-2 Channel architecture of writes

Each channel have valid-ready pair for handshaking process

Ref [2]

Global Signals

Signal	Source	Description
clk	Clock source	Global clock signal. All signals are sampled on the rising edge of the global clock.
rst_n	Reset source	Global reset signal. This signal is active LOW.

Write Address Channel

Signal	Source	Description
AWID[3:0]	Master	Write address ID. This signal is the identification tag for the write address group of signals. (In this project, we only use this to recognize master, reordering method is not supported)
AWADDR[31:0]	Master	Write address. The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
AWLEN[7:0]	Master	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
AWSIZE[2:0]	Master	Burst size. This signal indicates the size of each transfer in the burst. (In this project, we only support 3'b100 which is 16 Bytes (matched with Data Bus-width) in each transfer)
AWBURST[1:0]	Master	Burst type. The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated. (only INCR(2'b01) is supported in this Project)
AWVALID	Master	Write address valid. This signal indicates that valid write address and control information are available: 1 = address and control information available 0 = address and control information not available. The address and control information remain stable until the address acknowledge signal, AWREADY, goes HIGH.
AWREADY	Slave	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals: 1 = slave ready 0 = slave not ready.

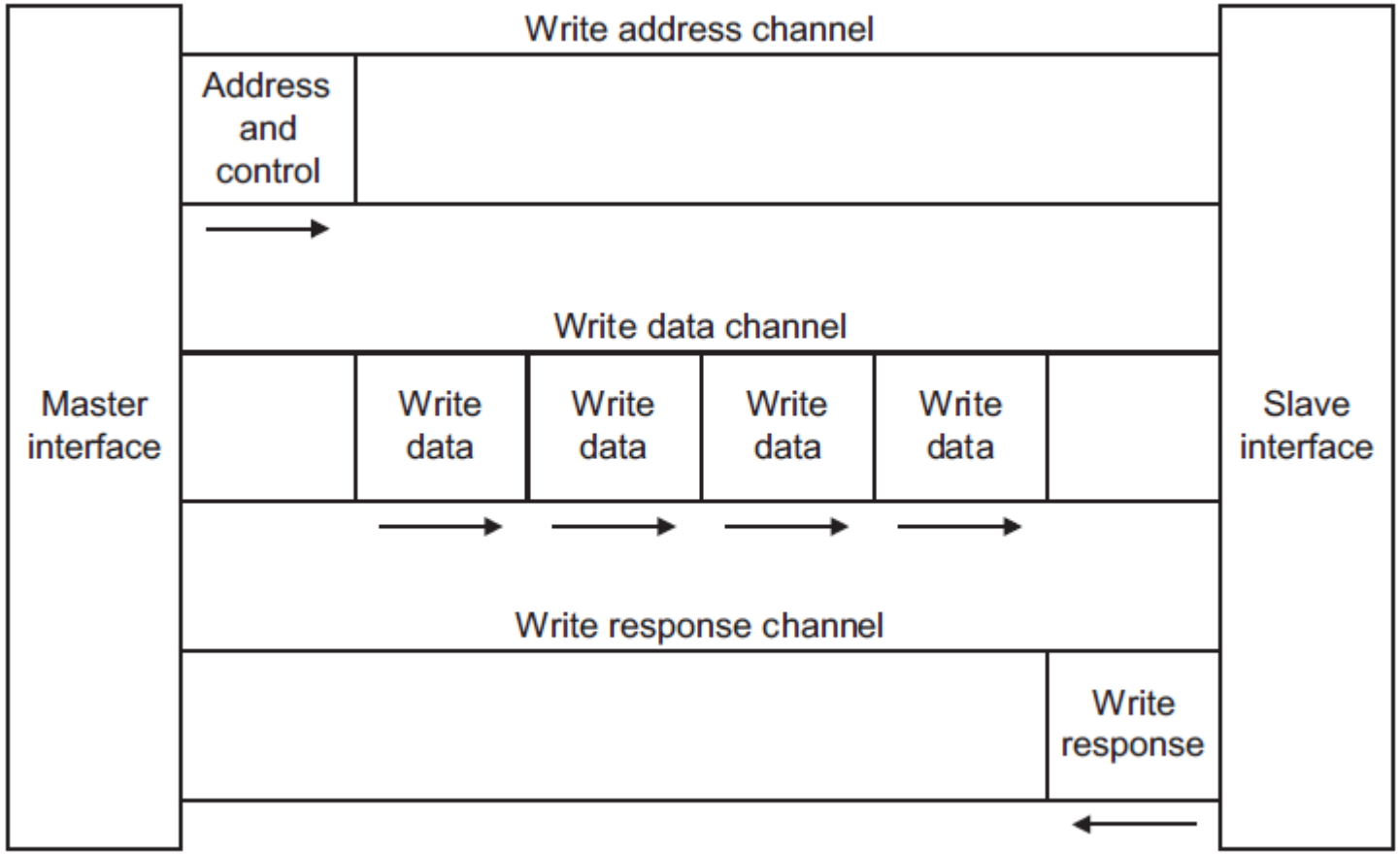
Write Data Channel

Signal	Source	Description
WDATA	Master	Write data. The write data bus can be 8, 16, 32, 64, 128, 256, 512, or 1024 bits wide. (In this project, we only support 128 bit data width: WDATA[127:0])
WLAST	Master	Write last. This signal indicates the last transfer in a write burst.
WVALID	Master	Write valid. This signal indicates that valid write data and strobes are available: 1 = write data and strobes available 0 = write data and strobes not available.
WREADY	Slave	Write ready. This signal indicates that the slave can accept the write data: 1 = slave ready 0 = slave not ready.

Write Response Channel

Signal	Source	Description
BID[3:0]	Slave	Response ID. The identification tag of the write response. The BID value must match the AWID value of the write transaction to which the slave is responding.
BRESP[1:0]	Slave	Write response. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR. (only OKAY(2'b00) is supported in this Project)
BVALID	Slave	Write response valid. This signal indicates that a valid write response is available: 1 = write response available 0 = write response not available.
BREADY	Master	Response ready. This signal indicates that the master can accept the response information. 1 = master ready 0 = master not ready.

Write Transaction



Waveform of Write Transaction

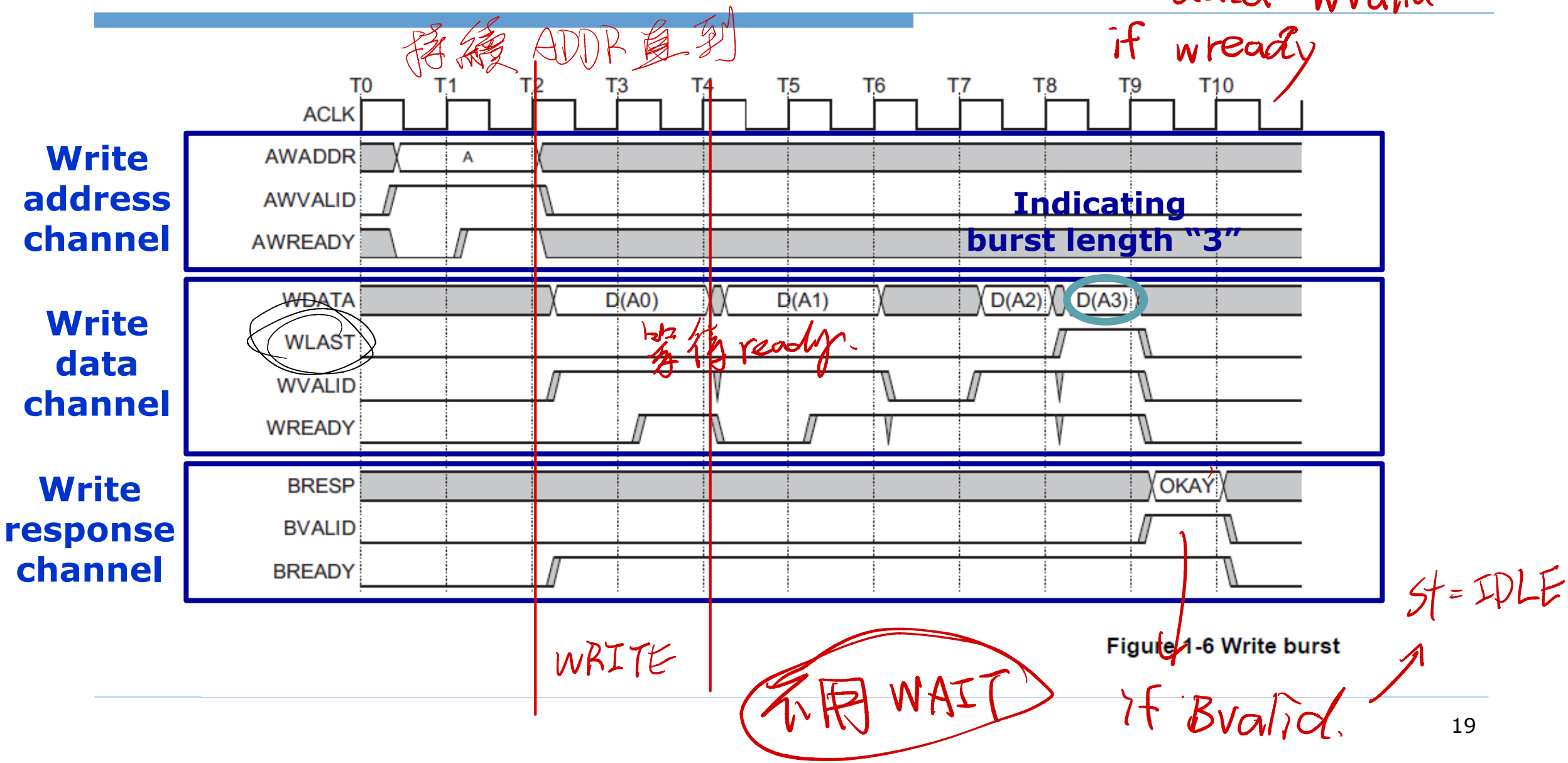


Figure 1-6 Write burst

Read Address Channel

Signal	Source	Description
ARID[3:0]	Master	Read address ID. This signal is the identification tag for the read address group of signals. (In this project, we only use this to recognize master, reordering method is not supported)
ARADDR[31:0]	Master	Read address. The read address bus gives the initial address of a read burst transaction.
ARLEN[7:0]	Master	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
ARSIZE[2:0]	Master	Burst size. This signal indicates the size of each transfer in the burst. (In this project, we only support 3'b100 which is 16 Bytes (matched with Data Bus-width) in each transfer)
ARBURST[1:0]	Master	Burst type. The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated. (only INCR(2'b01) is supported in this Project)
ARVALID	Master	Read address valid. This signal indicates, when HIGH, that the read address and control information is valid and will remain stable until the address acknowledge signal, ARREADY, is high. 1 = address and control information valid 0 = address and control information not valid.
ARREADY	Slave	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals: 1 = slave ready 0 = slave not ready.

Read Data Channel

Signal	Source	Description
RID[3:0]	Slave	Read ID tag. This signal is the ID tag of the read data group of signals. The RID value is generated by the slave and must match the ARID value of the read transaction to which it is responding.
RDATA[127:0]	Slave	Read data. The read data bus can be 8, 16, 32, 64, 128, 256, 512, or 1024 bits wide. (In this project, we only support 128 bit data width: RDATA[127:0])
RRESP[1:0]	Slave	Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR. (only OKAY(2'b00) is supported in this Project)
RLAST	Slave	Read last. This signal indicates the last transfer in a read burst.
RVALID	Slave	Read valid. This signal indicates that the required read data is available and the read transfer can complete: 1 = read data available 0 = read data not available.
RREADY	Master	Read ready. This signal indicates that the master can accept the read data and response information: 1= master ready 0 = master not ready.

Read Transaction

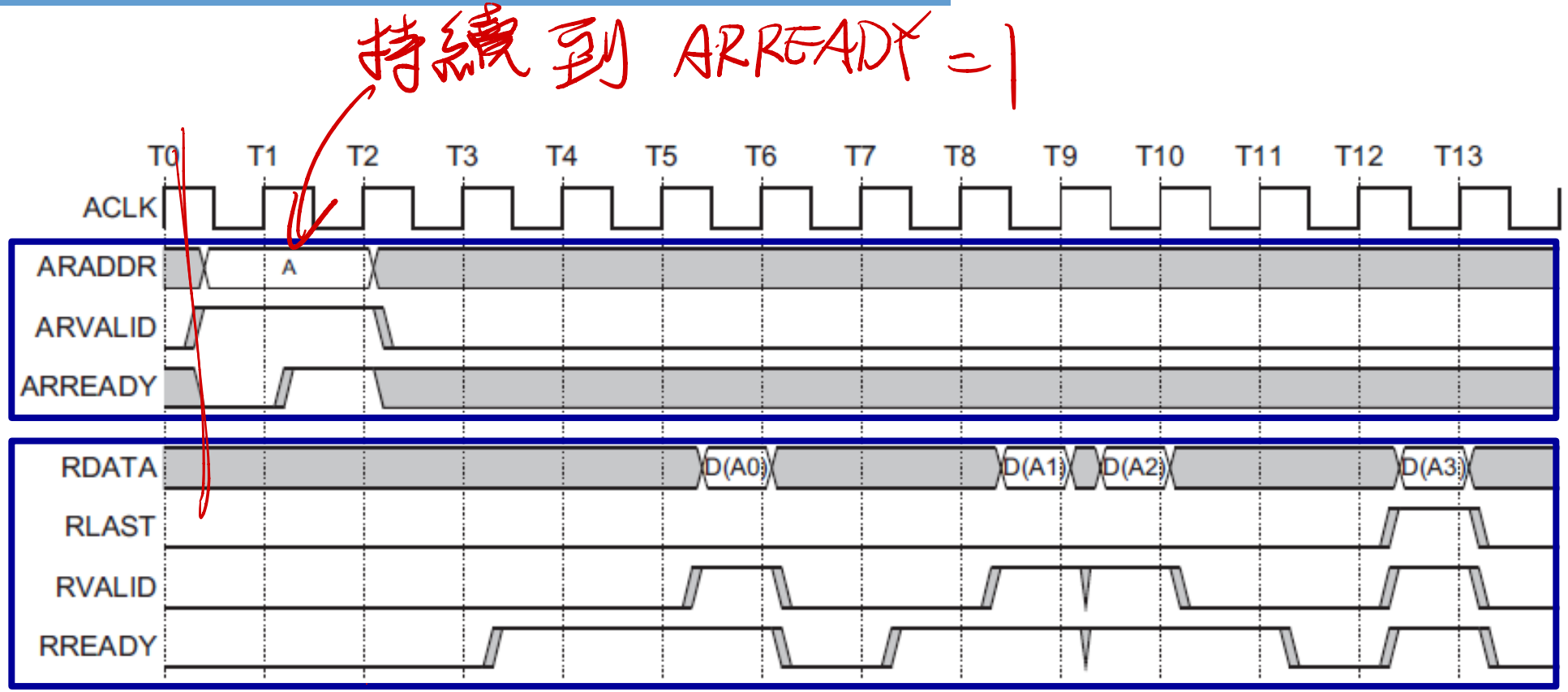
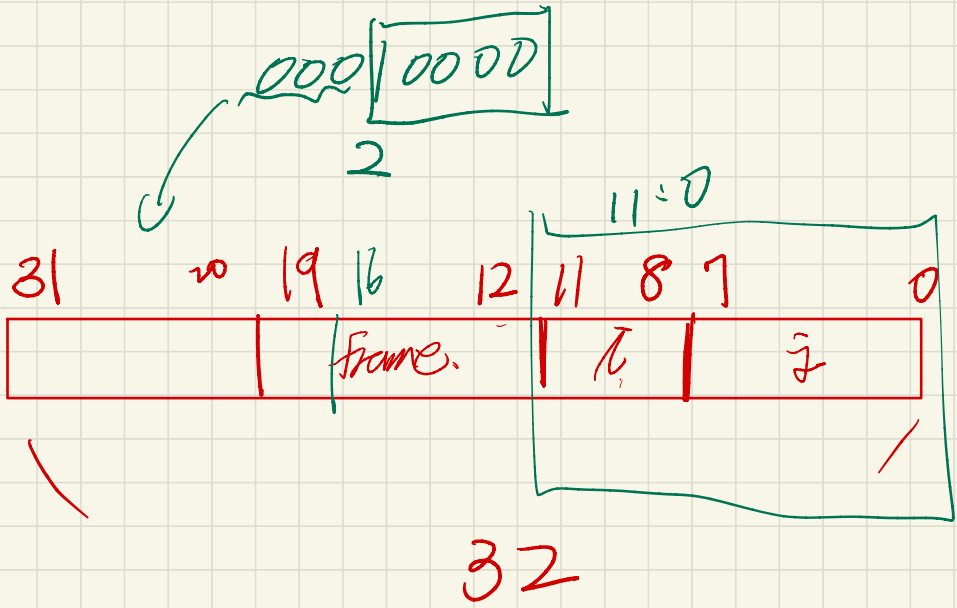


Figure 1-4 Read burst

Author

- 2019-Spring Will Liu (willvegapunk.ee03@g2.nctu.edu.tw)
- 2019-Fall Yun-Sheng Chan (yschan.ee03g@g2.nctu.edu.tw)
- 2021-Spring Hsi Hao Huang (hung6466@gmail.com)
- 2022-Spring Wen-Yue, Lin (kenlin.ee09@nycu.edu.tw)



0x00010000-0x000100FE: Histogram
0x000100FF: Distant for that pixel
0x00010?XX: 16 Histograms form 1 frame
0x0001?XXX: 16 Frames
0x0002?XXX: another 16 Frames

19 : 12