NCTU-EE IC LAB – Spring 2022

Lab12 Exercise

Design: Digit matching machine APRII

Data Preparation

1. Extract test data from TA's directory:

   % tar xvf ~iclabta01/Lab12.tar

2. The extracted LAB directory contains:

   a. 00_TESTBED
   b. 01_RTL
   c. 02_SYN
   d. 03_GATE
   e. 04_MEM
   f. 05_APR
   g. 06_POST

Description

In this lab you will finish the **backend flow (APR)** for this design and use the **IR drop and Power Analysis** tool for your layout.

Inputs and Outputs

Input Signals	Bit Width	Definition
clk	1	Clock.
rst_n	1	Asynchronous active-low reset.
in_valid	1	High when input signals are valid.
keyboard	5	The digit basis.
answer	5	The correct answer.
weight	4	The weight set for each digit position.
match_target	3	The matching requirement.

Output Signals	Bit Width	Definition
out_valid	1	High when output is valid.
result	5	Output the result 5-digit combination.
out_value	11	Output the corresponding maximum weighted score.

Layout Specifications

1. CHIP.sdc (provided by TA) period is fixed to 8ns input/output delay is fixed to 4ns
2. Core power pad and io power pad
   a. At least one pair at each side.
3. Floorplanning
   a. Core size:
      ✓ Defined by you
   b. Core to IO boundary:
      ✓ Each side must larger than 100
4. Power Planning
   a. Core Ring
      ✓ Top & Bottom: metal layer must be odd and width is fixed to 9.
      ✓ Left & Right: metal layer must be even and width is fixed to 9.
      ✓ Each side must be wire group, interleaving, and at least 4 pairs.
   b. Stripes
      ✓ Vertical: metal layer must be even and width is defined by you.
      ✓ Horizontal: metal layer must be odd and width is defined by you.
      ✓ Number of pairs is defined by you
   c. Timing Analysis
      ✓ Timing Slack:
        NO negative slacks after setup/hold time analysis
        (Post-Route stage)
      ✓ Design Rule Violation (DRV)
        The DRV of (fanout, cap, tran) should be all 0 after setup/hold time analysis
   d. Design Verification Result
      ✓ LVS : No LVS violations after "verify connectivity"
      ✓ DRC : No DRC violations after "verify geometry"
      ✓ Note: Remember to check DRC / LVS again after placing the fillers.
      Although in normal cases, if DRC and LVS are verified after nanoRoute, no more DRC / LVS will be produced during postRoute optimization and adding core filler. However some special cases produce the further DRC and LVS. For example: inserting a filler that is isolated from all other cells and power lines, then open LVS occurs. Thus, be sure to verify all the specs above after performing all APR steps.
   e. Rail Analysis:
      ✓ VDD Threshold set to 1.7
      ✓ GND Threshold set to 0.1
      ✓ No IR drop is allowed larger than 5mV

Note

1. Complete CHIP.io and CHIP_SHELL.v
2. Do all the flow as in APRI (Lab11) with Layout Specification above
3. Run Power Analysis (Setup & Run)
4. Run Rail Analysis
   - Set PG Library Mode
   - Generate PG Library
   - Setup Rail Analysis
   - Run Rail Analysis
5. Observe the IR Drop to analyze whether IR drop is within 5mV.
6. Please upload the following file on e3 platform before (2022/5/30 Mon 23:59)
   - CHIP_APR2_iclab???.tar:
     Please follow the following steps to put all required files in one folder named

CHIP_APR2_iclab???/ and compress the folder as CHIP_APR2_iclab???.tar:

1) In Exercise/05_APR folder, create a folder named CHIP_APR2_iclab???

```
linux01[Exercise/05_APR]% mkdir CHIP_APR2_iclab???
```

2) Copy the following files/directories into the folder:
   i. CHIP.inn

```
linux01[Exercise/05_APR]% cp CHIP.inn ./CHIP_APR2_iclab???
```

   ii. CHIP.inn.dat (this one is a directory so remember to use -r)

```
linux01 [Exercise/05_APR]% cp -r CHIP.inn.dat ./CHIP_APR2_iclab???
```

   iii. CHIP_SHELL.v

```
linux01[Exercise/05_APR]% cp CHIP_SHELL.v ./CHIP_APR2_iclab???
```

   iv. CHIP.io

```
linux01 [Exercise/05_APR]% cp CHIP.io ./CHIP_APR2_iclab???
```

3) Compress the CHIP_APR2_iclab??? folder into the tar file CHIP_APR2_iclab???.tar

```
linux01[Exercise/05_APR]% tar cvf CHIP_APR2_iclab???.tar CHIP_APR2_iclab???
```

7. **If you don't follow the steps above to compress the folder or type the wrong names, you may cause some link problems in the file or failure when TA demonstrates your files, and your demo will fail!!!**

Grading Policy

- **You should meet all the Layout Specification and File Specification above, pass post simulation without any timing violation, and within tolerable IR drop to pass the demo.**
- **Post simulation correctness & Within Tolerable IR Drop: 100 points**
- **2de pass grade: 70 points**