NCTU-EE IC LAB – Spring2022

Lab11 Exercise

Design: Local Binary Pattern

Data Preparation

1. Extract test data from TA's directory:
   % tar –xvf ~iclabta01/Lab11.tar
2. The extracted LAB director contains:
   a. Exercise

Design Description

This lab will use a basic digital image process operation, local binary pattern, to enhance image, and you don't have to write the design just run the APR flow for LBP.

Specifications

1. Top module name : LBP
2. Asynchronous, active low reset
3. The clock period is 3.0ns for RTL to gate-sim, You can adjust your clock period by yourself.
4. Input delay is half of clock period except clock signal.
5. Output delay is 1ns at APR and post-sim.
6. The SRAM has been given, memory files are in 04_MEM

Input and Outputs

Input signal	Bit width	Definition
clk	1	Clock
rst_n	1	Asynchronous active-low reset
in_valid	1	High when input signals are valid
in_image	8	Input image.

Output signal	Bit width	Definition
out_valid	1	Should be set to low after reset and not be raise when in_valid is high. Should set to high when out_image is ready.
out_image	8	Output result.

Constraints of the design in APR flow

1. Floorplaning
   a. Core size
      Define by user
   b. Core to IO boundary
      Each side must be more than 100
   c. Hard Macro placement
      All hard macro should be in CORE

2. Power planning

a. Core Ring
   (i) Top & Bottom: metal layer must be odd (1,3,…) and width is 9.
   (ii) Left & Right: metal layer must be even (2,4,…) and width is 9.
   (iii) Each side must be wire group, interleaving, and at least 4 pairs.

b. Stripes
   (i) Vertical: metal layer must be even (2,4,…) and width is at least 2.
   (ii) Horizontal: metal layer is must be odd (1,3,…) and width is at least 2.
   (iii) The maximum distance between two stripes or the stripe and edge should be less than 200.

3. Timing analysis results
   a. Timing Slack
      NO negative slacks after setup/hold time analysis (include SI).
   b. Design Rule Violation (DRV)
      The DRV of (fanout, cap, tran) should be all 0 after post-Route setup/hold time analysis (including SI)

4. Design verification results
   a. Layout vs. Schematic (LVS)
      NO LVS violations after "verify Connectivity".
   b. Design Rule Check (DRC)
      NO DRC violations after "verify DRC".

Grading Policy

1. APR and Post Simulation Correctness (70%)
   a. Complete the APR flow and meet all the constraints above.
   b. Pass the post-layout gate-level simulation
2. Performance (30%)
   a. Core area * Clock_Period(@posim)
      *** (Latency is not counted) ***
   b. You will only get performance score with correct APR and Post Simulation Result

Note

1. Please upload an archive file on e3 platform before 23:59 on 5/29:
   (If you type the wrong name of the file, you will be treated as FAIL at this lab !!!!!)
   a. Naming rule: Lab11_iclabXXX.tar
   b. The archive file must include the following files:
      (1) cycle_iclabXXX.txt : record the clock period of your post-layout simulation (cycle time in 06_pattern)
      (2) CHIP_iclabXXX.sdc (Rename from the file "CHIP.sdc ")
      (3) CHIP_iclabXXX.io (Rename from the file "CHIP.io ")
      (4) CHIP_iclabXXX.v (Rename from the file "CHIP.v " , layout version)
      (5) CHIP_iclabXXX.sdf (Rename from file "CHIP.sdf ")
      (6) CHIP_iclabXXX.inn (Rename from the file "CHIP.inn ")
      (7) CHIP_iclabXXX.inn.dat.tar (Rename the file "CHIP.inn.dat" to "CHIP_iclabXXX.inn.dat" and compress the file)

(8) All this files should fill in the directory ” Lab11_iclabXXX/” ， and tar it to Lab11_iclabXXX.tar with the command ”tar cvf Lab11_iclabXXX.tar Lab11_iclabXXX/”. You must compress the file on Linux, and finish the check list. If any error occurs when restoring your design, you will FAIL the lab.

2. Template folders and reference commands:
   04_MEM/(don’t modify)
   05_APR/ (Automatic Place & Route Folder) ./00_combine
   06_POSTSIM/ (Post Layout Simulation) ./01_run
   (TA already wrote the PATTERN.v, you don’t need to write the PATTERN in this lab)

3. Don’t use any wire/reg/submodule/parameter name called *error*, *congratulation*, *latch* or *fail* otherwise you will fail the lab. Note: * means any char in front of or behind the word. e.g: error_note is forbidden.

4. Don’t write Chinese comments or other language comments in the file you turned in.