

## 3TB4 Lab 2 Report

Lin Fu ful10 400234794

Keyin Liang liangk10 400236736

1. We used 14 bits of XOR Fibonacci LFSR in our project that used 1, 3, 5, and 14 taps. We chose Fibonacci LFSR because it is relatively easy to implement in hardware and has a lower gate count compared to a Galois LFSR, which also has a shorter period. These taps are used because they are the positions of the most significant bit and other specific bits that have been determined to produce a maximal length pseudo-random sequence. By choosing these taps, the LFSR will generate a random sequence of 14 bits with a maximal period of  $2^{14} - 1$ , meaning it can generate all  $2^{14} - 1$  non-zero states before repeating. This is a good choice for generating a random number in a range of 1000 to 5000, as the sequence generated by the LFSR will be uniform and evenly distributed in this range.
2. Advantages of short LFSR:
  - Short LFSRs require fewer gates and less power consumption, making them more suitable for low-power applications or applications with limited hardware resources.
  - Due to their simplicity, short LFSRs may be simpler to implement and verify. Also, it takes a shorter time to generate.

Disadvantages of short LFSR:

- Sequences produced are more predictable and easier to guess. So that sometimes may not generate random numbers.

Advantages of long LFSR:

- They could create sequences that appear more random and are more difficult to anticipate, making them better suited for cryptographic applications.
- They are more suitable for applications that require longer sequences.

Disadvantages of long LFSR:

- Long LFSRs may need more gates and use more power and time, which makes them less appropriate for low-power applications with limited hardware resources.
- They could be trickier to develop and test, and hence more likely to have design problems.

3.

## Complication Report:

Quartus Prime Lite Edition - C:/Users/LinF/Documents/School/Winter2023/3TB4/TRON-3TB4-Winter-2023/lab2/lab2\_restored/lab2 - lab2

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

lab2.v

Compilation Report - lab2

Entity/Instance

- lab2
  - clock\_divider:comb\_40
  - counter:comb\_41
  - counter:comb\_42
  - random:comb\_43
  - blinkHEX:comb\_44
  - mux4to1:comb\_45
  - mux4to1:comb\_46
  - mux4to1:comb\_47
  - mux4to1:comb\_48
  - mux4to1:comb\_49
  - mux4to1:comb\_50
  - seven\_seg\_decoder:decoder0
  - seven\_seg\_decoder:decoder1
  - seven\_seg\_decoder:decoder2
  - seven\_seg\_decoder:decoder3
  - seven\_seg\_decoder:decoder4

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Setting
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Flow Messages
- Flow Suppressed Messages
- Assembler
- TimeQuest Timing Analyzer

Flow Summary

Flow Status: Successful - Mon Feb 20 00:03:57 2023

Quartus Prime Version: 17.1.0 Build 590 10...017 SJ Lite Edition

Revision Name: lab2

Top-level Entity Name: lab2

Family: Cyclone V

Device: 5CSEMA5F31C6

Timing Models: Final

Logic utilization (in ALMs): 373 / 32,070 ( 1 % )

Total registers: 156

Total pins: 57 / 457 ( 12 % )

Total virtual pins: 0

Total block memory bits: 0 / 4,065,280 ( 0 % )

Total DSP Blocks: 0 / 87 ( 0 % )

Total HSSI RX PCSs: 0

Total HSSI PMA RX Deserializers: 0

Total HSSI TX PCSs: 0

Total HSSI PMA TX Serializers: 0

Total PLLs: 0 / 6 ( 0 % )

Total DLLs: 0 / 4 ( 0 % )

Tasks

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programming)
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Edit Settings
- Program Device (Open Programmer)

Messages

System Processing (201)

Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 579 warnings

293000 Quartus Prime Full Compilation was successful. 0 errors, 1427 warnings

100% 00:01:19

Total number of logic elements used by your circuit: 373

Total number of registers: 156

Total number of pins: 57/457

The maximum number of logic elements that can fit on the FPGA that you used: 32070