3TB4 Lab 1 Report

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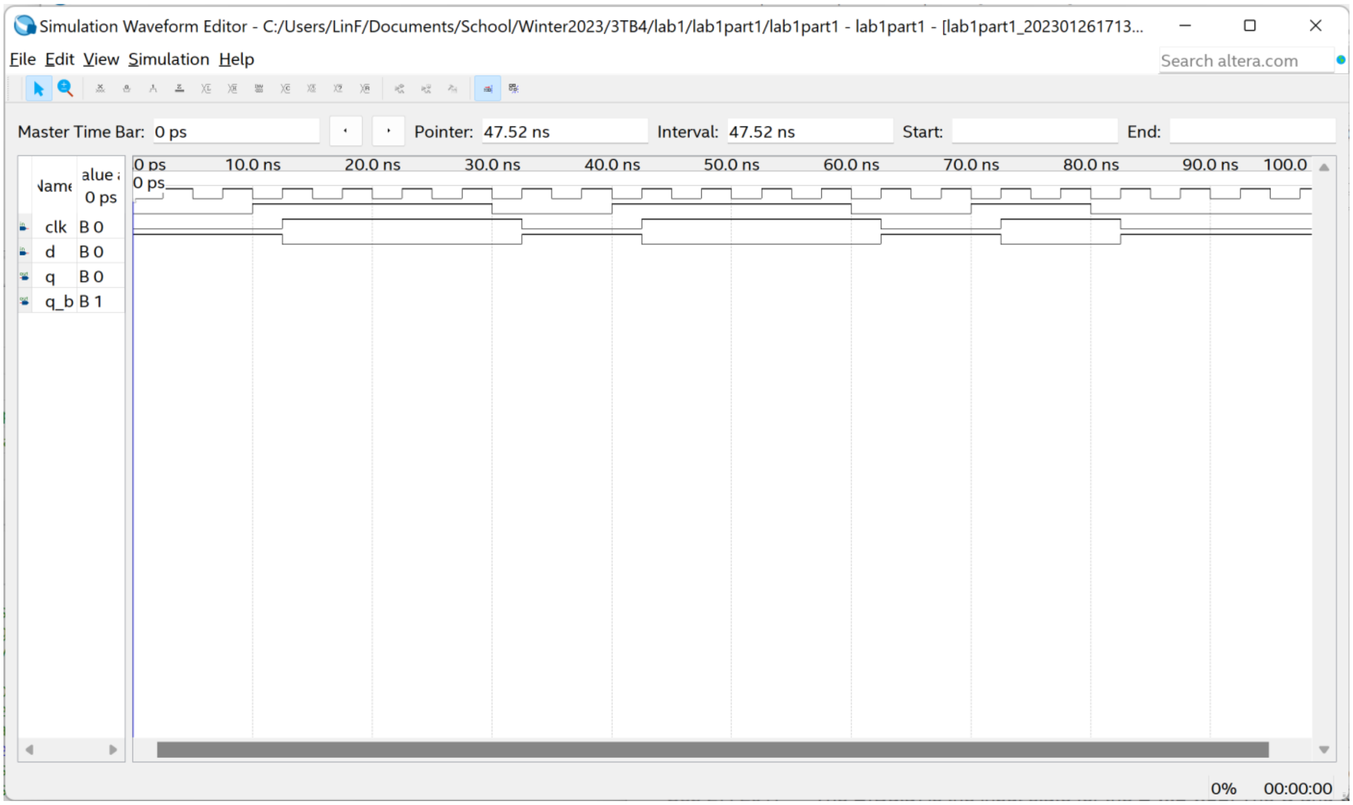
D flip-flop simulation:

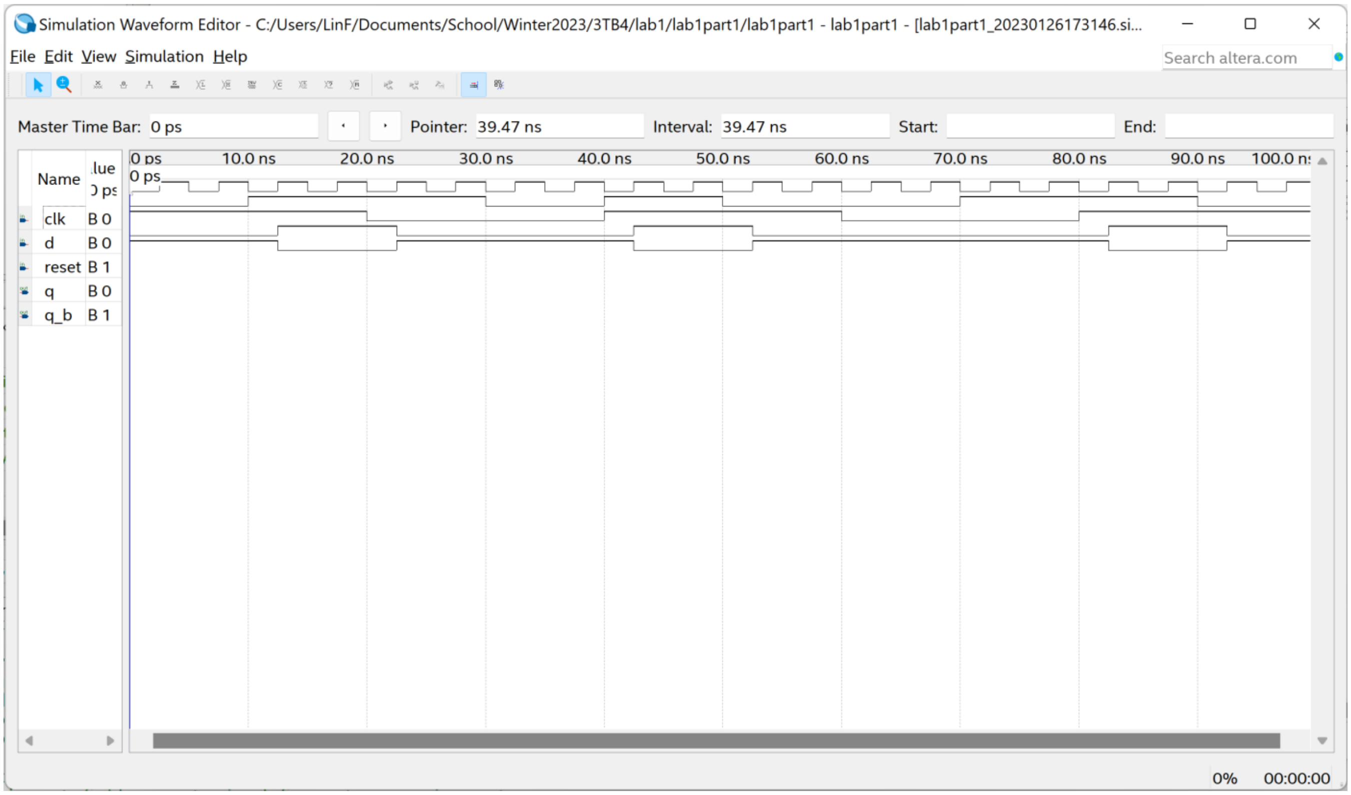


Simulation Waveform Editor - C:/Users/LinF/Documents/School/Winter2023/3TB4/lab1/lab1part1/lab1part1 - lab1part1 - [lab1part1_202301261713...

Master Time Bar: 0 ps Pointer: 47.52 ns Interval: 47.52 ns Start: End:

Name	Value at 0 ps
clk	B 0
d	B 0
q	B 0
q_b	B 1

D flipflop with active low synchronous reset:

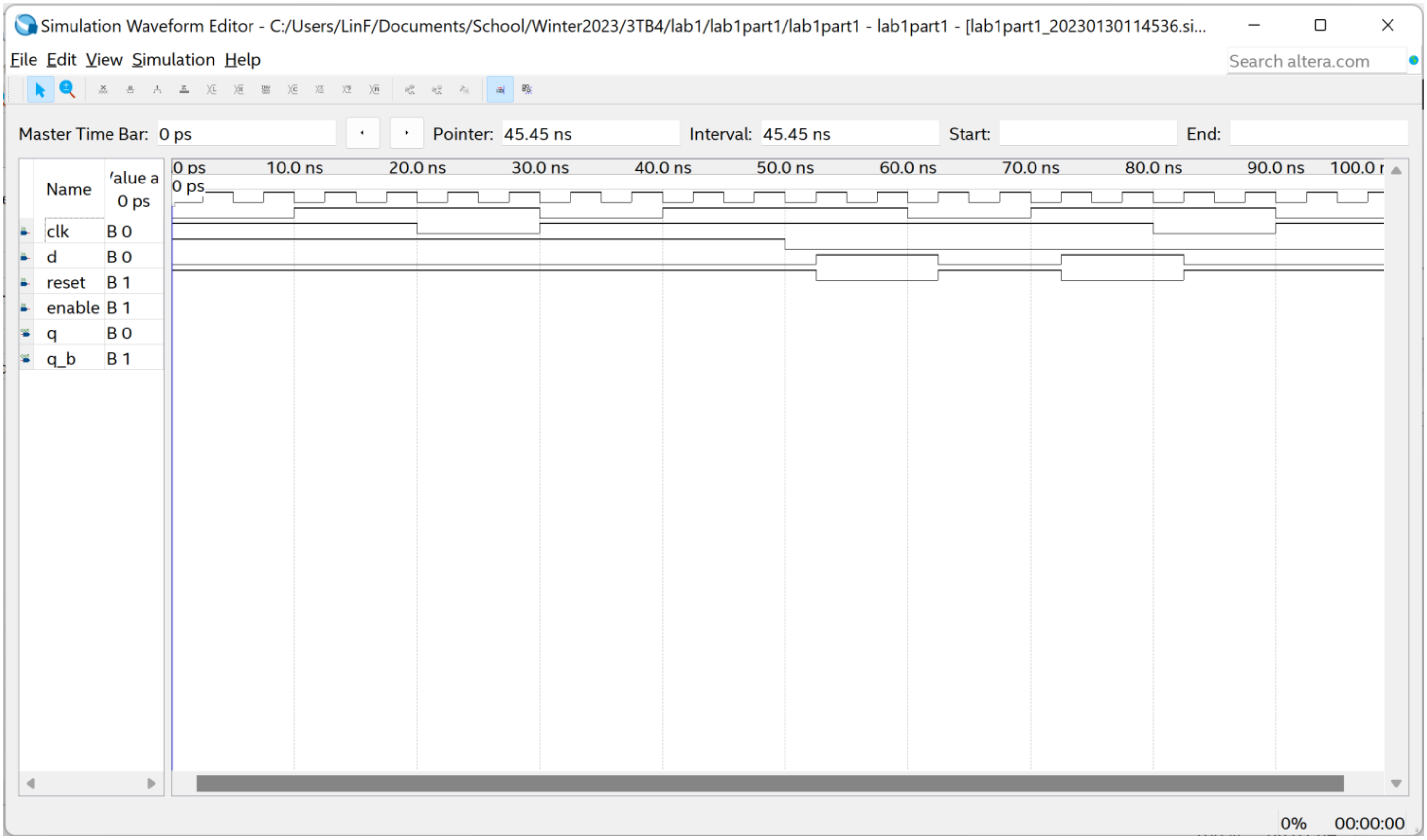


Simulation Waveform Editor - C:/Users/LinF/Documents/School/Winter2023/3TB4/lab1/lab1part1/lab1part1 - lab1part1 - [lab1part1_20230126173146.si...

Master Time Bar: 0 ps Pointer: 39.47 ns Interval: 39.47 ns Start: End:

Name	Value at 0 ps
clk	B 0
d	B 0
reset	B 1
q	B 0
q_b	B 1

D flipflop with active low synchronous reset and active low enable:



Simulation Waveform Editor - C:/Users/LinF/Documents/School/Winter2023/3TB4/lab1/lab1part1/lab1part1 - lab1part1 - [lab1part1_20230130114536.si...

Master Time Bar: 0 ps

Pointer: 45.45 ns

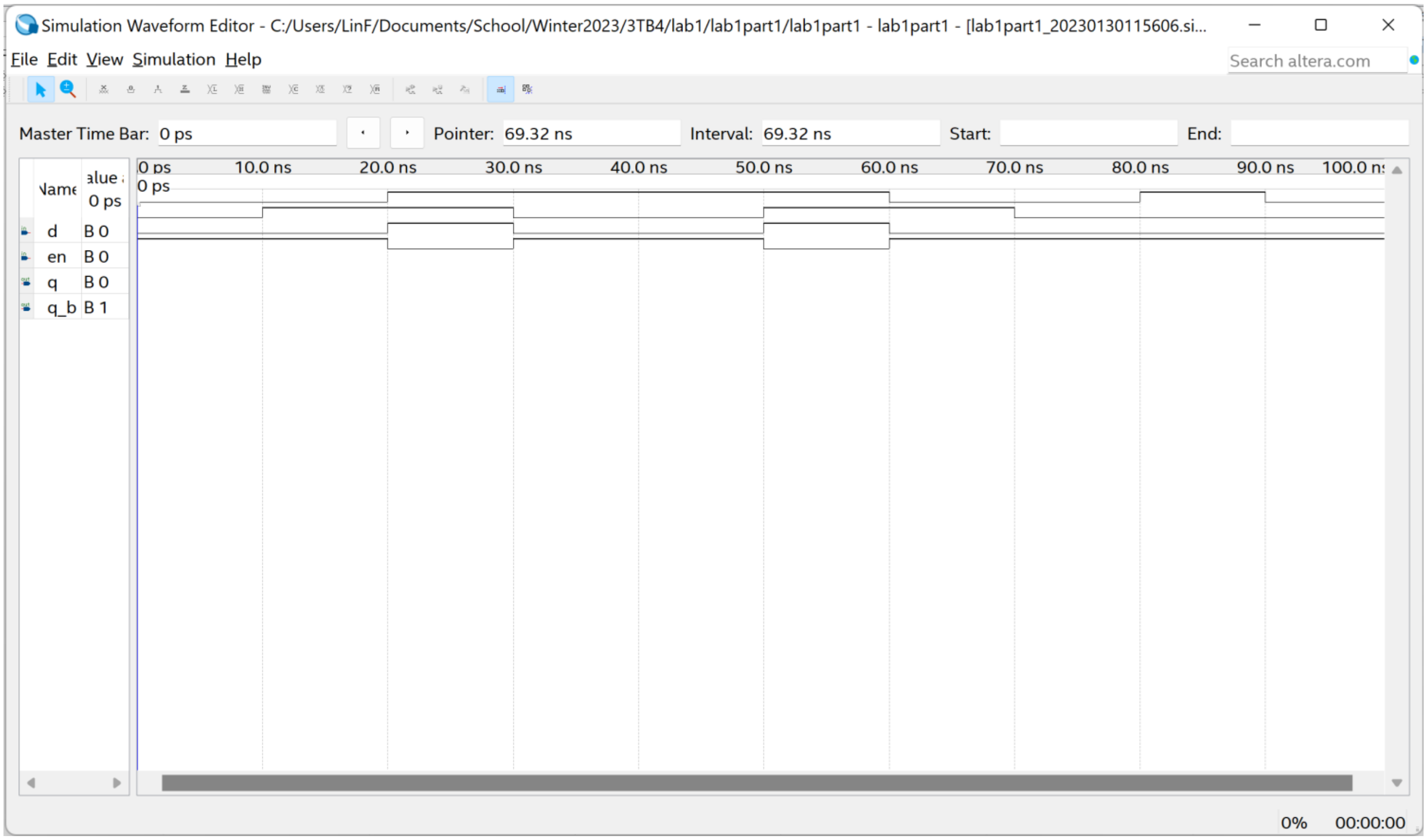
Interval: 45.45 ns

Start:

End:

Name	'alue a 0 ps
clk	B 0
d	B 0
reset	B 1
enable	B 1
q	B 0
q_b	B 1

D latch:



Simulation Waveform Editor - C:/Users/LinF/Documents/School/Winter2023/3TB4/lab1/lab1part1/lab1part1 - lab1part1 - [lab1part1_20230130115606.si...

Master Time Bar: 0 ps

Pointer: 69.32 ns

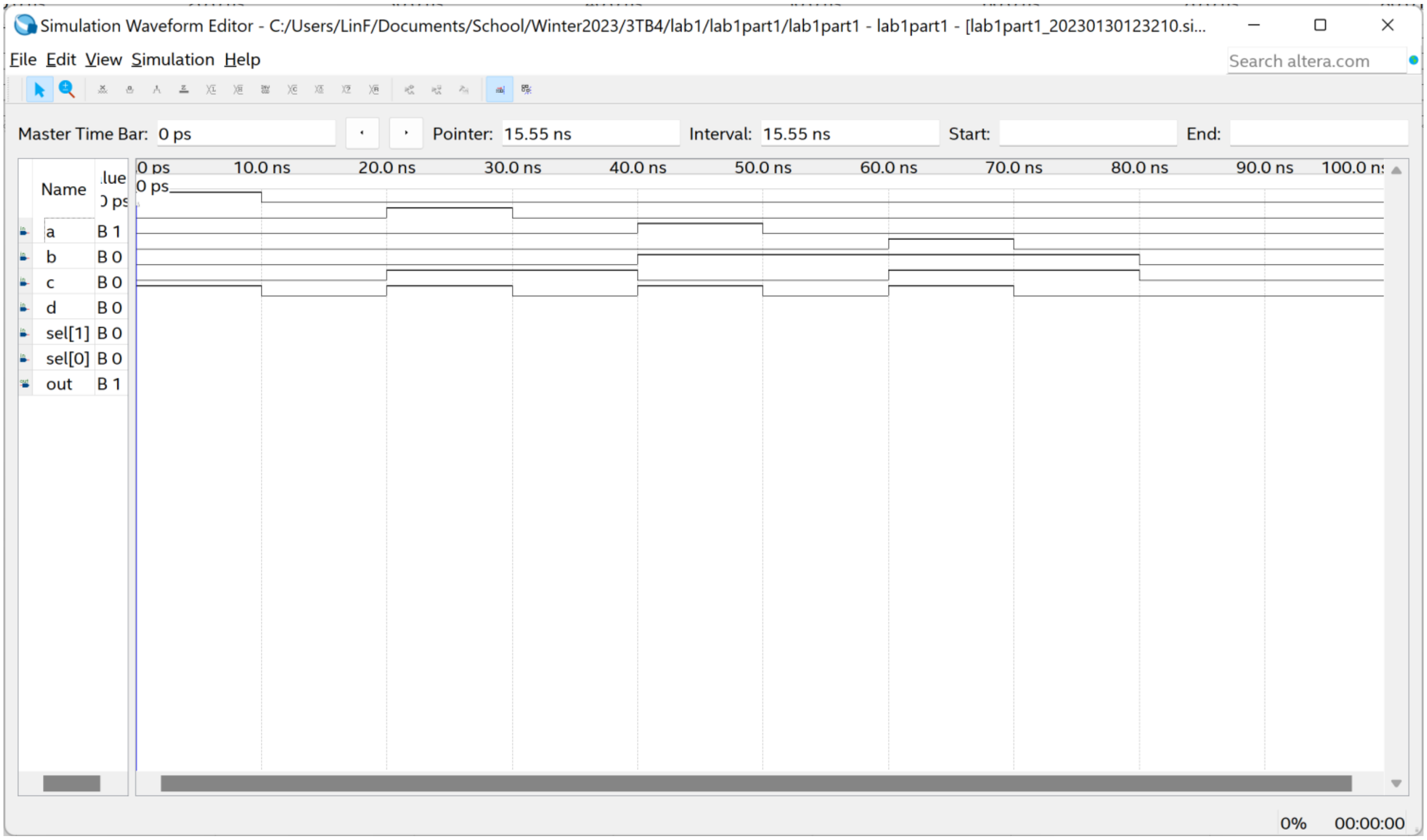
Interval: 69.32 ns

Start:

End:

Name	alue a 0 ps
d	B 0
en	B 0
q	B 0
q_b	B 1

Multiplexer:



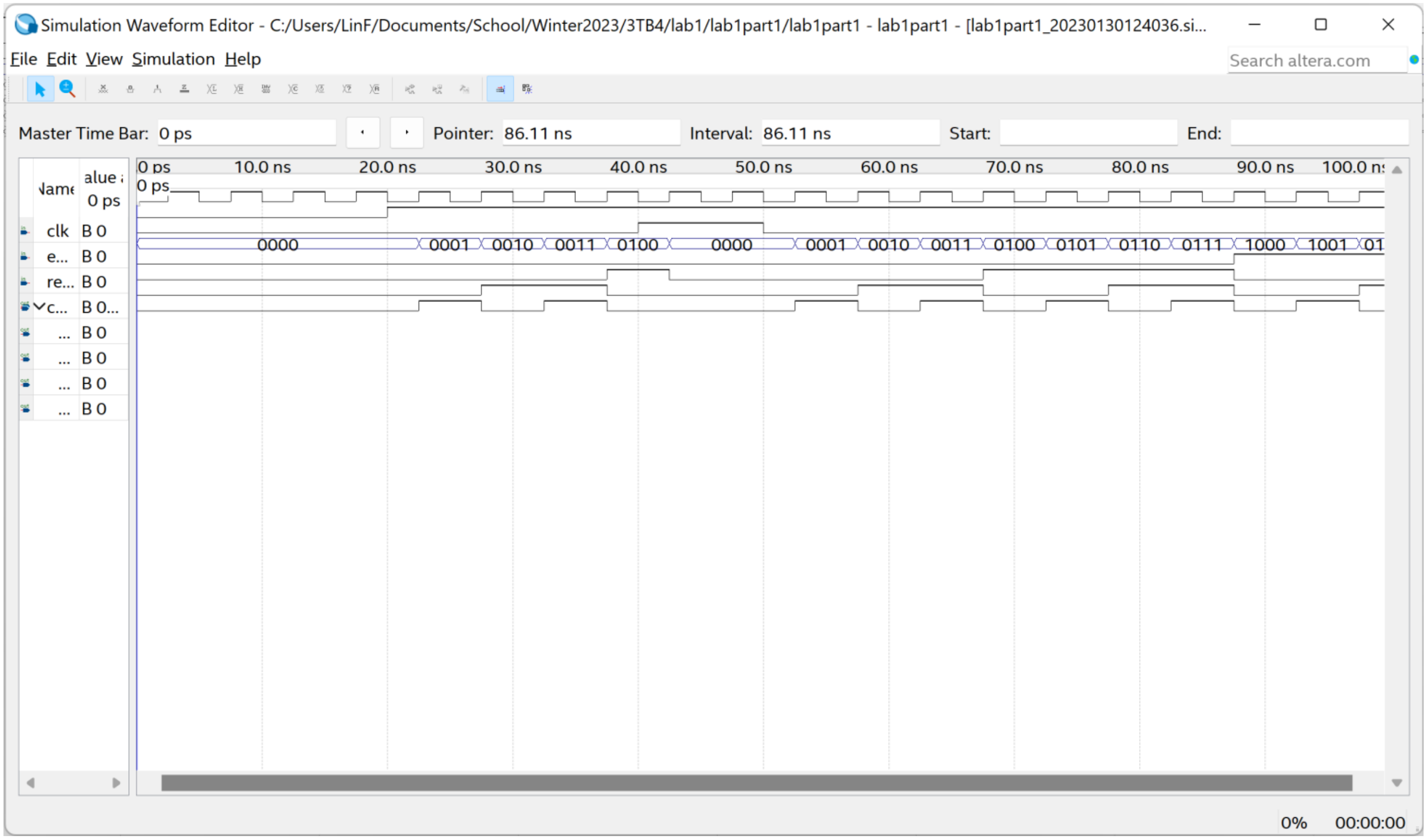
Simulation Waveform Editor - C:/Users/LinF/Documents/School/Winter2023/3TB4/lab1/lab1part1/lab1part1 - lab1part1 - [lab1part1_20230130123210.si...

Master Time Bar: 0 ps
Pointer: 15.55 ns
Interval: 15.55 ns
Start:
End:

Name	Value at 0 ps
a	B 1
b	B 0
c	B 0
d	B 0
sel[1]	B 0
sel[0]	B 0
out	B 1

0% 00:00:00

Counter:



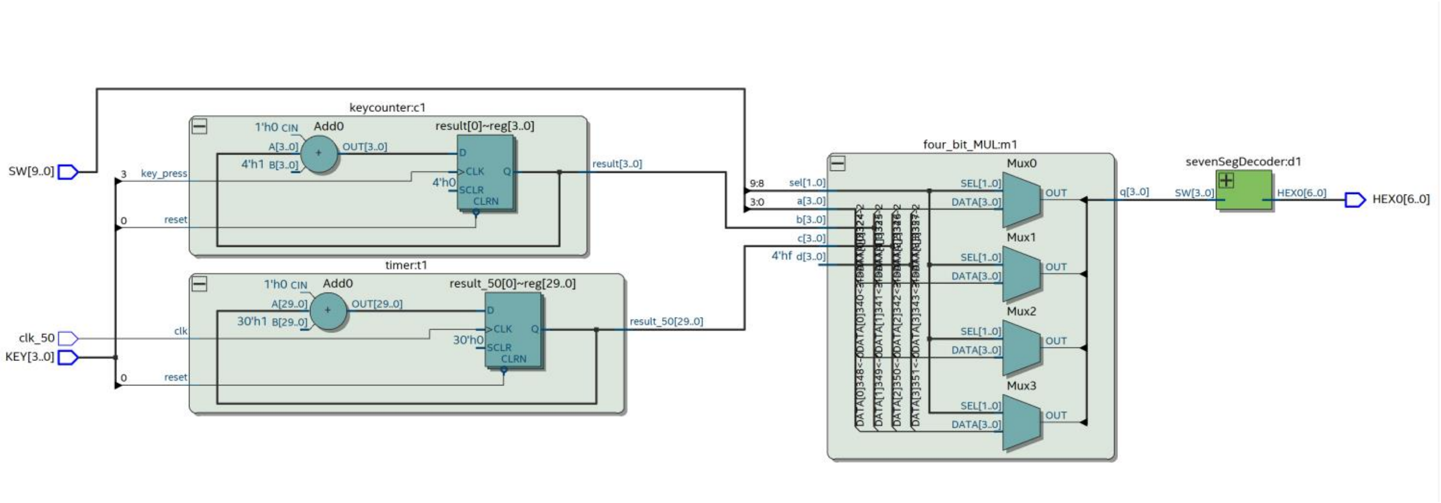
Simulation Waveform Editor - C:/Users/LinF/Documents/School/Winter2023/3TB4/lab1/lab1part1/lab1part1 - lab1part1 - [lab1part1_20230130124036.si...

Master Time Bar: 0 ps
Pointer: 86.11 ns
Interval: 86.11 ns
Start:
End:

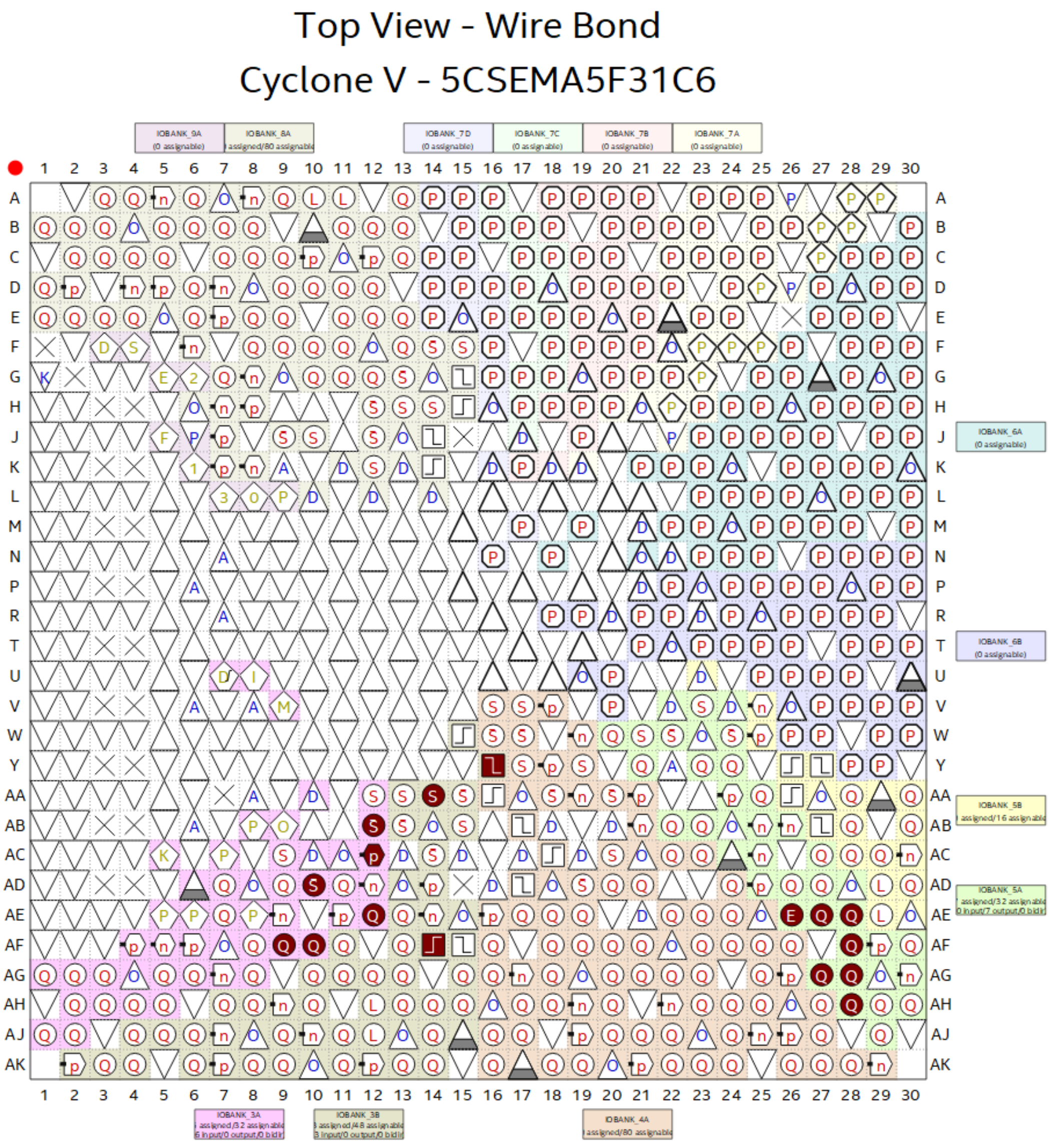
Name	Value at 0 ps
clk	B 0
e...	B 0
re...	B 0
c...	B 0...
...	B 0
...	B 0
...	B 0
...	B 0

0% 00:00:00

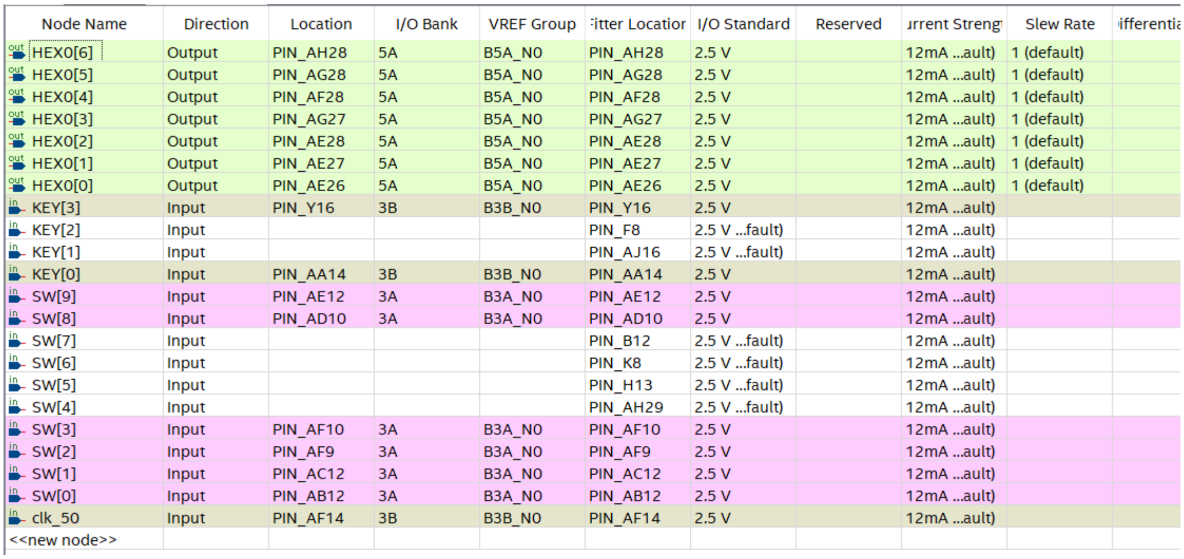
Lab1part3 RTL view:



Lab1part3 Pin Planner:

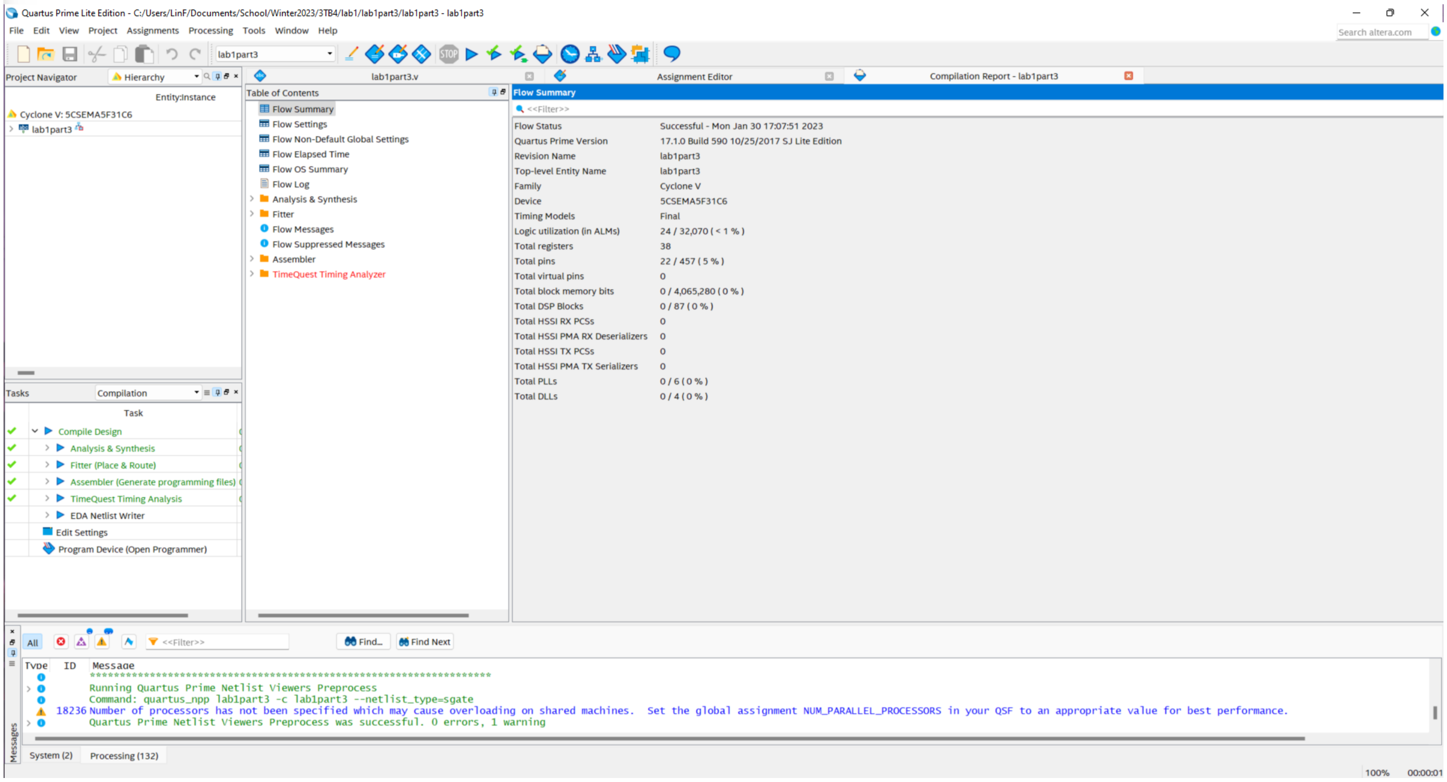


Top View - Wire Bond
Cyclone V - 5CSEMA5F31C6
IOBANK_9A (0 assignable)
IOBANK_8A assigned/80 assignable
IOBANK_7D (0 assignable)
IOBANK_7C (0 assignable)
IOBANK_7B (0 assignable)
IOBANK_7A (0 assignable)
IOBANK_6A (0 assignable)
IOBANK_6B (0 assignable)
IOBANK_5B assigned/16 assignable
IOBANK_5A assigned/32 assignable 0 input/7 output/0 bidir
IOBANK_3A assigned/32 assignable 6 input/0 output/0 bidir
IOBANK_3B assigned/48 assignable 3 input/0 output/0 bidir
IOBANK_4A assigned/80 assignable
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30
A B C D E F G H J K L M N P R T U V W Y AA AB AC AD AE AF AG AH AJ AK



Node Name	Direction	Location	I/O Bank	VREF Group	itter Locatior	I/O Standard	Reserved	urrent Streng	Slew Rate	ifferentia
HEX0[6]	Output	PIN_AH28	5A	B5A_N0	PIN_AH28	2.5 V		12mA ...ault)	1 (default)	
HEX0[5]	Output	PIN_AG28	5A	B5A_N0	PIN_AG28	2.5 V		12mA ...ault)	1 (default)	
HEX0[4]	Output	PIN_AF28	5A	B5A_N0	PIN_AF28	2.5 V		12mA ...ault)	1 (default)	
HEX0[3]	Output	PIN_AG27	5A	B5A_N0	PIN_AG27	2.5 V		12mA ...ault)	1 (default)	
HEX0[2]	Output	PIN_AE28	5A	B5A_N0	PIN_AE28	2.5 V		12mA ...ault)	1 (default)	
HEX0[1]	Output	PIN_AE27	5A	B5A_N0	PIN_AE27	2.5 V		12mA ...ault)	1 (default)	
HEX0[0]	Output	PIN_AE26	5A	B5A_N0	PIN_AE26	2.5 V		12mA ...ault)	1 (default)	
KEY[3]	Input	PIN_Y16	3B	B3B_N0	PIN_Y16	2.5 V		12mA ...ault)		
KEY[2]	Input				PIN_F8	2.5 V ...fault)		12mA ...ault)		
KEY[1]	Input				PIN_AJ16	2.5 V ...fault)		12mA ...ault)		
KEY[0]	Input	PIN_AA14	3B	B3B_N0	PIN_AA14	2.5 V		12mA ...ault)		
SW[9]	Input	PIN_AE12	3A	B3A_N0	PIN_AE12	2.5 V		12mA ...ault)		
SW[8]	Input	PIN_AD10	3A	B3A_N0	PIN_AD10	2.5 V		12mA ...ault)		
SW[7]	Input				PIN_B12	2.5 V ...fault)		12mA ...ault)		
SW[6]	Input				PIN_K8	2.5 V ...fault)		12mA ...ault)		
SW[5]	Input				PIN_H13	2.5 V ...fault)		12mA ...ault)		
SW[4]	Input				PIN_AH29	2.5 V ...fault)		12mA ...ault)		
SW[3]	Input	PIN_AF10	3A	B3A_N0	PIN_AF10	2.5 V		12mA ...ault)		
SW[2]	Input	PIN_AF9	3A	B3A_N0	PIN_AF9	2.5 V		12mA ...ault)		
SW[1]	Input	PIN_AC12	3A	B3A_N0	PIN_AC12	2.5 V		12mA ...ault)		
SW[0]	Input	PIN_AB12	3A	B3A_N0	PIN_AB12	2.5 V		12mA ...ault)		
clk_50	Input	PIN_AF14	3B	B3B_N0	PIN_AF14	2.5 V		12mA ...ault)		
<<new node>>										

Lab1part3 complication report:


Quartus Prime Lite Edition - C:/Users/LinF/Documents/School/Winter2023/3TB4/lab1/lab1part3/lab1part3 - lab1part3

Flow Summary

Flow Status	Successful - Mon Jan 30 17:07:51 2023
Quartus Prime Version	17.1.0 Build 590 10/25/2017 SJ Lite Edition
Revision Name	lab1part3
Top-level Entity Name	lab1part3
Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Final
Logic utilization (in ALMs)	24 / 32,070 (< 1 %)
Total registers	38
Total pins	22 / 457 (5 %)
Total virtual pins	0
Total block memory bits	0 / 4,065,280 (0 %)
Total DSP Blocks	0 / 87 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)

```
Type  ID    Message
            ******************************************************************
            Running Quartus Prime Netlist Viewers Preprocess
            Command: quartus_npp lab1part3 -c lab1part3 --netlist_type=sgate
      18236 Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
            Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 1 warning
```

Answers to lab questions:

1. The DE1-SoC.qsf file includes all the available pin assignments on the DE1-SoC board. By importing this file to the Assignment Editor, it automatically assign pins with names pre-defined in the file, it simplifies the pin assignment process during the lab so we don’t have to assign every pin manually.

2.

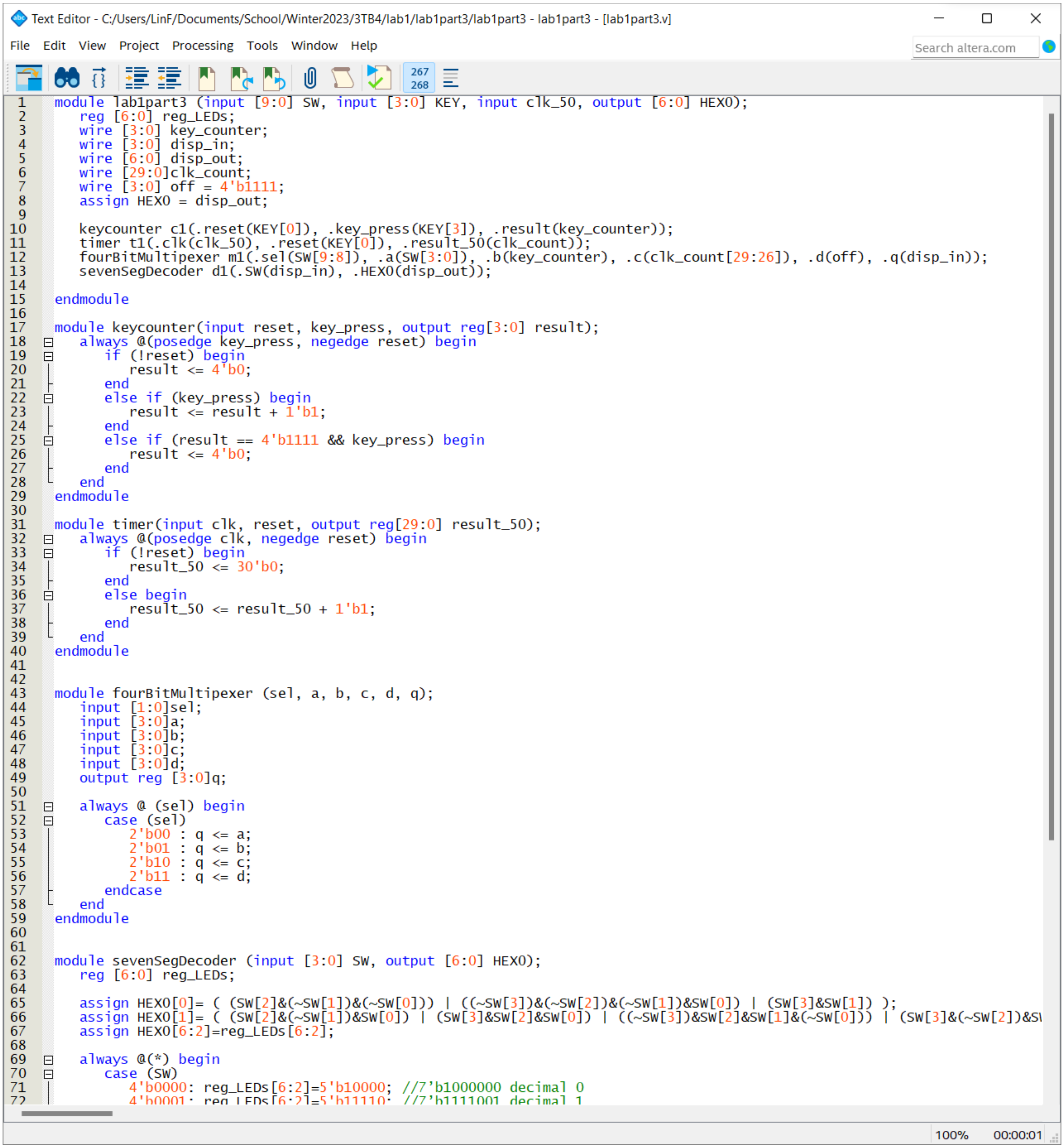
- Total number of logic elements used by your circuit: 24

- Total number of registers: 38

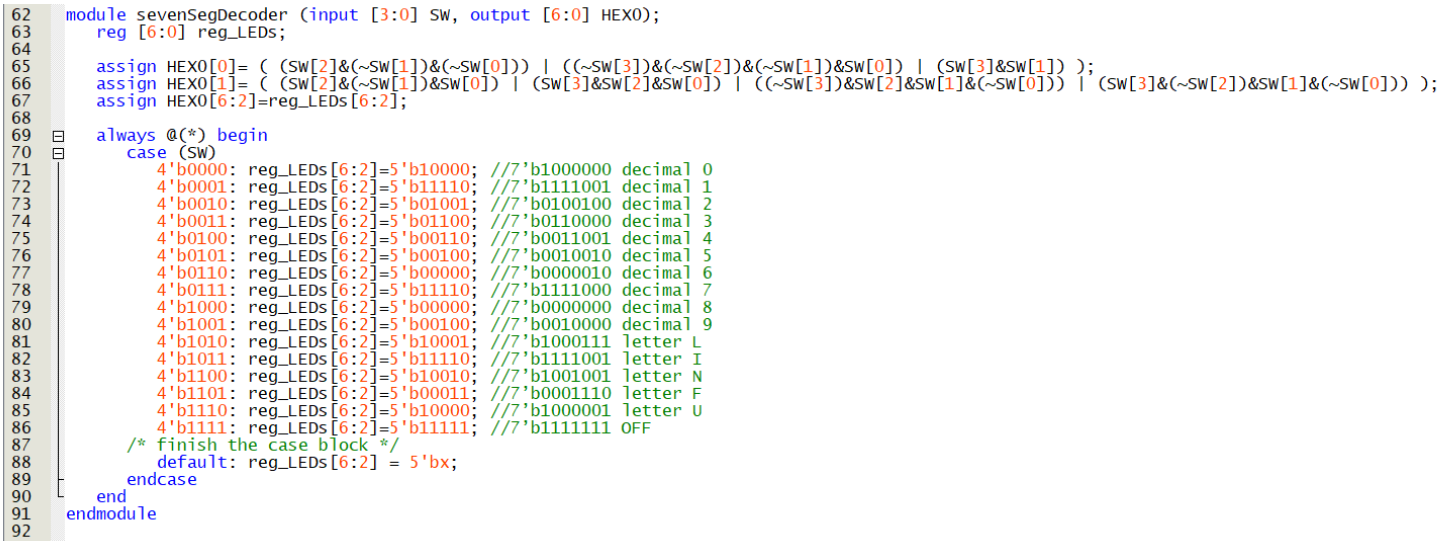
- Total number of pins: 22

- The maximum number of logic elements that can fit on the FPGA you used: 32,070

Code for lab1part3:


Text Editor - C:/Users/LinF/Documents/School/Winter2023/3TB4/lab1/lab1part3/lab1part3 - lab1part3 - [lab1part3.v]
File
Edit
View
Project
Processing
Tools
Window
Help
Search altera.com
267
268
100%
00:00:01

```
module lab1part3 (input [9:0] SW, input [3:0] KEY, input clk_50, output [6:0] HEX0);
   reg [6:0] reg_LEDs;
   wire [3:0] key_counter;
   wire [3:0] disp_in;
   wire [6:0] disp_out;
   wire [29:0]clk_count;
   wire [3:0] off = 4'b1111;
   assign HEX0 = disp_out;

   keycounter c1(.reset(KEY[0]), .key_press(KEY[3]), .result(key_counter));
   timer t1(.clk(clk_50), .reset(KEY[0]), .result_50(clk_count));
   fourBitMultipexer m1(.sel(SW[9:8]), .a(SW[3:0]), .b(key_counter), .c(clk_count[29:26]), .d(off), .q(disp_in));
   sevenSegDecoder d1(.SW(disp_in), .HEX0(disp_out));

endmodule

module keycounter(input reset, key_press, output reg[3:0] result);
   always @(posedge key_press, negedge reset) begin
      if (!reset) begin
         result <= 4'b0;
      end
      else if (key_press) begin
         result <= result + 1'b1;
      end
      else if (result == 4'b1111 && key_press) begin
         result <= 4'b0;
      end
   end
endmodule

module timer(input clk, reset, output reg[29:0] result_50);
   always @(posedge clk, negedge reset) begin
      if (!reset) begin
         result_50 <= 30'b0;
      end
      else begin
         result_50 <= result_50 + 1'b1;
      end
   end
endmodule


module fourBitMultipexer (sel, a, b, c, d, q);
   input [1:0]sel;
   input [3:0]a;
   input [3:0]b;
   input [3:0]c;
   input [3:0]d;
   output reg [3:0]q;

   always @ (sel) begin
      case (sel)
         2'b00 : q <= a;
         2'b01 : q <= b;
         2'b10 : q <= c;
         2'b11 : q <= d;
      endcase
   end
endmodule


module sevenSegDecoder (input [3:0] SW, output [6:0] HEX0);
   reg [6:0] reg_LEDs;

   assign HEX0[0]= ( (SW[2]&(~SW[1])&(~SW[0])) | ((~SW[3])&(~SW[2])&(~SW[1])&SW[0]) | (SW[3]&SW[1]) );
   assign HEX0[1]= ( (SW[2]&(~SW[1])&SW[0]) | (SW[3]&SW[2]&SW[0]) | ((~SW[3])&SW[2]&SW[1]&(~SW[0])) | (SW[3]&(~SW[2])&S
   assign HEX0[6:2]=reg_LEDs[6:2];

   always @(*) begin
      case (SW)
         4'b0000: reg_LEDs[6:2]=5'b10000; //7'b1000000 decimal 0
         4'b0001: reg_LEDs[6:2]=5'b11110; //7'b1111001 decimal 1
```



```
module sevenSegDecoder (input [3:0] SW, output [6:0] HEX0);
   reg [6:0] reg_LEDs;

   assign HEX0[0]= ( (SW[2]&(~SW[1])&(~SW[0])) | ((~SW[3])&(~SW[2])&(~SW[1])&SW[0]) | (SW[3]&SW[1]) );
   assign HEX0[1]= ( (SW[2]&(~SW[1])&SW[0]) | (SW[3]&SW[2]&SW[0]) | ((~SW[3])&SW[2]&SW[1]&(~SW[0])) | (SW[3]&(~SW[2])&SW[1]&(~SW[0])) );
   assign HEX0[6:2]=reg_LEDs[6:2];

   always @(*) begin
      case (SW)
         4'b0000: reg_LEDs[6:2]=5'b10000; //7’b1000000 decimal 0
         4'b0001: reg_LEDs[6:2]=5'b11110; //7’b1111001 decimal 1
         4'b0010: reg_LEDs[6:2]=5'b01001; //7’b0100100 decimal 2
         4'b0011: reg_LEDs[6:2]=5'b01100; //7’b0110000 decimal 3
         4'b0100: reg_LEDs[6:2]=5'b00110; //7’b0011001 decimal 4
         4'b0101: reg_LEDs[6:2]=5'b00100; //7’b0010010 decimal 5
         4'b0110: reg_LEDs[6:2]=5'b00000; //7’b0000010 decimal 6
         4'b0111: reg_LEDs[6:2]=5'b11110; //7’b1111000 decimal 7
         4'b1000: reg_LEDs[6:2]=5'b00000; //7’b0000000 decimal 8
         4'b1001: reg_LEDs[6:2]=5'b00100; //7’b0010000 decimal 9
         4'b1010: reg_LEDs[6:2]=5'b10001; //7’b1000111 letter L
         4'b1011: reg_LEDs[6:2]=5'b11110; //7’b1111001 letter I
         4'b1100: reg_LEDs[6:2]=5'b10010; //7’b1001001 letter N
         4'b1101: reg_LEDs[6:2]=5'b00011; //7’b0001110 letter F
         4'b1110: reg_LEDs[6:2]=5'b10000; //7’b1000001 letter U
         4'b1111: reg_LEDs[6:2]=5'b11111; //7’b1111111 OFF
      /* finish the case block */
         default: reg_LEDs[6:2] = 5'bx;
      endcase
   end
endmodule
```