**3TB4 Lab 1 Report**

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D flip-flop simulation:

Graphical user interface, application, table

Description automatically generated

D flipflop with active low synchronous reset:

Graphical user interface, application, table, Excel

Description automatically generated

D flipflop with active low synchronous reset and active low enable:

Graphical user interface, application, table

Description automatically generated

D latch:

Graphical user interface, application, table

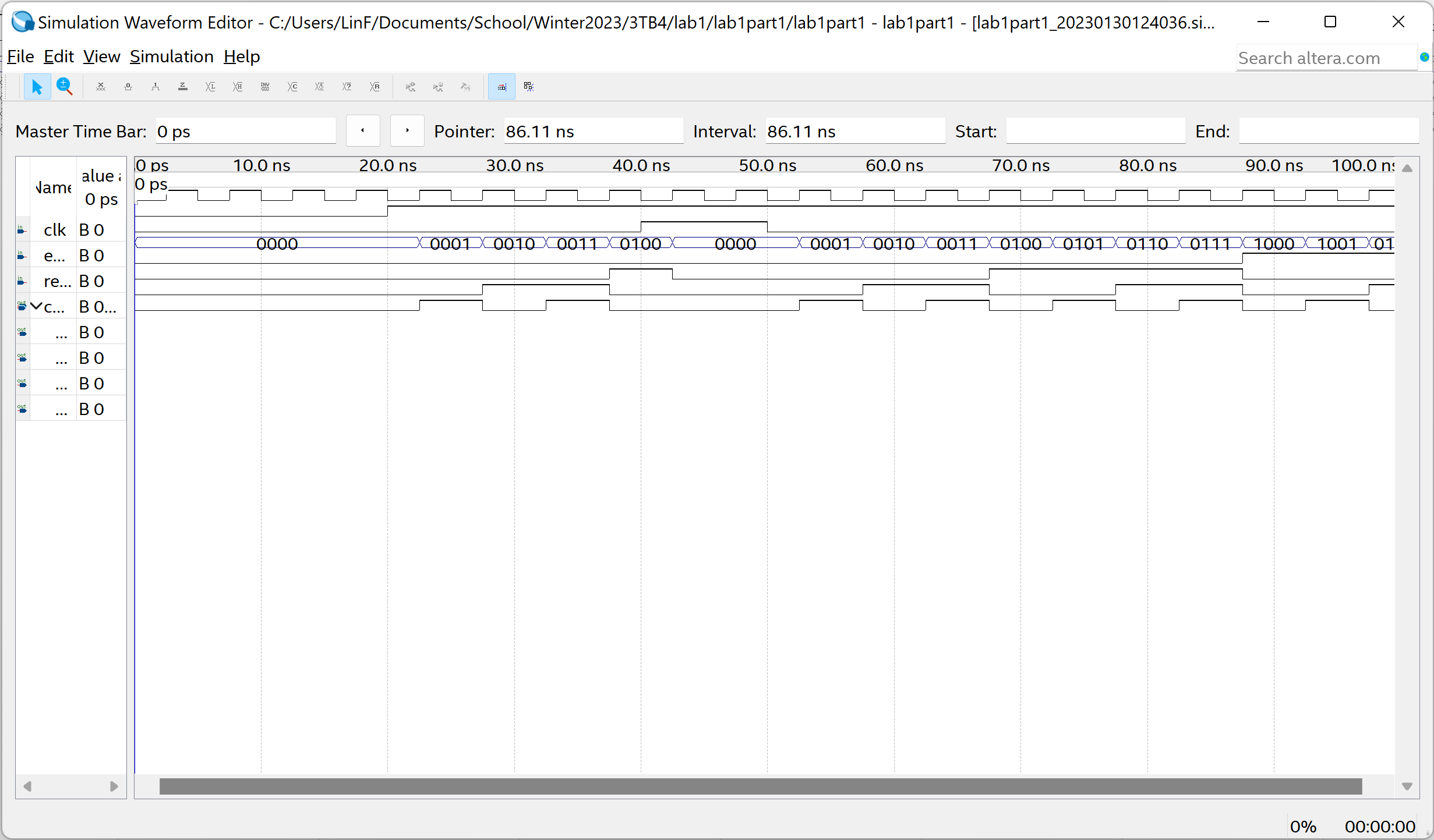
Description automatically generated

Multiplexer:

Graphical user interface, application, table

Description automatically generated

Counter:



Lab1part3 RTL view:

Diagram

Description automatically generated

Lab1part3 Pin Planner:

Map, scatter chart

Description automatically generated

Table

Description automatically generated

Lab1part3 complication report:

Graphical user interface, text, application, email

Description automatically generated

Answers to lab questions:

1. The DE1-SoC.qsf file includes all the available pin assignments on the DE1-SoC board. By importing this file to the Assignment Editor, it automatically assign pins with names pre-defined in the file, it simplifies the pin assignment process during the lab so we don’t have to assign every pin manually.

2.

• Total number of logic elements used by your circuit: 24

• Total number of registers: 38

• Total number of pins: 22

• The maximum number of logic elements that can fit on the FPGA you used: 32,070

Code for lab1part3:

Text

Description automatically generated

