DSD Final Project Scores

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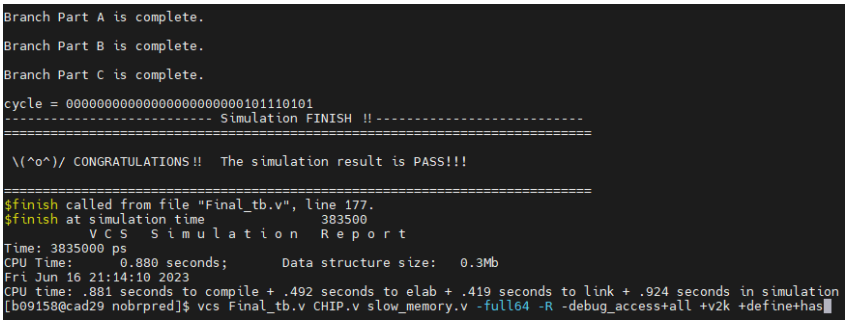
1. BrPred

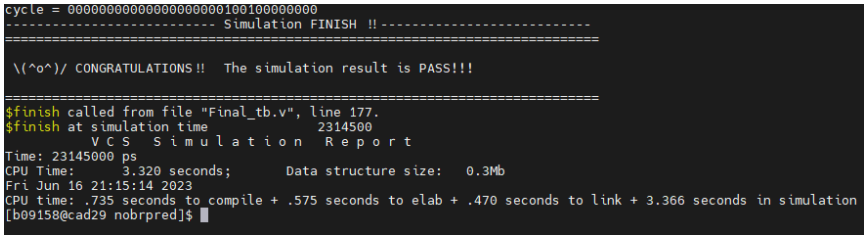
(1) Total execution cycles of given I_mem_BrPred: 373 cycles

截圖:



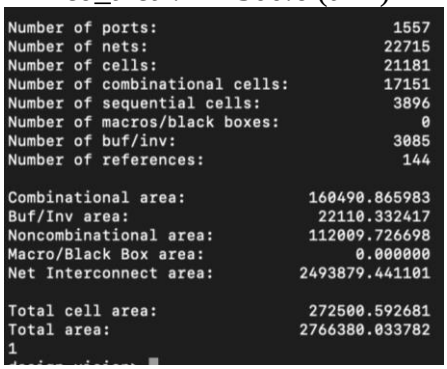
(2) Total execution cycles of given I_mem_hasHazard: 2304 cycles

截圖:

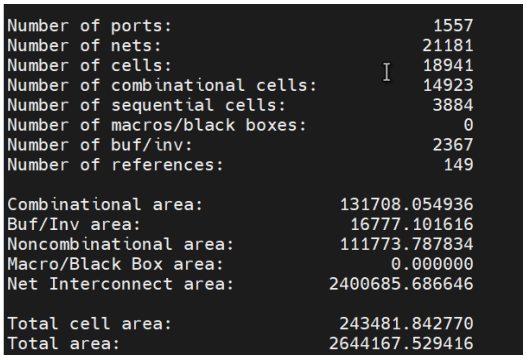


(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): 29018.8(um^2)

BrPred_area : 272500.6 (um^2)



Baseline_area : 243481.8 (um^2)



2. Compressed instructions

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same):18070.6 (um^2)

截圖:

Compression_area: 261552.4(um^2)

```
Number of ports:                        1557
Number of nets:                        22526
Number of cells:                       21514
Number of combinational cells:         17415
Number of sequential cells:             3965
Number of macros/black boxes:              0
Number of buf/inv:                      2504
Number of references:                    141

Combinational area:            147349.594784
Buf/Inv area:                   17900.780396
Noncombinational area:         114202.767160
Macro/Black Box area:               0.000000
Net Interconnect area:        2571206.615662

Total cell area:               261552.361945
Total area:                   2832758.977607
```

Baseline_area: 243481.8(um^2)

```
Number of ports:                        1557
Number of nets:                        21181
Number of cells:                       18941
Number of combinational cells:         14923
Number of sequential cells:             3884
Number of macros/black boxes:              0
Number of buf/inv:                      2367
Number of references:                    149

Combinational area:            131708.054936
Buf/Inv area:                   16777.101616
Noncombinational area:         111773.787834
Macro/Black Box area:               0.000000
Net Interconnect area:        2400685.686646

Total cell area:               243481.842770
Total area:                   2644167.529416
```

(2) Total Simulation Time of given I_mem_compression: 2089.8(ns)

截圖:

```
--------------------------- Simulation FINISH !!---------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
$finish called from file "Final_tb.v", line 159.
$finish at simulation time             2089800
           V C S   S i m u l a t i o n   R e p o r t
Time: 2089800 ps
CPU Time:      2.220 seconds;       Data structure size:   5.7Mb
Tue Jun 13 08:43:12 2023
CPU time: 3.758 seconds to compile + 1.253 seconds to elab + .847 seconds to link + 2.272
seconds in simulation
```

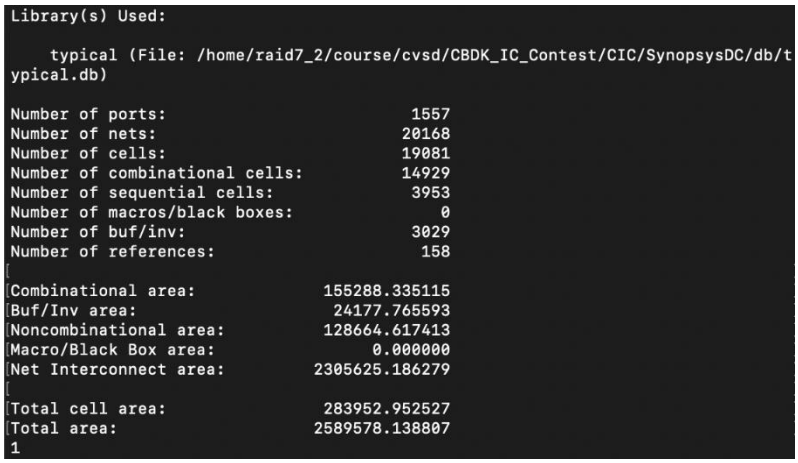
(3) Area*Total Simulation Time: 37763939.88(um^2 * ns)

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): 3.6(ns)

3. Q_sort

(1) Area: 283952.95(um^2)

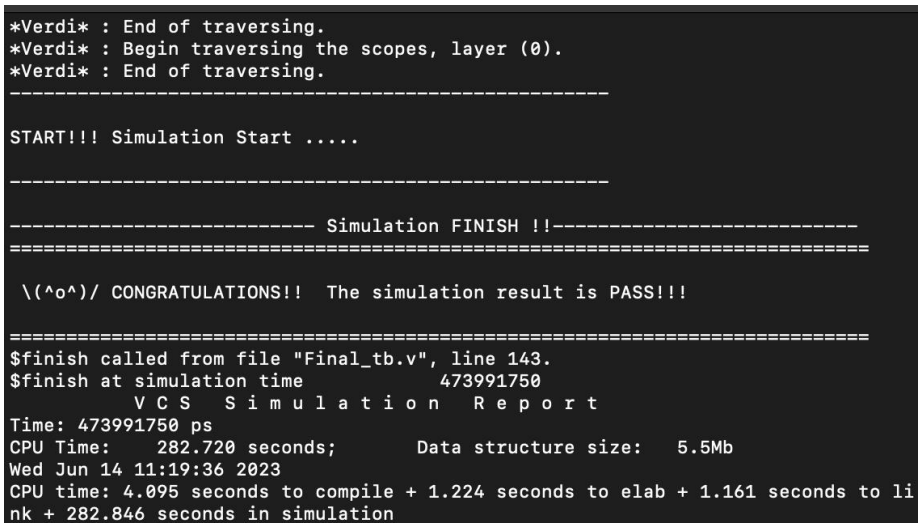
截圖:



```
Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/t
ypical.db)

Number of ports:                         1557
Number of nets:                         20168
Number of cells:                        19081
Number of combinational cells:          14929
Number of sequential cells:              3953
Number of macros/black boxes:               0
Number of buf/inv:                       3029
Number of references:                     158

Combinational area:            155288.335115
Buf/Inv area:                   24177.765593
Noncombinational area:         128664.617413
Macro/Black Box area:               0.000000
Net Interconnect area:        2305625.186279

Total cell area:               283952.952527
Total area:                   2589578.138807
1
```

(2) Best Total Simulation Time :473991.75 (ns)
(either using compressed or uncompressed instructions)
(we use compressed & old Final_tb)

截圖:



```
*Verdi* : End of traversing.
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.
-----------------------------------------------------

START!!! Simulation Start .....

-----------------------------------------------------

---------------------------- Simulation FINISH !!---------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
$finish called from file "Final_tb.v", line 143.
$finish at simulation time            473991750
           V C S   S i m u l a t i o n   R e p o r t
Time: 473991750 ps
CPU Time:    282.720 seconds;       Data structure size:   5.5Mb
Wed Jun 14 11:19:36 2023
CPU time: 4.095 seconds to compile + 1.224 seconds to elab + 1.161 seconds to li
nk + 282.846 seconds in simulation
```

(3) Area*Total Simulation Time:1.3459×10^{11} (um^2 * ns)

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc):2.7 (ns)