DSD Final Checkpoint Scores

1. Baseline

(1) Area: (um^2)

截圖:

```
****************************************
Report : area
Design : CHIP
Version: U-2022.12
Date   : Thu May 30 13:27:22 2024
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                         1594
Number of nets:                         22073
Number of cells:                        19186
Number of combinational cells:          15059
Number of sequential cells:              3961
Number of macros/black boxes:               0
Number of buf/inv:                       1551
Number of references:                     106

Combinational area:             130044.604528
Buf/Inv area:                    11513.464187
Noncombinational area:          115284.010563
Macro/Black Box area:                0.000000
Net Interconnect area:         2614886.804047

Total cell area:                245328.615091
Total area:                    2860215.419137
1
```

(2) Total Simulation Time of given noHazard testbench: 1705 (ns)

截圖:

RTL:

```
------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
$finish called from file "./Final_tb.v", line 218.
$finish at simulation time              170500
         V C S   S i m u l a t i o n   R e p o r t
Time: 1705000 ps
CPU Time:      1.260 seconds;       Data structure size:   0.3Mb
Thu May 30 13:43:21 2024
CPU time: 1.291 seconds to compile + .866 seconds to elab + .584 seconds to link + 1.310 seconds in simulation
```

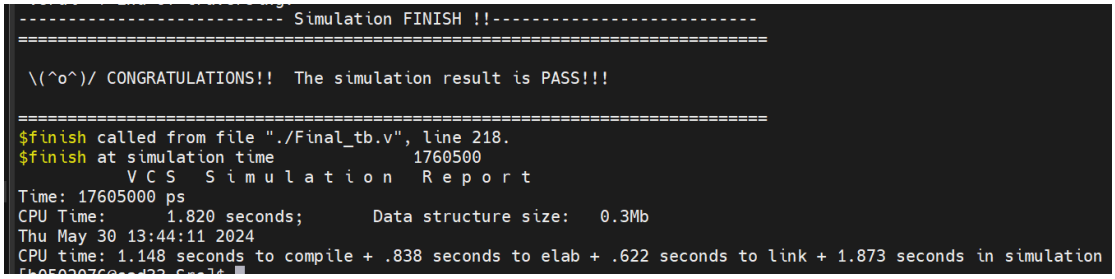
Gate Level:

```
*Verdi* : End of traversing.
------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
$finish called from file "Final_tb.v", line 218.
$finish at simulation time             1705000
         V C S   S i m u l a t i o n   R e p o r t
Time: 1705000 ps
CPU Time:      2.230 seconds;       Data structure size:   5.6Mb
Thu May 30 13:37:22 2024
CPU time: 7.701 seconds to compile + 2.548 seconds to elab + 1.367 seconds to link + 2.284 seconds in simulation
```

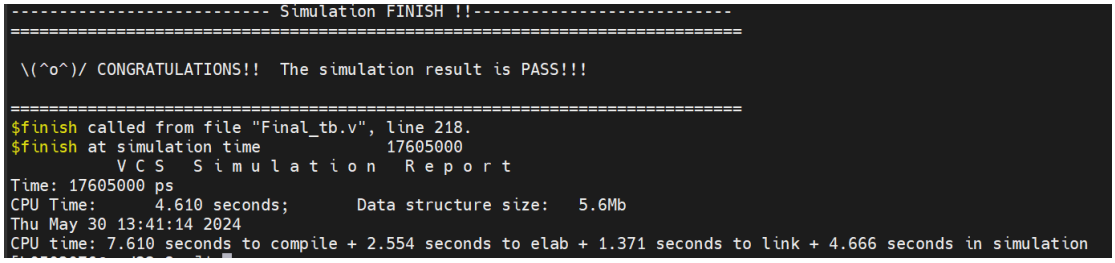
(3) Total Simulation Time of given hasHazard testbench: 17695 (ns)

截圖:

RTL:



Gate Level:



(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)

Ans: 10 (ns)