林桓鈺 B10502013

DSD HW2

- Gate-level simulation clock cycle : 3.6
- Total cell area = 90,386.548917
- Cost = 90,386.548917 × 3.6 = 325,391.5761012

```
Inferred memory devices in process
        in routine CHIP line 173 in file
                '/home/raid7_2/userb10/b0502013/DSD_HW2/verilog/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|      PC_r_reg       | Flip-flop |  32   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
```