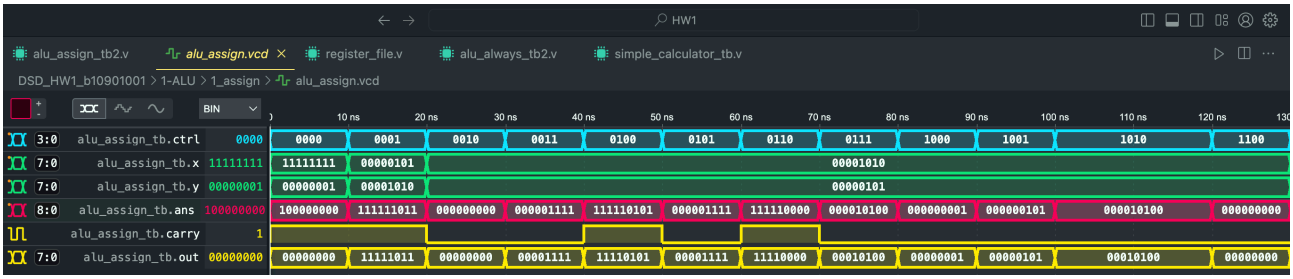
林桓鈺 B10502013

Digital System Design Homework #1

ALU

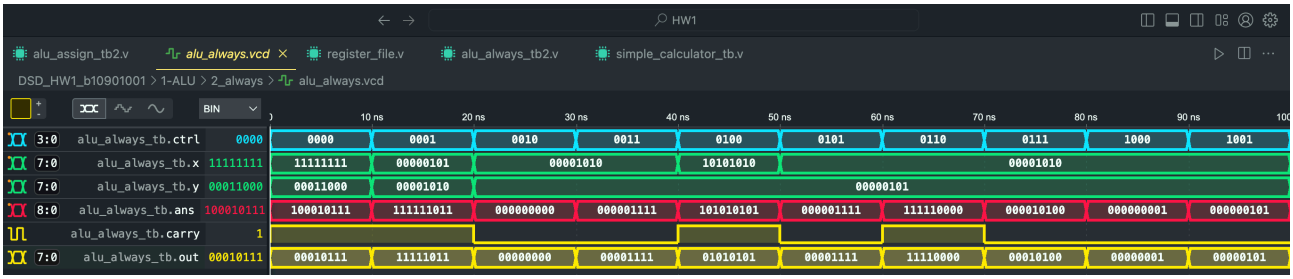
I. alu_assign.v

A. Waveform :



II. alu_always.v

A. Waveform :



III. Verify the correctness

1. After each test case is executed, it compares ans with carry and out. If they are equal, the test case is considered passed; otherwise, it is considered failed. This method ensures the consistency between the expected behavior and the actual behavior of the test cases.

8x8 Register File:

I. alu_register_file.v

A. Waveform :

- Since using BIN format will cause the data to be incomplete, the data on busX and busY are displayed in HEX format.

B. Verify the correctness

1. Case 1:
   a) In this case, WEN is set to 1, enabling the write operation to register r_6. The value AA (10101010 in binary) will be written to register r_6. The read operations will then occur, with busX outputting the value from register r_6 and busY outputting the value from register r_7. However, since the write to register r_7 doesn't happen immediately, busY might still contain the previous value until the next clock cycle.
2. Case 2:
   a) Here, WEN is set to 1, enabling the write operation to register r_7. The value FF (11111111 in binary) will be written to register r_7. Subsequently, busX will output the value from register r_7, and busY will output the value from register r_6.
3. Case 3:
   a) WEN is set to 1, allowing the write operation to register r_0. The value A5 (10100101 in binary) will be written to register r_0. Afterward,

busX will output the value from register r_0, and busY will output the value from register r_1.

4. Case 4:
   a) In this scenario, WEN is set to 0, disabling the write operation. Thus, no new value will be written to any register. BusX will output the value from register r_2, and busY will output the value from register r_3.
5. Case 5:
   a) WEN is set to 1, enabling the write operation to register r_5. The value 7F (01111111 in binary) will be written to register r_5. Then, busX will output the value from register r_0, and busY will output the value from register r_5.
6. Case 6:
   a) WEN is set to 1, allowing the write operation to register r_3. The value 0A (00001010 in binary) will be written to register r_3. Following this, busX will output the value from register r_3, and busY will output the value from register r_6.

Reflection

Because I am more accustomed to writing programs on my local machine, for this assignment I used iverilog for compiling and running simulations. To visualize waveforms, I found a plugin called WaveTrace on VS Code, which allows me to directly view waveforms in the editor. However, it only supports the .vcd file format. Therefore, I modified the testbench to generate .vcd files instead of .fsdb files, enabling me to open waveforms directly in VS Code.

During the lecture, the TA mentioned that when using assign, if the right-hand side (RHS) values are sometimes 9 bits and sometimes 8 bits, only the last eight bits will be output, potentially causing the carry not to be assigned a value. However, I did not encounter this issue while writing and simulating my program. I speculate that it might be due to differences in the compiling system, resulting in different outputs.Please the TA could pay extra attention to this aspect when testing my programs.