**DSD Final Project Scores**

**1. BrPred**

(1) Total execution cycles of given I\_mem\_BrPred:

截圖:

(2) Total execution cycles of given I\_mem\_hasHazard:

截圖:

(3) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)

**2. Compressed instructions**

(1) Total Simulation Time of given I\_mem\_compression: (ns)

截圖:

(2) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)

**3. Multiplication instructions**

(1) Total Simulation Time of given Mul/I\_mem: (ns)

截圖:

(2) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)

**4. Q\_sort & Conv**

(1) Area: (um2)

截圖:

(2) Total Simulation Time of Q\_Sort: (ns)

(either using compressed or uncompressed instructions)

截圖:

(3) Total Simulation Time of Conv: (ns)

(either using compressed or uncompressed instructions)

截圖:

(3) Area\*Total Simulation Time Q\_Sort\*Total Simulation Time of Conv: (um2 \* ns2)

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)