An Energy-Efficient Fast Maximum Power Point Tracking Circuit in an 800-μW Photovoltaic Energy Harvester

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***Abstract*—An energy-efficient maximum power point tracking (MPPT) circuit with a fast-tracking time for use with 800-μW PV energy harvesters is presented in this paper. The proposed MPPT circuit uses a successive approximation register MPPT algorithm, which has a power down mode and a fast tracking time, to achieve low power consumption and energy savings. The prototype MPPT circuit, which consists of analog-based circuits, has been implemented and fabricated in a 0.35-μm BCDMOS process. The MPPT core occupies an area of 3 mm^2 and consumes 4.6 μW of power. The tracking time is reduced by 69.4% and the stored energy is increased by 31.4% as compared to the conventional hill climbing-based MPPT algorithm under indoor conditions.**

***Index Terms*—Energy harvesting, maximum power point tracking (MPPT), photovoltaic (PV), solar cell, wireless sensor networks (WSNs).**

I. Introduction

RECENTLY, photovoltaic (PV) cells, which convert solar irradiation directly into electrical energy, have been widely utilized as the energy harvesters in applications such as wireless sensor networks (WSNs), autonomous systems, and power plant systems. However, there are several challenges to energy harvesting with PV cells. PV cells suffer from a low efficiency of approximately 10–40%. Furthermore, the maximum output power from a PV cell degrades under changing atmospheric conditions [1], [2]. To maximize the efficiency of the PV energy harvester, a maximum power point tracking (MPPT) technique, which enables the operating point of the PV cells to track the maximum power point (MPP), has been implemented in the PV energy harvesters [2]–[9].

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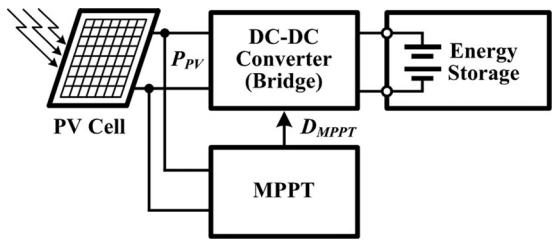

Fig. 1. Conventional PV energy harvester system.

Fig. 1 shows a block diagram of the conventional PV energy harvester, which consists of PV cells, a dc–dc converter, an energy storage, and an MPPT circuit [9]. Based on the difference between the previous and current operating points of the PV cells, the MPPT circuit selects a next operating point so as to maximize the PV output power. The dc–dc converter, which changes the operating point of the PV cell according to the duty control bits D_{MPPT} from the MPPT circuit, delivers the maximized energy from the PV cell to an energy storage such as a battery or supercapacitor. The MPPT circuit enables the PV energy harvester to deliver the maximum energy under various atmospheric conditions.

The conventional PV energy harvester has two sources of energy loss: the MPPT circuit and the dc–dc converter. To increase the efficiency of the PV energy harvester, the energy losses from the MPPT circuit and the dc–dc converter need to be minimized. In high-power applications such as solar power plant systems, the MPPT circuit, which is implemented using an analog-to-digital converter and a microcontroller, consumes less than 2% of the generated energy from the PV cell [9]–[14]; therefore, the energy loss in the MPPT circuit is negligible. The energy efficiency of the dc–dc converter is one of the most critical in high-power applications. In low-power applications such as wireless sensor networks, because the range of the PV cell output is from a few hundred microwatts to a few milliwatts, the energy loss in the MPPT circuit is responsible for a significantly larger portion of the generated energy from the PV cell [15]–[17]. Therefore, the minimization of energy consumption in the MPPT circuit is the most significant challenge in low-power energy harvesting applications.

In this paper, we present an energy-efficient PV energy harvester with 800-μW PV cells for WSNs. To reduce the energy loss in the MPPT circuit, an MPPT controller, adopting a successive approximation register (SAR) method and a power down

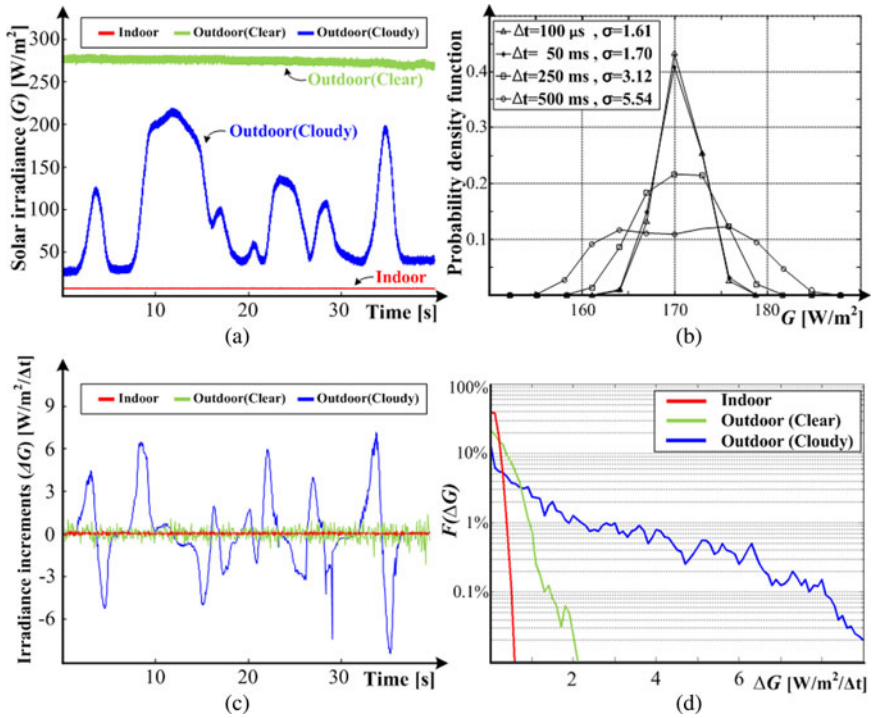

Fig. 2. Examples of measured irradiance data. (a) Measured data with 400k Samples/s. (b) Probability density function of the largest irradiance variation part in (a) with various time intervals Δt. (c) Irradiance increments with Δt of 50 ms. (d) Frequency distribution function of irradiance increments.

mode, is proposed. The proposed controller is based on a hill climbing algorithm with a fast tracking time. The remainder of this paper is organized as follows. Section II describes the effect of irradiance variation on the PV cell and analyzes the power down mode of the PV energy harvester. The proposed PV energy harvester with the SAR MPPT is described in Section III. Section IV reports the experimental results. Finally, Section V is devoted to conclusions.

II. Design Considerations

The efficiency of the energy harvester, including the PV cell, heavily depends upon the conditions of solar irradiance. This section quantifies and analyzes the irradiance variation in the measured datasets. In addition, the effectiveness of the power down mode in the PV energy harvester is examined under the measured irradiance conditions. Since a perpetual MPPT operation under small irradiance variation wastes a portion of the energy of the several hundreds of microwatts of the PV energy harvester, the power down mode during the MPPT operation is a possible solution to minimize the energy loss in the MPPT circuit.

A. Variability of Solar Irradiance on the PV Cell

Several previous studies regarding the variability of solar irradiance analyzed a dataset of irradiance at a sampling period of either 1-h, 1-min, or 1-s [18]. However, since the time constant of the PV cell, which represents the dynamic time response of the PV cell, is considerably faster [19], this work uses a fast-sampled dataset of solar irradiance to allow precise analysis. The sampling period used to measure the changes in the solar irradiance is 10 μs or faster for our target PV cell, which has a time constant of 20 μs.

Fig. 2(a) shows the measured datasets for an irradiation G with a sampling period of 2.5 μs. The measured irradiance, which includes noise components, is slowly changed in comparison with the sampling period. Fig. 2(b) depicts the probability density function of the irradiance that has the largest irradiance variation in Fig. 2(a), at various sampling interval Δt. As Δt increases, the standard deviation σ, which represents the diversity of the irradiance during Δt, also increases. Due to the relative standard deviation σ/G less than 1% at a Δt of 50 ms, a representative value of irradiance G_i can be defined as the mean value of the irradiance during the period Δt of 50 ms. A variation in irradiance can be represented by the irradiance increments ΔG for a Δt of 50 ms, as shown in Fig. 2(c). Here, $\Delta G = G_{i+1} - G_i$. G_{i+1} and G_i are two consecutive irradiances with a time interval of Δt. Fig. 2(d) shows the frequency distribution function of the irradiance increments $F(\Delta G)$, which classifies ΔG according to the number of times that the irradiance changes of ΔG occur [20].

B. Power Down Mode in MPPT

The irradiance variability can be modeled as a ramp signal, which has an amplitude of ΔG_i, and the probability of the ramp signal $F(\Delta G_i) \cdot N$ with a period of $\Delta t = 50$ ms, as shown in Fig. 3(a) [21], [22]. Here, N is the total number of cycles of the ramp signal over a period of T. $F(\Delta G_i) \cdot N$ refers to how frequently the ramp irradiance signal with the amplitude of ΔG_i occurs during a period of T. Fig. 3(b) shows the operation of the MPPT with the power down mode under the conditions

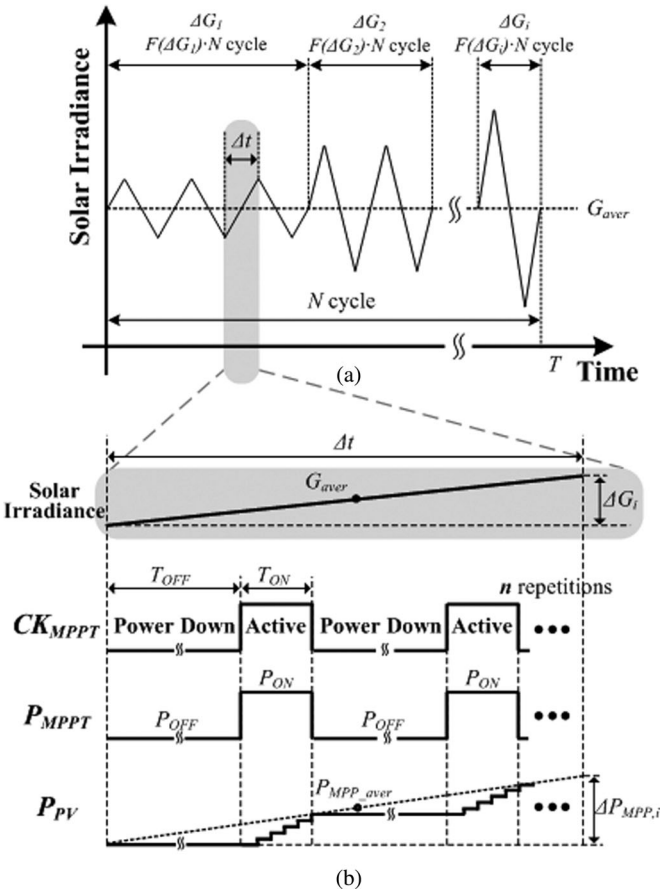

Fig. 3. (a) Modeling of irradiance variation. (b) Timing diagram of MPPT operation with power down mode.

of the highlighted irradiance variation. In the active mode, the MPPT circuit is turned ON and the PV output power $P_{\rm PV}$ tracks the MPP. The MPP tracking should be performed within the active mode time $T_{\rm ON}$. In the power down mode, the MPPT circuit turns OFF and keeps the load impedance of the PV cell during the power down mode time $T_{\rm OFF}$. Although $P_{\rm PV}$ has a small change in the power down mode, this analysis does not consider the variation of $P_{\rm PV}$ during power down mode, since this quantity of variation is small compared to the generated energy level of a PV cell.

The energy delivered by the PV cell to the energy storage $E_{\rm Store}$ is given by

$$E_{\rm Store} = E_{\rm PV} - E_{\rm MPPT} = \int P_{\rm PV}(t)dt - \int P_{\rm MPPT}(t)dt \tag{1}$$

where $P_{\rm PV}$ is the power produced by the PV cell and $P_{\rm MPPT}$ is the power consumed by the MPPT circuit. In (1), the energy loss in the dc–dc converter is neglected. Here, we assume that the maximum power $P_{\rm MPP}$ of the PV cell is proportional to the solar irradiance [10] and that it is represented by an increment in the maximum power $\Delta P_{{\rm MPP},i}$; the average value of the maximum power $P_{\rm MPP\_aver}$ during Δt is shown in Fig. 3(b). The energy generated by the PV cell and the energy consumed by the MPPT circuit during Δt ($E_{{\rm PV},\Delta t}$ and $E_{{\rm MPPT},\Delta t}$) can be expressed as

$$\begin{aligned} E_{{\rm PV},\Delta t} &= \int_0^{\Delta t} P_{\rm PV}\,dt \\ &= P_{\rm MPP\_aver}\Delta t - \frac{\Delta P_{{\rm MPP},i}}{2}T_{\rm OFF} \end{aligned} \tag{2}$$

$$\begin{aligned} E_{{\rm MPPT},\Delta t} &= \int_0^{\Delta t} P_{\rm MPPT}\,dt \\ &= (T_{\rm ON}P_{\rm ON} + T_{\rm OFF}P_{\rm OFF})\,\frac{\Delta t}{T_{\rm ON}+T_{\rm OFF}} \end{aligned} \tag{3}$$

where $P_{\rm ON}$ and $P_{\rm OFF}$ are the average power consumptions of the MPPT circuit in the active mode and the power down mode, respectively. In (2) and (3), the variation of $P_{\rm PV}$ in the active mode is simplified with a constant increment. Because the ramp irradiance signal, with an amplitude of ΔG_i and period of $2\Delta t$, repeats $F(\Delta G_i)\cdot N$ times during a time period T, the energy generated by the PV cell and energy consumed by the MPPT circuit during T ($E_{{\rm PV},T}$ and $E_{{\rm MPPT},T}$) are as follows:

$$\begin{aligned} E_{{\rm PV},T} &= \sum_{i=1}^{\infty} E_{{\rm PV},\Delta t}F(\Delta G_i)\frac{T}{\Delta t} \\ &= P_{\rm MPP\_aver}T - \frac{T}{2\Delta t}\sum_{i=1}^{\infty}\Delta P_{{\rm MPP},i}F(\Delta G_i)T_{\rm OFF} \end{aligned} \tag{4}$$

$$\begin{aligned} E_{{\rm MPPT},T} &= E_{{\rm MPPT},\Delta t}\frac{T}{\Delta t} \\ &= (T_{\rm ON}P_{\rm ON} + T_{\rm OFF}P_{\rm OFF})\,\frac{T}{T_{\rm ON}+T_{\rm OFF}}. \end{aligned} \tag{5}$$

Then, the delivered energy from the PV cell to the energy storage can be obtained as

$$\begin{aligned} E_{\rm Store} = P_{\rm MPP\_aver}T &- \frac{T_{\rm ON}P_{\rm ON}+T_{\rm OFF}P_{\rm OFF}}{T_{\rm ON}+T_{\rm OFF}}T \\ &- \frac{T}{2\Delta t}\sum_{i=1}^{\infty}\Delta P_{{\rm MPP},i}F(\Delta G_i)T_{\rm OFF}. \end{aligned} \tag{6}$$

Fig. 4(a) shows the relationship between the energy delivered by the PV cell to the energy storage $E_{\rm store}$ and the power down mode time $T_{\rm OFF}$ for various weather conditions. Here, $P_{\rm ON}$ is 200 μW, $P_{\rm OFF}$ is 200 nW, $T_{\rm ON}$ is 650 μs, T is 600 s, and the weather conditions from the dataset in Fig. 2 are used. There is an optimal power down mode time that minimizes energy loss in the MPPT circuit. $T_{\rm OFF}$ = 42, 15.5, and 34.5 ms are the optimal values for indoor conditions, cloudy outdoor conditions, and clear outdoor conditions, respectively. Fig. 4(b) compares the values of $E_{\rm store}$ with and without using the power down mode under different weather conditions. The power down mode increases the value of $E_{\rm Store}$ by 32%, 12%, and 4% under the indoor, cloudy outdoor, and clear outdoor conditions, respectively.

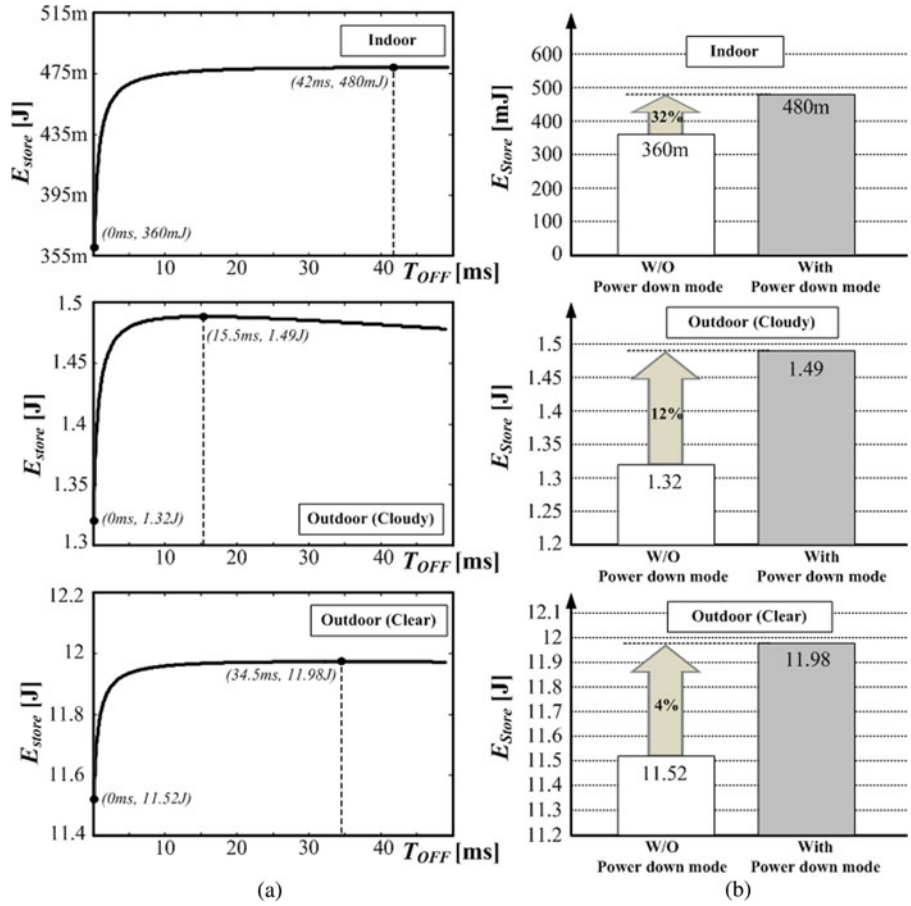

Fig. 4. (a) Energy delivered by the PV cell to the energy storage $E_{\rm store}$ versus power down mode time $T_{\rm OFF}$ for various weather conditions. (b) Performance $E_{\rm Store}$ improvement by the power down mode.

III. Proposed PV Energy Harvesters

A. SAR MPPT Algorithm

The selection of the optimal value of $T_{\rm OFF}$ for the power down mode is critical to reduce the energy consumed by the MPPT circuit. However, because the MPPT operation is suspended when the system is in the power down mode, the operating point of the PV cell is different from the ideal MPP at the beginning of the active mode. To reduce waste of the energy delivered in the active mode, a short $T_{\rm ON}$ is required. Moreover, a short $T_{\rm ON}$ results in additional energy savings for the MPPT circuit, as derived in (5).

Fig. 5 presents a flow diagram of the proposed SAR MPPT algorithm with a fast MPPT time, which can reduce $T_{\rm ON}$. This algorithm is a hill climbing algorithm with SAR operation. The SAR MPPT determines the direction of perturbation of $D_{\rm MPPT}$, which represents the operating point of the PV cell, using the binary search method of successive approximation. If the value of $D_{\rm MPPT}$ increases, the operating point moves in such a direction that the output voltage of the PV cell is decreased. Assume that a 4-bit $D_{\rm MPPT}$ is used in the MPPT operation; it begins by comparing the output power of the PV cell [$P_{\rm PV}(t-1)$] at $D_{\rm MPPT} = 1000$ and $P_{\rm PV}(t)$ at $D_{\rm MPPT} = 1001$. $P_{\rm PV}(t)$ and $P_{\rm PV}(t-1)$ represent the PV output power of the current state and the previous state, respectively. If $P_{\rm PV}(t) > P_{\rm PV}(t-1)$, the duty control bits, which determine the next states [$P_{\rm PV}(t+1)$ and $P_{\rm PV}(t+2)$], are set to $D_{\rm MPPT} = 1100$ and $D_{\rm MPPT} = 1101$. In contrast, if $P_{\rm PV}(t) < P_{\rm PV}(t-1)$, the duty control bits of the next states are $D_{\rm MPPT} = 0100$ and $D_{\rm MPPT} = 0101$. This SAR operation starts to decide the MSB bit to an LSB bit. After the completion of the SAR operation, the operating point of the PV cell is located at the MPP and the system enters the power down mode. In the power down mode, the proposed algorithm maintains the final value of $D_{\rm MPPT}$ and the other operations are suspended, which results in no power consumption in the MPPT circuit during the power down mode.

The tracking time of the MPPT algorithm is the required time to reach the MPP, when the irradiance changes. It can be represented by the MPPT operation cycles. Let us assume that an N-bit $D_{\rm MPPT}$ is used in the MPPT operations. The conventional hill climbing algorithm works like an N-bit digital counter and needs additional 4 cycles to confirm that the PV output power reaches the MPP. Therefore, the conventional hill climbing algorithm requires $2^N + 4$ cycles to reach the MPP in the worst case, whereas the proposed SAR MPPT algorithm requires $2N-1$ cycles to reach the MPP. In this case, the step size of the conventional hill climbing algorithm is equal to the smallest step size of the SAR MPPT algorithm. Fig. 6 shows ideal power tracking graphs for the conventional hill climbing algorithm (4 bit) and the proposed SAR MPPT algorithm (4 bit), and compares

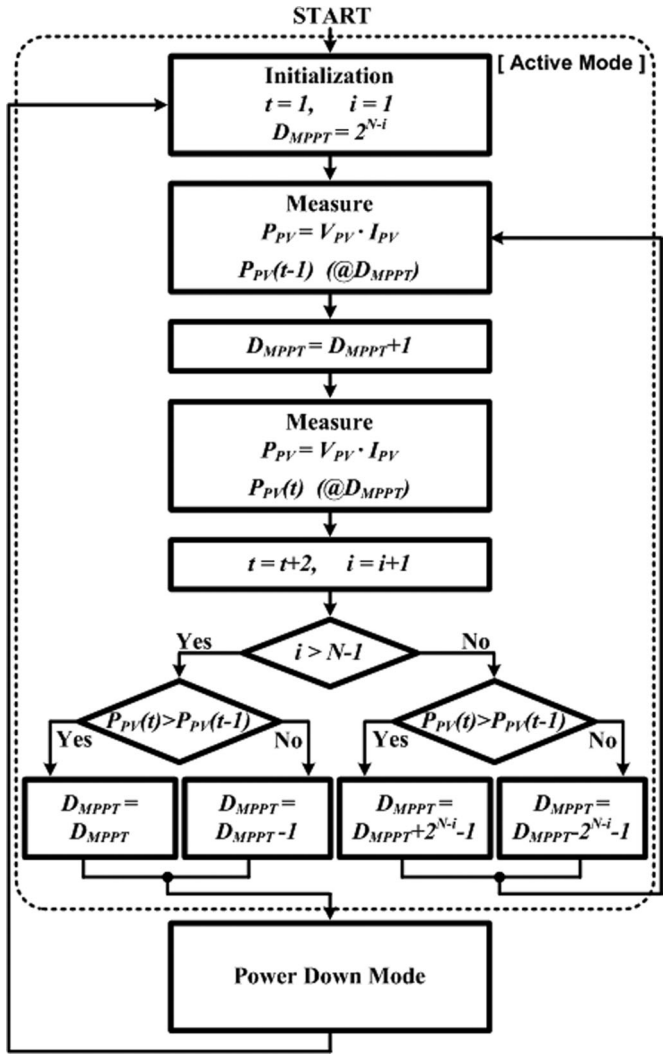

Fig. 5. Flowchart for the proposed SAR MPPT algorithm.

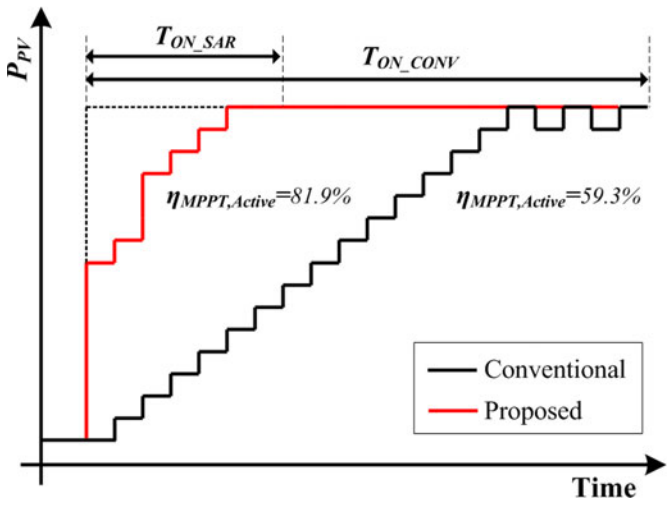

Fig. 6. Performance comparison graphs between the conventional hill climbing (4 bit) and the proposed SAR MPPT algorithms (4 bit) in the active mode.

their MPPT algorithm during only active mode (for further details, see the Appendix). The proposed SAR MPPT algorithm achieves a fast tracking time, no oscillations around the MPP. Furthermore, the enhancement of the MPPT efficiency during active mode improves the entire MPPT tracking efficiency.

B. Circuit Description

Fig. 7 shows a block diagram of the proposed MPPT circuit for WSN PV energy harvesters. The PV energy harvester consists of an MPPT circuit, a dc–dc converter, a clock generator, and an energy storage. The dc–dc converter utilizes the conventional buck-type converter with an external inductor and a digital pulsewidth modulator. The clock generator produces system clock signals for execution of the proposed SAR MPPT algorithm. To achieve low power consumption, the MPPT circuit, which operates according to the proposed SAR MPPT algorithm, is implemented with an analog-based voltage-and-current sensing circuit, a power comparator circuit, and SAR logic circuits.

The voltage-and-current sensing circuit is implemented using a switched-capacitor integrator circuit, as shown in Fig. 8(a). Here, the two-phase clocks of PH_1 and PH_2 are nonoverlapping. If PH_1 = High, C_1 and C_3 sample the current and voltage of the PV cell at a sensing resistor R_{Sense}, respectively. If PH_2 = High, the amplifier integrates the output current I_{PV} and voltage V_{PV} of the PV cell. The switched-capacitor integrator reduces the effects of the fluctuation of V_P and V_N. In addition, the common-mode input voltage of the amplifier maintained as a constant, which improves the linearity of the amplifier gain.

The power comparator circuit is illustrated in Fig. 8(b). The multiplier circuit is implemented using the conventional analog multiplier of the Gilbert-cell [23]. It calculates the output power of the PV cell using $V_{V,\mathrm{PV}}$ and $V_{I,\mathrm{PV}}$. The input voltage ranges of the Gilbert cell ($V_{V,\mathrm{PV}}$ and $V_{I,\mathrm{PV}}$) are 400 $\mathrm{mV}_{p\text{-}p}$. To compare the output power of the current state [$V_{P,\mathrm{PV}}(t)$] with the output power of the previous state [$V_{P,\mathrm{PV}}(t-1)$], the sample-and-hold circuit and comparator are used. If $V_{P,\mathrm{PV}}(t) > V_{P,\mathrm{PV}}(t-1)$, the output of the power comparator $V_{P,\mathrm{CMP}}$ becomes high. $V_{P,\mathrm{CMP}}$ determines the direction of the next states in the SAR MPPT algorithm.

Fig. 8(c) presents a circuit diagram of the 6-bit SAR logic [24]. To support the controlling of the LSB of D_{MPPT}, a flip-flop and a multiplexer are added. In the active mode, the signal *Start* is set to high and D_{MPPT} changes according to the SAR MPPT algorithm. In the power down mode, D_{MPPT} is stored and the last value of the active mode is retained.

IV. Experimental Result

The proposed circuit was implemented and fabricated in a 0.35-μm BCDMOS process. Fig. 9 shows a microphotograph of the fabricated chip. The proposed MPPT circuit excluding the dc–dc converter, occupies an area of 2000 μm $\times$ 1500 μm. The buck-type dc–dc converter with external inductor of 47 μH is used. The switching frequency of the dc–dc converter is 500 kHz and R_{on} of the switches is 165 mΩ. The experimental environment of the PV energy harvester is shown in Fig. 10. A 1000-W

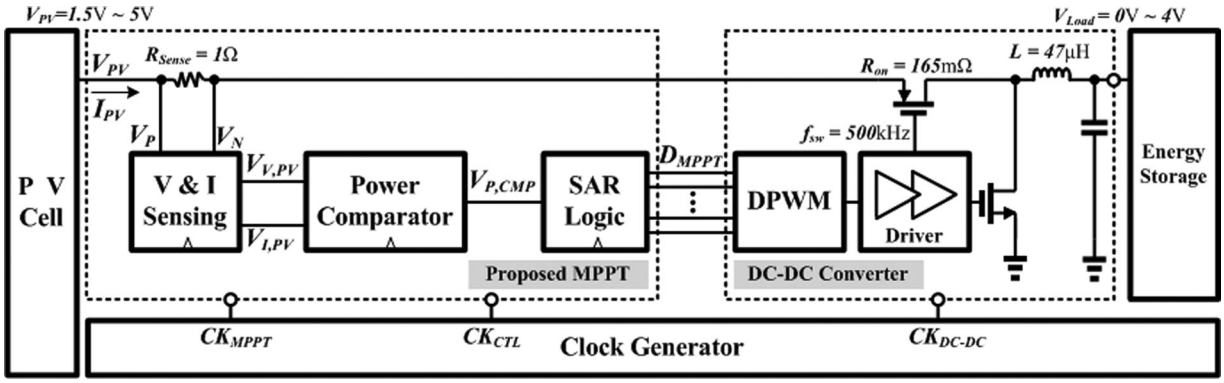

Fig. 7. Block diagram of the proposed MPPT circuit for a solar energy harvester.

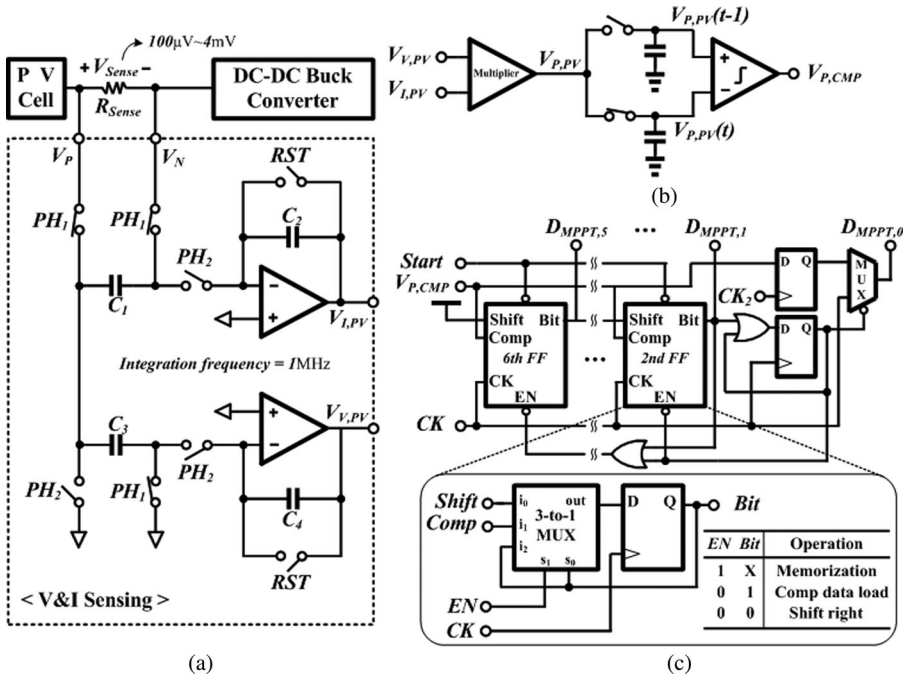

Fig. 8. Circuit diagrams of (a) voltage-and-current sensing, (b) power comparator, and (c) 6-bit SAR logic.

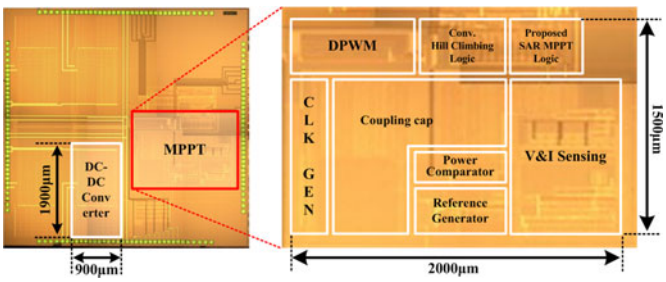

Fig. 9. Chip microphotograph.

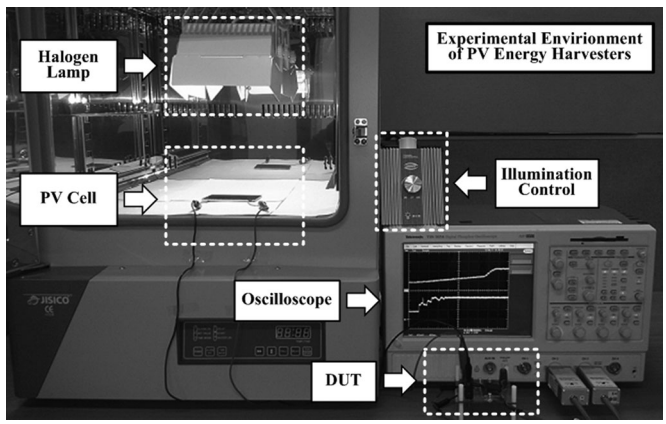

Fig. 10. Experimental environment of the PV energy harvester.

halogen lamp was used instead of solar irradiance. An a-Si PV cell with an open-circuit voltage of 5 V and short-circuit current of 30 mA at 1000 W/m^2 was used.

Fig. 11 shows the measured *I–V* curves with and without the use of MPPT. In Fig. 11(a), the operating point of the PV cell is far from the MPP and the output power of the PV cell is not at its maximum value. In Fig. 11(b), the operating point of the PV cell tracks the MPP according to the SAR MPPT algorithm; in the end, it identifies a location near the MPP.

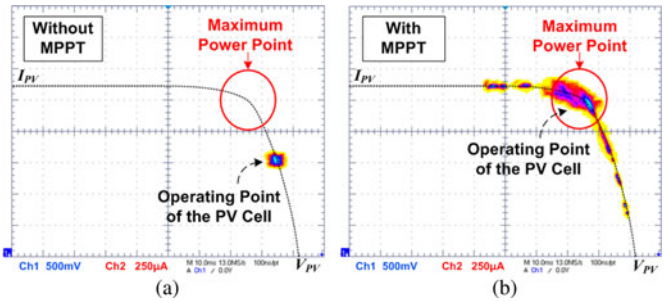

Fig. 11. Measured *I–V* curves (a) without MPPT and (b) with MPPT.

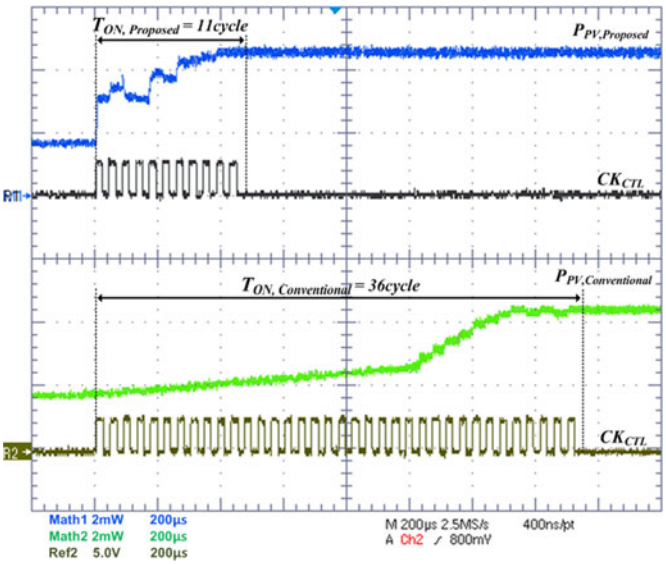

Fig. 12. Measured power tracking waveforms in active mode with the conventional MPPT and the proposed SAR MPPT.

The measured results of the operation of the proposed SAR MPPT and the conventional hill climbing algorithm in the active mode are depicted in Fig. 12. Although the conventional hill climbing algorithm tracks the MPP within 36 cycles, the proposed MPPT algorithm tracks the MPPT within 11 cycles. The PV output power does not oscillate at the MPP after the active mode, since the duty ratio of the dc–dc converter remains constant. Therefore, the proposed MPPT has faster dynamics and no oscillation around the MPP. In addition, the proposed SAR MPPT algorithm improves the MPPT efficiency during only active mode of (7) from 62.3% to 84.3%.

Measurement results of the proposed chip are summarized in Table I. The SAR MPPT circuit, which includes the voltage-and-current sensing circuit, the power comparator circuit, and the SAR logic circuit, operates only within the short active mode time and dissipates 4.6 μW of power. The proposed PV energy harvester with SAR MPPT produces 381 mJ, 1.41 J, and 10.2 J, which increase the E_{Store} by 31.4%, 5.2%, and 2%, under the indoor, cloudy outdoor, and clear outdoor conditions, respectively.

TABLE I
TEST CHIP PERFORMANCE SUMMARY

Process		0.35µm BCDMOS	
Supply voltage (V_{DD})		3 V	
Input voltage range (V_{PV})		1.5 ~ 5 V	
Output voltage (V_{Load})		0 ~ 4 V	
Power consumption of MPPT (P_{MPPT})		4.6 µW	
Performance comparison		**Conventional MPPT**	**Proposed SAR MPPT**
Tracking time (T_{ON})		36 cycles	11 cycles
MPPT efficiency during active mode ($\eta_{MPPT,Active}$)		62.3 %	84.3 %
Delivered energy (E_{Store})	Indoor	290 mJ	381 mJ
	Outdoor (Cloudy)	1.34 J	1.41 J
	Outdoor (Clear)	10 J	10.2 J

TABLE II
PERFORMANCE COMPARISON

	This work		[13]	[16]	[17]
	Conv. Hill climbing	Prop. SAR MPPT			
MPPT Processing	Analogue		Digital. DSP TMS320F28035	Analogue	Analogue
Process	0.35µm BCDMOS		N/A	0.25µm CMOS	0.35µm HV Triple-well CMOS
Rated power throughput	800µW		14.8W	1.66mW	36W
MPPT power consumption	4.6µW		N/A	3.5µW	1.3mW
Entire MPPT tracking efficiency	97.1%	99%	94.59%	< 88%	> 99%

V. CONCLUSION

An energy-efficient fast-tracking MPPT circuit for an 800-μW PV energy harvester is presented in this paper. The proposed SAR MPPT algorithm, which has a power down mode and fast tracking time, has been implemented and fabricated in 0.35-μm BCDMOS technology. The experimental results show that, under indoor conditions, the proposed SAR MPPT circuit consumes only 4.6 μW of power and reduces the tracking time by 69.4%. Moreover, the energy stored in the energy storage is increased by 31.4% and the MPPT efficiency during only active mode is improved from 62.3% to 84.3%. A performance comparison with state-of-the-art publications is shown in Table II. Consequently, the proposed circuit has sufficiently high energy efficiency for use as the WSN PV energy harvesters. Furthermore, the proposed SAR MPPT algorithm is extensible and applicable to low-power applications such as mobile and attachable medical devices.

APPENDIX

The MPPT efficiency during the active mode is given by

$$\eta_{\mathrm{MPPT,Active}} = \left.\frac{E_{\mathrm{PV}}}{E_{\mathrm{MPPT,ideal}}}\right|_{T_{\mathrm{ON}}} \tag{7}$$

where $E_{\mathrm{MPPT,ideal}}$ is the energy produced when at the ideal MPP, T_{ON} is the active mode time. As shown in Fig. 6, the MPPT efficiency during the active mode for the 4-bit conventional hill climbing algorithm and the proposed SAR MPPT algorithm is approximately 59.3% and 81.9%, respectively.

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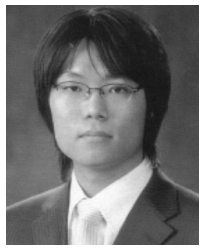

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