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## 1 Schematics and Simulation Results

The front end design including power, clamper, scaling, buffer, anti-aliasing filter and inverting level shifter is shown in figure 1.1.

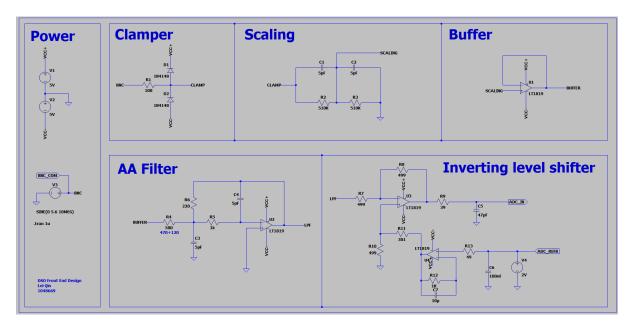


Figure 1.1: Front End design schematic.

## 1.1 Frequency response at the ADC input

The magnitude and phase response at the ADC input are shown in figure 1.2 and figure 1.3. The magnitude at 1Hz and 18.72MHz are about -14.68dB and -17.67dB. Thus , the cut off frequency is about 18.72MHz. The phase at 18.72MHz is about  $-73.755^{\circ}$  which is larger than  $-180^{\circ}$ . The response is of more than 20dB per decade and less than 2dB ripple.

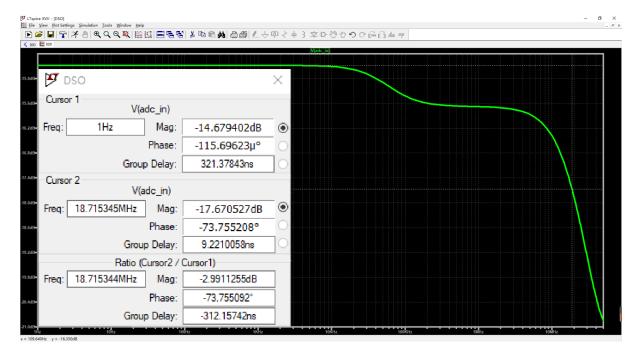
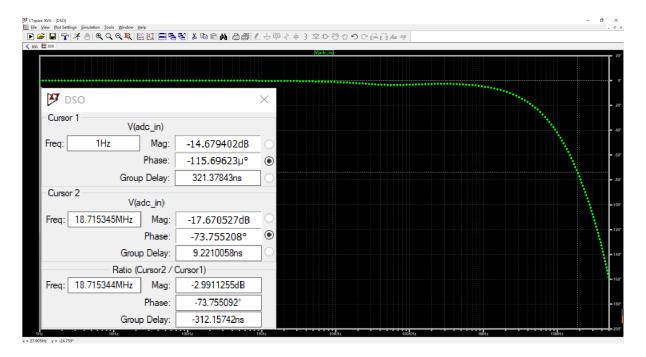


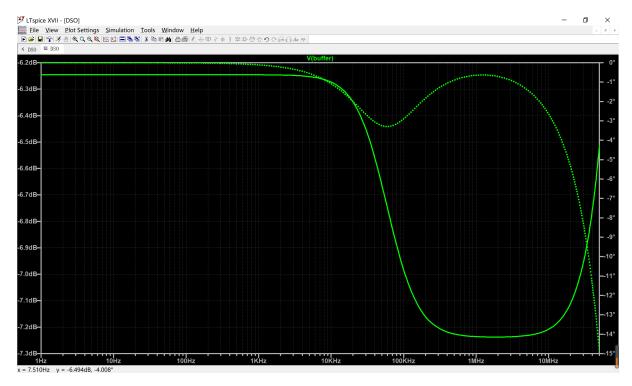
Figure 1.2: Magnitude response at the ADC input.



**Figure 1.3:** Phase response at the ADC input.

## 1.2 Frequency response at the input to the anti-aliasing filter

The frequency response at the input to the anti-aliasing filter is shown in figure 1.4.



**Figure 1.4:** Frequency response at the input to the anti-aliasing filter.

#### 1.3 Input impedance at the BNC

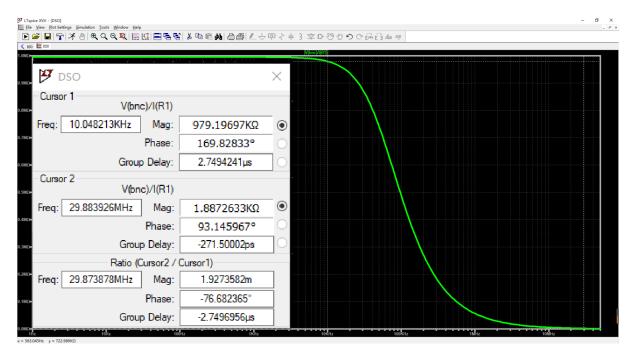
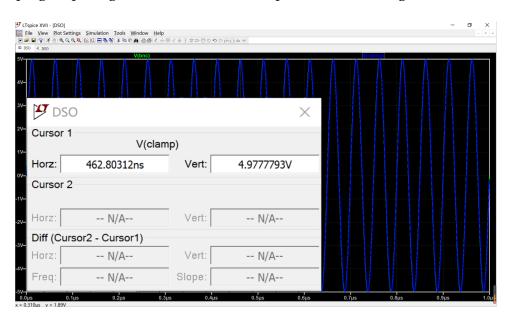


Figure 1.5: Input impedance at the BNC.

The input impedance at the BNC is shown in figure 1.5. We can the input impedance from DC to 10kHz is at least  $0.979M\Omega$ ; the input impedance from 10kHz to 30MHz is at least

## 1.4 Clamper

The clamping output signals with 5V and 10V input are shown in figure 1.6 and 1.7.



**Figure 1.6:** Clamping circuit with 5 V input.

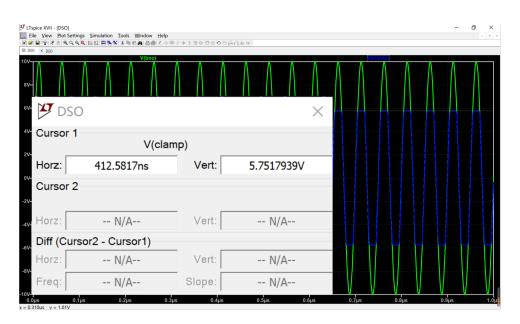


Figure 1.7: Clamping circuit with 10 V input.

#### 1.5 Power dissipation

Given that the device must draw less than 150mA per rail when running a maximum sampling rate, the maximum power at 5V is:

$$P_{max} = 150m \times 5 = 750mW$$

From the operating point information in Appendix and the formulation for power consumption of Op-Amp in figure 1.8, we can calculate the total power dissipation in figure 1.9 is about  $387.964\,mW$  which is less that than the requirement.

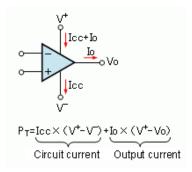


Figure 1.8: Power consumption of Op-Amp.

Component	Vo	lo	Icc	Max power consumed (mW)
Component				(5.6V, 20MHz)
Buffer OpAmp (U1)	0.497	-8.581E-04	9.05E-03	86.671
AA Filter OpAmp (U2)	-0.192	3.741E-03	9.43E-03	113.705
ADC In OpAmp (U3)	2.681	-2.877E-03	9.38E-03	87.126
Level Shifter OpAmp (U4)	1.997	2.494E-03	9.30E-03	100.462
Sum				387.964

Figure 1.9: Power dissipation table.

## 1.6 10 kHz input signal at the input to the ADC

The input to the ADC in time domain with  $10 \, \text{kHz} \, 5.6 V$  input signal is shown in figure 1.10. We can see the signal goes from 1.834 V to 3.529 V.

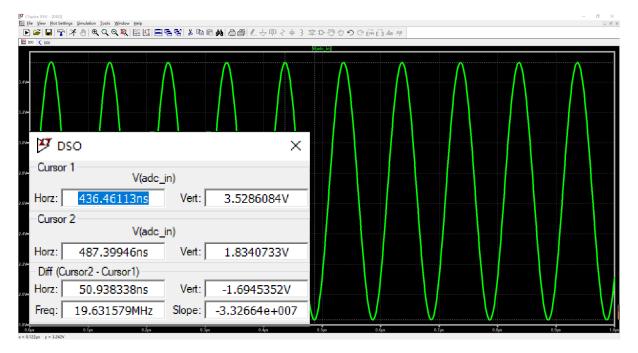


Figure 1.10: Time domain 10 kHz input signal at the input to the ADC.

## 2 Discussion

#### 2.1 Power Block

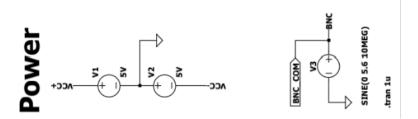


Figure 2.1: Power.

 $V_{cc+} = 5V$ ,  $V_{cc-} = -5V$ . The input signal is through a BNC connector.

### 2.2 Clamper Block

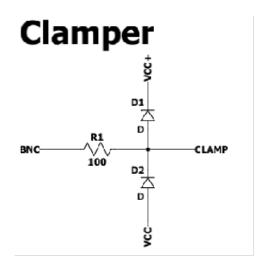
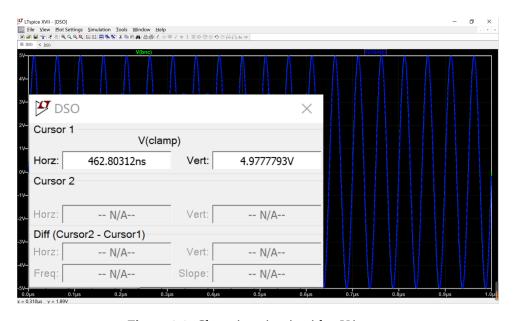


Figure 2.2: Clamper.

The BNC input can accept a maximum input of  $\pm 5.6V$  after which the input voltage is clamped. The clamper circuit is to protect the front end circuit by clipping the input signal if it exceeds  $\pm 5.6V$ .

Resistor  $R_1 = 100\Omega$  is to absorb the divided voltage when clamping. A small value is chosen because when there is a high frequency input signal, the total impedance would become very small which would increase the total current of the circuit. Since we do not want many voltages drop on  $R_1$ , we need to choose a small value for that.

The clamping output signals with 5V and 10V input are shown in figure 2.3 and 2.4. We can see if the magnitude of input is larger than 5.6V, it would be clamped by this part circuit to around 5.6V.



**Figure 2.3:** Clamping circuit with 5 V input.

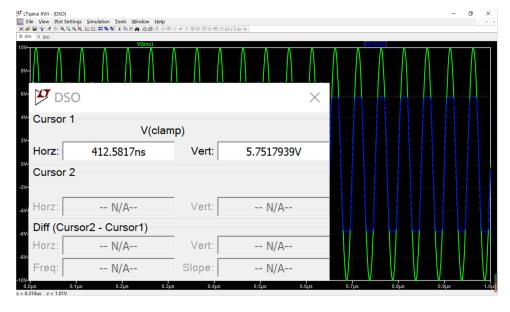


Figure 2.4: Clamping circuit with 10 V input.

#### 2.3 Scaling Block

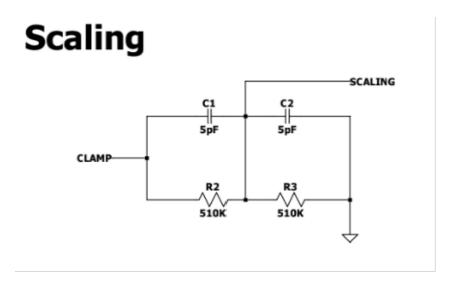


Figure 2.5: Scaling.

The scaling circuit is to provide enough impedance for the whole circuit and scale the input signal for later use.

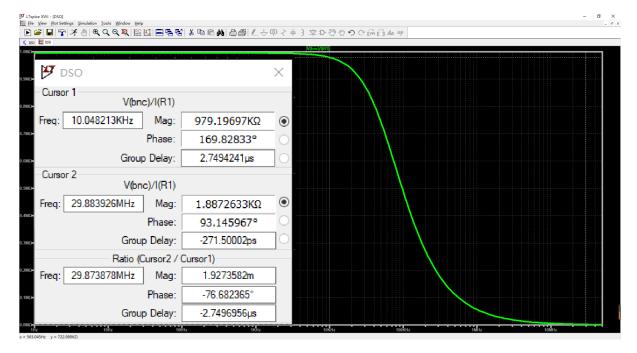
 $R_2 = R_3 510 k\Omega$ ,  $C_1 = C_2 = 5 pF$  are to ensure the input has a  $1M\Omega \pm 10\%$  input impedance from DC to 10 kHz and at least  $100\Omega$  input impedance from 10 kHz to 30 MHz. The total impedance can be calculated by:

$$Z_{total} = (X_{C1}||R_2) + (X_{C2}||R_3)$$

For 10kHz:  $Z_{total} = 2 * (\frac{1}{2\pi f C_1} || R_2) \approx 1.02M\omega$ ;

For 30MHz:  $Z_{total} = 2 * (\frac{1}{2\pi f C_1} || R_2) \approx 2.12 k\omega$ .

The input impedance at the BNC is shown in figure 2.6. We can the input impedance from DC to 10kHz is at least  $0.979M\Omega$ ; the input impedance from 10kHz to 30MHz is at least  $1.887k\Omega$ .



**Figure 2.6:** Input impedance at the BNC.

Additionally,  $C_1 = C_2 = 5pF$  is chosen to ensure that the input capacitance is less than 60pF.

Then the input signal is halved after the scaling circuit shown in figure 2.7

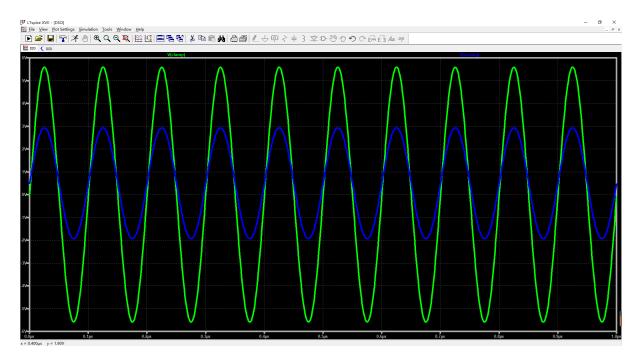


Figure 2.7: Scaling v.s. Camping.

#### 2.4 Buffer Block

# **Buffer**

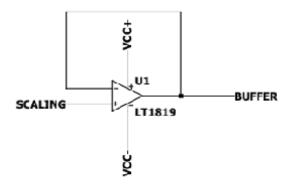
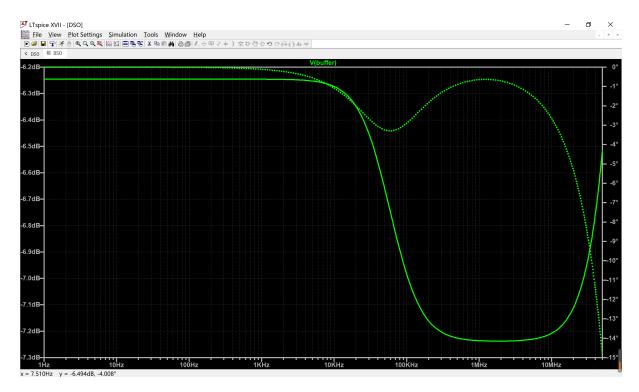


Figure 2.8: Buffer.

The buffer is used to decouple the front and back circuits. So it can keep the impedance of the previous design unchanged.

The frequency response at the input to the anti-aliasing filter is shown in figure 2.9.



**Figure 2.9:** Frequency response at the input to the anti-aliasing filter.

#### 2.5 Anti-aliasing Filter

## **AA Filter**

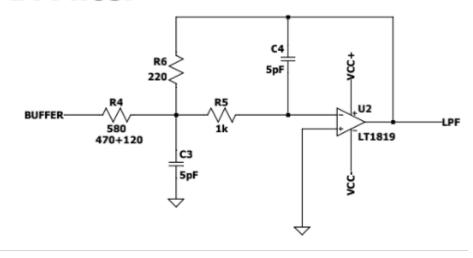


Figure 2.10: AA Filter.

The anti-aliasing filter is designed as a multiple feedback low-pass filter (2nd order Butterworth). The cut off frequency is designed as 20MHz to prevent alising of the input signal. The DC Amplitude of the circuit is designed to satisfy the requirement of ADC input  $V_{pp} = 2V$  with  $\pm 2dB$  maximum ripple.

We use online low-pass filter design tool with requirements to get initial values for components, then continue to tune these values to meet all requirements: 1)  $f_o = 20MHz$ , 2)  $H = \frac{2}{5.6} = 0.3571$ , 3)  $\pm 2dB$  maximum ripple in passband and 4) values from BOM list.

Finally,  $R_4 = 580\Omega$ ,  $R_5 = 1k\Omega$ ,  $R_6 = 220\Omega$  and  $C_3 = C_4 = 5pF$ . The magnitude and phase response at the ADC input are shown in figure 2.11 and figure 2.12. The magnitude at 1Hz and 18.72MHz are about -14.68dB and -17.67dB. Thus , the cut off frequency is about 18.72MHz. The phase at 18.72MHz is about  $-73.755^{\circ}$  which is larger than  $-180^{\circ}$ . The response is of more than 20dB per decade and less than 2dB ripple.

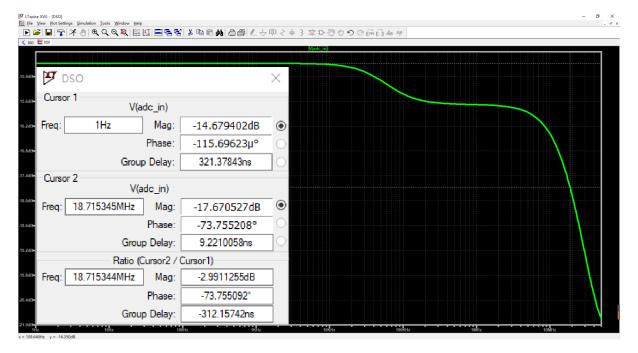
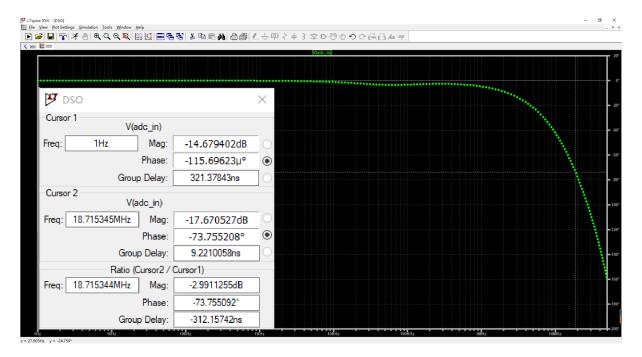


Figure 2.11: Magnitude response at the ADC input.



**Figure 2.12:** Phase response at the ADC input.

The output with 10MHz and 5.6V input signal before and after the anti-aliasing filter is shown in figure 2.13.

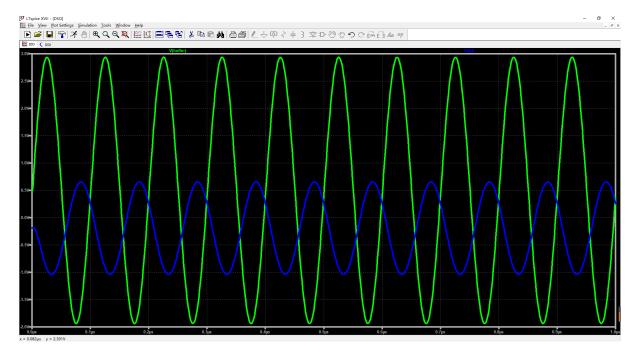


Figure 2.13: LPF v.s. Buffer.

### 2.6 Inverting Level Shifter Block

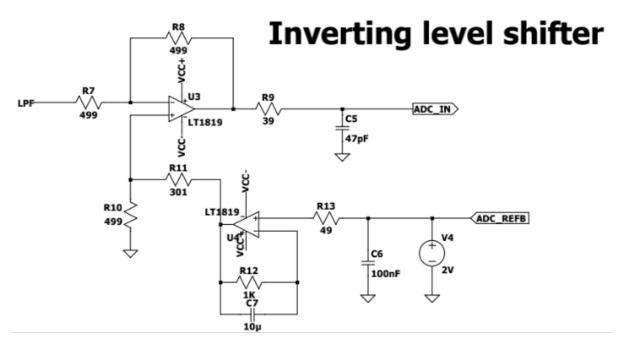
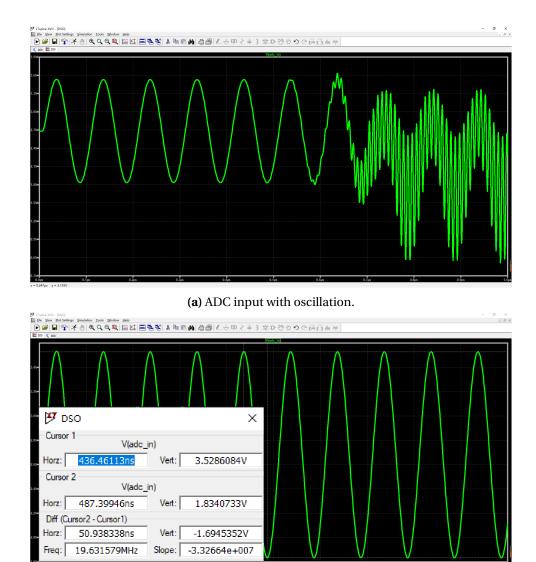


Figure 2.14: Inverting Level Shifter.

The inverting Level Shifter is designed from ADS830E data sheet with  $C_7$  to prevent the high frequency oscillation, the output signal comparison is shown in 2.15.



(b) ADC input without oscillation.

**Figure 2.15:** Comparison of circuits with or without  $C_7$ 

## 3 Observation

All core requirements are satisfied and discussed in last section. Since there might be a DC offset due to OpAmps in the final design, we can add trim pots to adjust that.

# 4 Summary

The performance can be expected that: 1) Signal from DC to 1MHz would be presented well; 2) Signal from 1MHz to 20MHz would be shifted in phase; 3) Signal larger than 20MHz could not be presented.

## **Appendix**

#### **Operating point**

```
* C:\Users\cassi\Desktop\EISD\DSO Project\DSO_LTSpice\DSO.asc
                                                                                     ×
       --- Operating Point ---
V(vcc+):
                             voltage
V(vcc-):
               -5
                             voltage
V(bnc):
               n
                             voltage
               9.74625e-005 voltage
V(clamp):
V(scaling): 0.497156
                             voltage
V(buffer):
             0.496935
                             voltage
V(n008):
              -0.0018872
                             voltage
              0.000112141
V(n009):
                             voltage
V(n005):
             1.24503
                             voltage
V(lpf):
               -0.191535
                             voltage
              2.68066
V(n006):
                             voltage
V(adc in):
             2.68066
                             voltage
V(n007):
              1.24623
                             voltage
              1.9974
V(n010):
                             voltage
V(n012):
               1.9992
                             voltage
V(n011):
               2.00009
                             voltage
V(adc_refb): 2
                             voltage
I(C4):
              9.58238e-025 device current
              1.80057e-020 device_current
I(C7):
              2e-019
                             device_current
I(C6):
               1.25991e-022 device current
I(C5):
               -9.43599e-027 device current
I(C3):
              -2.48578e-024 device current
I(C2):
I(C1):
             2.48529e-024 device current
              -5.0101e-012 device_current
-5.0099e-012 device_current
I(D2):
I(D1):
I(R6):
              0.000862037
                             device current
              1.7981e-006 device_current
I(R13):
              -1.80057e-006 device current
I(R12):
I(R11):
              -0.00249558 device current
I(R10):
               -0.00249745 device_current
I(R9):
                             device_current
I(R8):
              0.00287702
                             device current
             0.00287889
I(R7):
                             device_current
I(R5):
              1.99934e-006 device current
              -0.000860038 device_current
I(R4):
               -9.74816e-007 device_current
I(R3):
I(R2):
               9.74625e-007 device current
              9.74625e-007 device_current
I(R1):
I(V4):
              1.7981e-006
                             device current
I(V3):
               9.74625e-007
                             device current
               -0.0359076
I(V2):
                             device_current
               -0.0384107
I(V1):
                             device current
```

**Figure 1:** Operating point 1.

```
* C:\Users\cassi\Desktop\EISD\DSO Project\DSO_LTSpice\DSO.asc
                                                                                             \times
                -1.94944e-006 subckt_current
Ix(u1:1):
                                                                                              \wedge
Ix(u1:2):
                 -1.95005e-006 subckt current
Ix (u1:3):
                -0.000858088 subckt current
                0.00948449
                                subckt_current
Ix(u1:4):
                -0.00862251
Ix(u1:5):
                                subckt_current
                -1.87316e-006 subckt_current
-1.87647e-006 subckt_current
Ix(u3:1):
Ix(u3:2):
                -0.00287702 subckt current
Ix(u3:3):
Ix (u3:4):
                0.0108203
                               subckt current
                -0.00793954 subckt_current
-1.7981e-006 subckt_current
Ix(u3:5):
Ix (u4:1):
Ix(u4:2):
                -1.80057e-006 subckt current
                -0.00249378 subckt_current
Ix(u4:3):
Ix (u4:4):
                0.0105461
                                subckt current
                -0.00804876
                               subckt_current
Ix(u4:5):
Ix (u2:1):
                -1.99965e-006 subckt_current
Ix(u2:2):
                -1.99934e-006 subckt_current
Ix(u2:3):
                0.00374093
                                subckt_current
                0.0075599
Ix(u2:4):
                                subckt current
Ix(u2:5):
                 -0.0112968
                                subckt current
```

Figure 2: Operating point 2.