## 6.4 A 4nm 32Gb/s 8Tb/s/mm Die-to-Die Chiplet Using NRZ Single-Ended Transceiver With Equalization Schemes And Training Techniques

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Recently, the demand for multi-chip solutions, such as chip-on-wafer-on-substrate (CoWoS) and embedded multi-die interconnect bridge (EMIB), is increasing as they reduce chip size and cost for high-performance computing (HPC), artificial intelligence (AI), and big data applications [1]. Following this trend, the industry is establishing standard specifications for die-to-die interfaces, such as Universal Chiplet Interconnet Express (UCIe) and Open High-Bandwidth Interface (OpenHBI), and developing various chiplets with high data transmission bandwidth per unit width, low latency, and low power consumption [2-5]. This work implements a die-to-die (D2D) chiplet compatible with the UCIe specification using 2.5D packaging technology for die-to-die communication. A transmitter (TX) adopts a reflection-cancellation driver (RCD) that cancels the reflections caused by the impedance mismatch in case of not using an on-die termination of a receiver (RX). Also, a TX clock phase training scheme is implemented to achieve low latency with a synchronous reset generator. As for the RX, a direct decision-feedback equalizer (DFE) combined with a double tail latch compensates for the inter-symbol interference (ISI) while reducing its feedback time even at the high-speed operation. All necessary circuits for the offset calibration, the duty-cycle distortion, and the skew calibration are fully implemented in digital to eliminate static power consumption. This transceiver in 4nm FinFET CMOS technology operates at 32Gb/s/wire with 0.44pJ/b energy efficiency and shows 8Tb/s/mm beach-front bandwidth.

Figure 6.4.1 shows the 2.5D package structure of the D2D. Each chiplet has the D2D stacked in two rows to achieve higher total beach-front bandwidth, and each D2D consists of 4 slices of TX and RX. Each slice of the TX and the RX consists of 39 DQs and a DQS, which operate up to 32Gb/s. Every channel has an equal length to minimize the skew among channels, connecting the inner transceiver in chiplet1 to the outer transceiver in chiplet2. The number of metal layers required for the interposer is determined by the amount of transmitted data, the channel characteristics, and the length of die edge [5]. Logic circuits for training are implemented in the PCS layer of the D2D; the offset calibration logic achieves better voltage margin, and the skew calibration increases the timing margin in the RX sense amplifier. Also, data bus inversion encoders and decoders reduce the simultaneous switching noise. In addition, the lane repair function improves the reliability by lowering the yield loss caused by defects.

Figure 6.4.2 shows the implemented single-ended NRZ transmitter and receiver architecture of the D2D PHY. The D2D PHY adopts a source-synchronous architecture and has 39 DQs for data and a DQS for strobe clock in the slice of TX and RX. The TX includes low-swing output drivers for low power consumption; the output drivers consist of the push-pull NMOS-type voltage-mode driver for low swing and the reflection cancellation driver to eliminate the reflected waves. The DQS of the TX includes a synchronous reset generator (TX SYNC GEN) for low latency; by using the TX SYNC GEN, a FIFO used for the asynchronous interface of each DQ can be eliminated. As a result, the latency is also reduced. The RX includes a DFE that can operate at high-speed and de-skew circuits to align the clock with the data from the TX. The DQs and DQS of RX include local de-skew circuits and global de-skew circuits, respectively. The local and global de-skew circuits are implemented for per-bit and per-slice de-skew respectively so that they can be used depending on different data rates. At low data rates with sufficient timing margin, the global de-skew circuits are used to save power consumption; they consist of NAND-based coarse delay lines and phase-interpolator-based fine delay lines. The combination of the two delay lines can improve resolution while operating seamlessly. One of the 39 DQs is used for the periodic skew calibration (PSC) to compensate for the skew between the data and clock due to either voltage or temperature variations. The DQs for data align the clock to the center of the data from the TX, while the DQ for PSC aligns the clock to the edge of the data from the TX and tracks the change between the data and the clock due to either voltage or temperature variations. The DQ for PSC uses the clock pattern as TX data input (TXDATA[15:0]).

The synchronous reset generator (sync gen) for TX clock phase training is shown in Fig. 6.4.3. The purpose of the TX clock phase training is to find an optimal clock phase for the sampling data transmitted from the asynchronous clock domain; a FIFO was used to capture the data, which resulted in additional latency in a previous work [1]. Instead of shifting the clock directly in the TX clock phase training, the D2D shifts the reset signal used by the divider of each DQ to find the optimal clock position for data capturing. The reset signal is shifted by psel[1:0]; the shift range is $T_{async\_clk} + N \times 4UI$. By sweeping all the psel values, the psel code which generates the clock with the most timing margin is selected. The TX clock phase training can reduce latency to one cycle by eliminating the FIFO. A circuit diagram of the reflection cancellation driver (RCD) is shown in Fig. 6.4.3. Due to the impedance mismatch in the interposer, the input at the RX (RX PAD) can see the reflected waves on the transition. To eliminate the effect of reflected waves on the RX PAD, the D2D uses the reflection cancellation driver (RCD). A pre-driver in the RCD finds a compensation location to effectively remove a distorted signal due to the reflected waves.

Fig. 6.4.4 shows the implemented direct decision-feedback equalizer. In general, the direct DFE is limited in its operating speed due to the feedback time ($T_{fb}$). A look-ahead DFE or loop-unrolled DFE architecture that mitigates the limitation from the feedback time has been used in previous work. However, the loop-unrolled DFE has disadvantages in size and power consumption compared to the direct DFE. The D2D proposes a direct DFE combined with a double-tail latch for high data rate operation. In previous work [6], the feedback data (E_OP/E_ON, O_OP/O_ON) is connected to the first latch to compensate for ISI; the feedback time ($T_{fb}$) of the DFE is required to be less than 1UI for proper operation. In the implemented DFE, the feedback data (E_OP/E_ON and O_OP/O_ON) are connected to the gate of the pull-down transistor of the second latch (M1, M2). The implemented scheme is used to compensate for ISI by controlling the pull-down strength of the second latch. When ISI is present in the input signal of the RX (RX_PAD), the differential input from the first stage of the slicer becomes small, which slows down the second stage decision. The DFE feedback of the second stage slicer helps speed up the second stage operation. The control circuits for calculating the DFE coefficient are fully implemented in digital, eliminating static current.

The measurement results of the D2D with interposer channel at 32Gb/s are shown in Fig. 6.4.5. In order to monitor the TX eye-diagram, we also designed a 2D package using the D2D and measured TX eye-diagram. A measured eye-diagram at 32Gb/s with a 24.2ps/90mV margin shows that the implemented TX operates up to 32Gb/s as well. The measured eye-diagram is a waveform, which reflects the characteristics of the package, probe card and the internal VSS termination of the equipment. The post processing on-chip eye diagram of the D2D in a 2.5D package at 32Gb/s shows the horizontal/vertical eye-opening of 16ps/170mV.

The performance summary is shown in Fig. 6.4.6. The D2D is implemented in 4nm CMOS FinFET technology for a 2.5D package with silicon interposer. The D2D operates up to 32Gb/s/wire with 3mm silicon interposer channels. The channel loss is -4dB at 16GHz. The D2D achieves the best beach-front bandwidth and figure-of-merit (FoM) compared to previous works. The testchip micrograph with the interposer in a 2.5D package is shown in Fig. 6.4.7.

*References:*

[1] M.-Shan Lin et al., "A 7nm 4GHz Arm-core-based CoWoS Chiplet Design for High Performance Computing," *IEEE Symp. VLSI Technology*, pp.C28-C29, July 2019.

[2] K. McCollough et al., "A 480Gb/s/mm 1.7pJ/b Short-Reach Wireline Transceiver Using Single-Ended NRZ for Die-to-Die Application," *ISSCC*, pp.184-185, Feb. 2021.

[3] G. Gangasani et al., "A 1.6Tb/s Chiplet over XSR-MCM Channels using 113Gb/s PAM-4 Transceiver with Dynamic Receiver-Driven Adaptation of TX-FFE and Programmable Roaming Taps in 5nm CMOS," *ISSCC*, pp.122-123, Feb. 2022.

[4] Y-Y. Hus et al., "A 7nm 0.46pJ/bit 20Gbps with BER 1E-25 Die-to-Die Link Using Minimum Intrinsic Auto Alignment and Noise-Immunity Encode," *IEEE Symp. VLSI Technology*, pp. JFS1-3, June 2021.

[5] Y. Nishi et al., "A 0.297-pJ/bit 50.4-Gb/s/wire Inverter-Based Short-Reach Simultaneous Bidirectional Transceiver for Die-to-Die Interface in 5nm CMOS," *IEEE Symp. VLSI Technology*, pp.154-155, June 2022.

[6] J. Seo et al., "A 7.8-Gb/s 2.9-pJ/b Single-Ended Receiver With 20-Tap DFE for Highly Reflective Channels," *IEEE TVLSI*, pp.818-822, March 2020.

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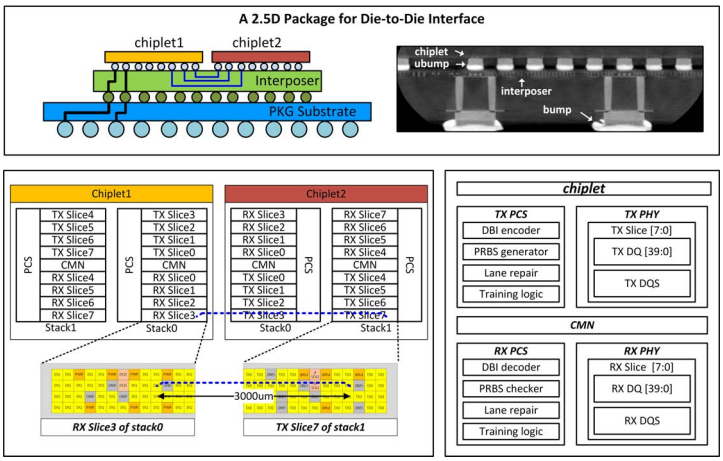



**Figure 6.4.1: Implemented die-to-die (D2D) chiplet.**

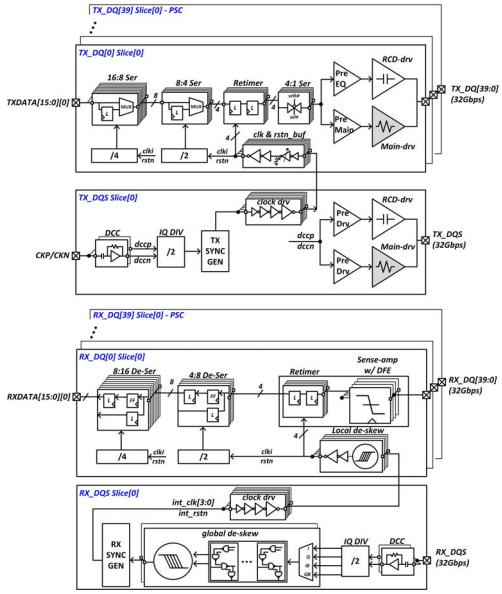



**Figure 6.4.2: Implemented TX and RX of the D2D PHY.**

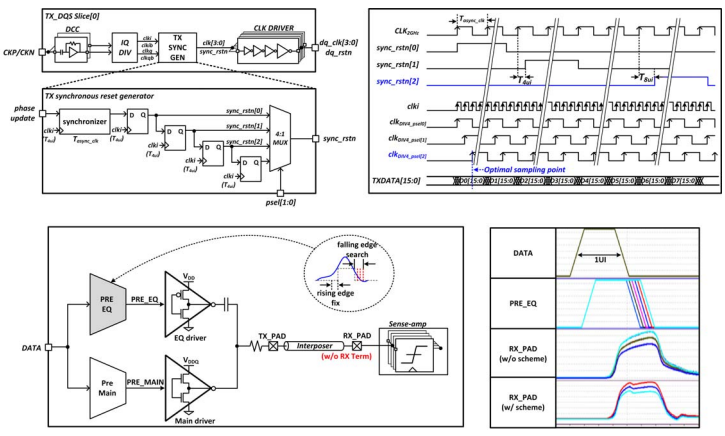



**Figure 6.4.3: The implemented TX scheme: TX synchronous reset generator and reflection-cancellation driver (RCD).**

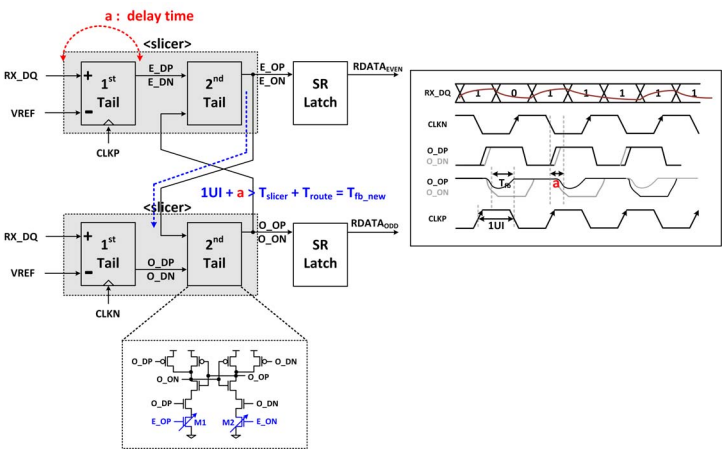



**Figure 6.4.4: Conceptual view of the implemented direct decision-feedback equalizer.**

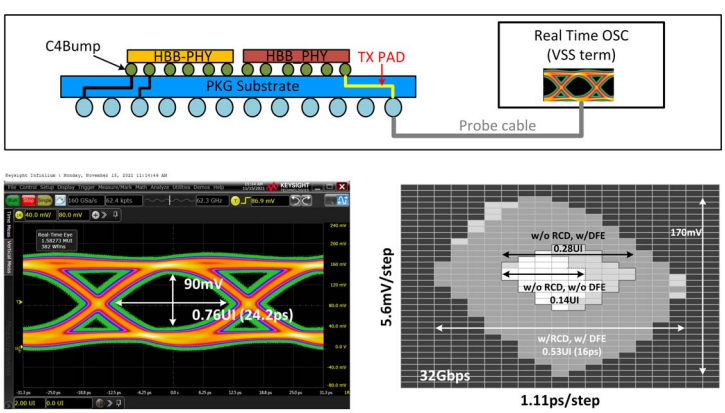
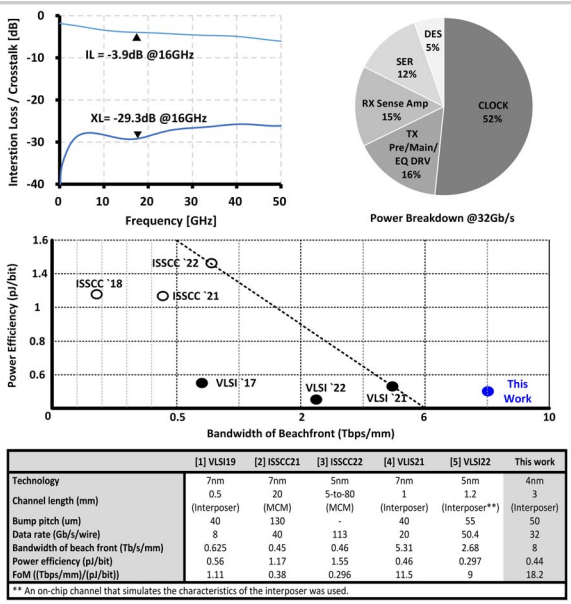



**Figure 6.4.5: Measured TX eye-diagram at 32Gb/s and post-processing on-chip eye diagram at 32Gb/s.**




| | [1] VLSI19 | [2] ISSCC21 | [3] ISSCC22 | [4] VLSI21 | [5] VLSI22 | This work |
|---|---|---|---|---|---|---|
| Technology | 7nm | 7nm | 5nm | 7nm | 5nm | 4nm |
| Channel length (mm) | 0.5 (Interposer) | 20 (MCM) | 5-to-80 (MCM) | 1 (Interposer) | 1.2 (Interposer**) | 3 (Interposer) |
| Bump pitch (um) | 40 | 130 | - | 40 | 55 | 50 |
| Data rate (Gb/s/wire) | 8 | 40 | 113 | 20 | 50.4 | 32 |
| Bandwidth of beach front (Tb/s/mm) | 0.625 | 0.45 | 0.46 | 5.31 | 2.68 | 8 |
| Power efficiency (pJ/bit) | 0.56 | 1.17 | 1.55 | 0.46 | 0.297 | 0.44 |
| FoM ((Tbps/mm)/(pJ/bit)) | 1.11 | 0.38 | 0.296 | 11.5 | 9 | 18.2 |

** An on-chip channel that simulates the characteristics of the interposer was used.

**Figure 6.4.6: Performance summary.**

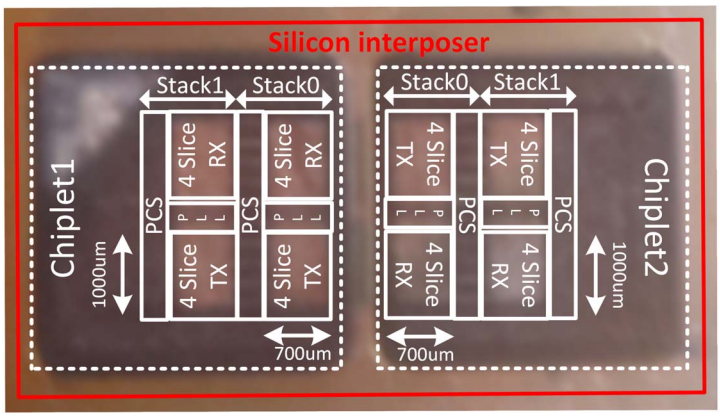



**Figure 6.4.7: Testchip micrograph with the interposer in a 2.5D package.**

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