An Electrical–Thermal Co-Simulation Model of Chiplet Heterogeneous Integration Systems

Xiaoning Ma, Qinzhi Xu, Chenghan Wang, *Graduate Student Member, IEEE*, He Cao, Jianyun Liu, Daoqing Zhang, and Zhiqiang Li, *Member, IEEE*

***Abstract*— Chiplet heterogeneous integration (CHI) is one of the important technology choices to continue Moore's law. However, due to the characteristics of high power and low supply voltage in CHI systems, heavy currents need to flow through the power delivery network (PDN), and the Joule heating effect will result in the overall temperature increase of the CHI system. Meanwhile, the high temperature will cause the current as well as the performance of the system to degrade and a series of reliability problems will occur. In this article, an effective electrical–thermal coupling model is proposed to predict the steady-state temperature distribution of a 2.5-D CHI system considering the Joule heating effect and the temperature effect on the IR drop. The equivalent electrical conductivity model is also built up to describe the design features of the redistribution layer (RDL), bump, and through silicon via (TSV) structures based on the electrical–thermal duality. Furthermore, the governing equations for voltage distribution and temperature distribution are solved simultaneously by utilizing the finite volume method (FVM) with nonuniform mesh to realize the electrical–thermal co-simulation of the multiscale CHI system. The model application is further performed to investigate the influence of the model parameters on the voltage drop and temperature distribution of the CHI system. The verified systems and simulated results of the present investigation demonstrate the viability and accuracy of voltage and temperature field co-simulation and indicate that the new proposed electrical–thermal model is helpful in thermal and voltage drop analysis of packaging structures with the Joule heating effect and can be adopted to assist in the physical design optimization of 2.5-D CHI or 3-D heterogeneous stacked chips.**

***Index Terms*— Chiplet heterogeneous integration (CHI) system, electrical–thermal co-simulation, equivalent electrical conductivity, finite volume method (FVM).**

I. Introduction

MOORE'S law states that the integration level of integrated circuits (ICs) will increase periodically. Since the 1990s, with the development of technology, the maturity of the manufacturing process, and the improvement of EDA tools, system-on-chip (SoC) has gradually become the main form of IC design [1], [2], [3], [4]. However, as the package density continues to increase, SoCs become more and more expensive as they migrate to more advanced process nodes, and it is difficult for Moore's law to continue [5]. Chiplet heterogeneous integration (CHI) is a technology that heterogeneously integrates chips through an advanced packaging process methodology, as shown in Fig. 1. The multiple chiplets are electrically connected through a redistribution layer (RDL) of silicon interposer and then through silicon via (TSV) structure to realize the system pinout [6], [7], [8].

The core idea of chiplet design is first to split the functional modules into a single chip and then integrate them into a large single chip through advanced packaging modules. Compared with SoC, chiplet has the following advantages [9], [10].

1) The individual chip can be made smaller and the appropriate process can be selected accordingly.
2) The chiplet can be reused in different products, which improves the scalability of chip design and accelerates the iteration speed of the chip to the market.
3) Chiplet technology allows for the integration of multiple cores, thus meeting the needs of high-performance computing processors.
4) Compared with the advanced semiconductor process, chiplets have lower costs.

In recent years, limited by the manufacturing ability of advanced lithography equipment and materials, the technology of packaging and integrating the processing chip with the memory chip in the form of chiplets has become increasingly important [10]. Intel[1], Samsung, and other manufacturers have released related products, which provide customized packages for the processor chip and the memory chip through the I/O interface of high density and narrow pitch to cope with the need for high-performance computing, artificial intelligence, and other cutting-edge industries. The advanced packaging

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Xiaoning Ma, Qinzhi Xu, Chenghan Wang, and Zhiqiang Li are with the Institute of Microelectronics and the Key Laboratory of Fabrication Technologies for Integrated Circuits, Chinese Academy of Sciences, Beijing 100045, China, also with the School of Integrated Circuits, University of Chinese Academy of Sciences, Beijing 101408, China, and also with Beijing Key Laboratory of Three-Dimensional and Nanometer Circuit Design Automation Technology, Beijing 100029, China (e-mail: maxiaoning@ime.ac.cn; xuqinzhi@ime.ac.cn; wangchenghan@ime.ac.cn; lizhiqiang@ime.ac.cn).

He Cao, Jianyun Liu, and Daoqing Zhang are with the Institute of Microelectronics and the Key Laboratory of Fabrication Technologies for Integrated Circuits, Chinese Academy of Sciences, Beijing 100045, China, and also with Beijing Key Laboratory of Three-Dimensional and Nanometer Circuit Design Automation Technology, Beijing 100029, China (e-mail: caohe@ime.ac.cn; liujianyun@ime.ac.cn; zhangdaoqing@ime.ac.cn).

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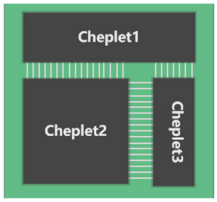


Fig. 1. CHI system.

technology requires extensive use of TSVs, microbumps, and RDLs, which results in insignificant challenges for the heat dissipation of the CHI system [11]. One side of the chiplet is usually used for electrical connections, and the other side of the chiplet is utilized for heat dissipation. The heat dissipation paths are relatively limited. In addition, the high power and low supply voltage of the CHI system require high current flowthrough the power delivery network (PDN), and the Joule heating effect will cause the temperature of the overall system to rise, which becomes an important contributor to the voltage drop in the PDN at the package level. The high temperature will cause the temperature-dependent electrical resistivity to vary as well as the system performance to degrade and a series of reliability problems will occur in the CHI system. Overall, the mutual coupling of electrical and thermal effects becomes increasingly significant for the interconnects and will further deteriorate the working environment of the CHI system [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30].

Thus, it is quite important to establish an electrical–thermal coupling simulation model and computational methods to capture the Joule heating effect for the CHI system [12]. Based on the computational fluid dynamics method in heat transfer, Lau and Yue [13] extract the lateral and longitudinal equivalent thermal conductivities in a 3-D IC system. Chen and Pan [14] proposed analytical solutions for the steady-state and transient thermal conductivities of 3-D ICs. Shiyanovskii et al. [15] proposed an analytical model for 3-D chips based on orthogonal functional forms, in which inhomogeneous electrical heating was considered. Min et al. [16] used an equivalent circuit and an equivalent conductivity model to simulate the electrical–thermal coupling of a TSV structure. Lu and Jin [17], [18] performed heat flow simulations and electrical–thermal coupling simulations of simple three-layer-plate structures as well as TSV arrays using the FETI method. Haiyan et al. [19] conducted an electrical–thermal co-simulation of a low-profile fine-ball ball grid array (LFBGA) using ANSIS. Chai et al. [31] proposed a steady-state electrical–thermal coupling method for TSV arrays based on the geometrical structure and physical parameters of TSVs and also carried out a study on the thermal crosstalk problem of TSV arrays.

Although the mentioned models and tools have effectively analyzed the thermal flow or electrical–thermal coupling effects of certain structures within the system, none of them have conducted a comprehensive electrical–thermal co-simulation at the packaging level for 2.5-D CHI systems. In addition, *HotSpot* adopts the finite-difference method (FDM) to build a compact thermal model and exhibits some discrepancies in temperature profiles when extending from 2-D to 3-D systems [26]. As for the design of heat sinks, the treatment for *HotSpot* is relatively coarse, leading to computational model accuracy loss. To improve simulation accuracy, the detailed heat sink structure needs to be provided. Moreover, *HotSpot* and other thermal models mentioned in the literature review of the present article do not provide equivalent methods of interconnect structures. Finally, the previous existing literature on equivalent thermal conductivity models primarily focuses on individual TSV without considering the effects of TSV arrays and bumps. In addition, Min et al. [16] used an equivalent circuit and an equivalent conductivity model to simulate the electrical–thermal coupling mechanism of a TSV structure. However, it lacks an equivalent electrical conductivity method for bumps and RDL structures. Thus, it is necessary to establish an electrical–thermal coupling model to achieve package-level thermal and voltage drop co-simulation of the CHI system with high efficiency and high accuracy.

In this article, we consider the physical and geometric parameters of individual TSV, bump, and RDL structures, and developed equivalent parameter models for TSV arrays, bump arrays, and RDL. Ultimately, we have developed an electrical–thermal model to simulate the Joule heating behavior of CHI systems. Compared with the 3-D IC, the design architecture, the heat dissipation path, and the boundary conditions of the CHI system are different. Accordingly, the simulation method also has some differences. We construct the present electrical–thermal co-simulation model according to the detailed architecture of the CHI system with model equivalence of parameters of different materials. Meanwhile, the effect of heat sinks has also been considered rather than treating them as having a constant ambient temperature. Moreover, our model supports inputting geometric parameters, material properties, and model parameters of each component for the CHI system. For example, the number and specific power of chiplets, quantities of TSVs and bumps, geometrical parameters of RDL, and heat transfer coefficient. The contributions of the present electrical–thermal coupling model are listed as follows.

1) As for the design architecture of the CHI system, we have derived the complete discrete format of the electrical–thermal coupling equations using the finite volume method (FVM) with consideration of the RDL in the interposer. An effective electrical–thermal coupling model for steady-state temperature and IR drop of 2.5-D CHI considering the Joule heating is proposed.
2) We propose a new method for extraction of the equivalent conductivity of the CHI systems. By conducting thermal parameter and electrical parameter equivalent modeling for complex structures such as TSVs, bumps, and RDL, enhancing the overall efficiency of the model.
3) Combined with the new extraction method of equivalent material parameters, a complete computational electrical–thermal co-simulation approach for the CHI system is established. Then, the simulated results of the present model are compared with the finite element method, where the simulation error is less than 1%.

4) The consistency of the present electrical–thermal coupling model and the FEM simulations indicates that the new proposed model is helpful in temperature and voltage drop analysis of CHI systems with the Joule heating effect.

This article is organized as follows. Section II describes the theoretical electrical–thermal coupling model in detail. A series of validations of the model are carried out in Section III. Based on this, physical parameter analysis of the CHI system by using electrical–thermal co-simulation is executed in Section IV. Finally, the conclusion of this article is given in Section V.

II. Modeling

In this section, the electrical–thermal coupling mechanism of the CHI system is investigated in Section II-A. In Section II-B, the FVM is utilized to discretize the steady-state heat conduction equation and the current continuity equation, and an iterative solution procedure for electrical–thermal coupling flow is given. The architecture of the CHI system is presented in Section II-C. In Section II-D, the equivalent thermal and electrical modeling of TSV, bump, and RDL is carried out by electrical–thermal duality.

A. Electrical–Thermal Coupling Mechanism of CHI System

During the operation of ICs, most of the power consumption is due to active devices and interconnects. The power consumption leads to a temperature rise in the CHI system, which can cause changes in the temperature-dependent material parameters and in turn affect the electrical properties. The interaction between electrical and thermal properties is known as the electrical–thermal coupling effect or the Joule heating effect.

The governing equation for the steady-state voltage distribution of a conductor in the CHI system is given by

$$\nabla \cdot \left(\frac{1}{\rho(x, y, z, T)} \nabla \varphi(x, y, z) \right) = 0 \tag{1}$$

where ρ is the temperature-dependent resistivity and φ is the potential distribution. The resistivity of the conductor is represented as follows:

$$\rho = \rho_0 [1 + \alpha (T - T_0)] \tag{2}$$

where T_0 is the reference temperature of the conductor, ρ_0 is the resistivity of the conductor at the reference temperature, and α is the temperature coefficient of the conductor in the CHI system [21].

The distribution of the steady-state temperature is controlled by the heat equation, and the heat transfer control equation is expressed as follows:

$$\nabla \cdot \left[\kappa(x, y, z) \nabla T(x, y, z) \right] = -P(x, y, z) \tag{3}$$

where κ is the thermal conductivity of the solid medium and T is the temperature. P is the heat source, which is the sum of the heat source excitation from the chiplet and the Joule heating converted from the Ohmic loss due to current flowing through conductors.

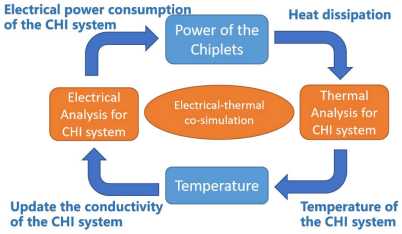


Fig. 2. Schematic of the electrical–thermal co-simulation of the CHI system.

The Joule heating is related to the current density and the electric field distribution, which is represented as follows:

$$P_{\text{Joule}}(x, y, z) = \vec{J} \cdot \vec{E}(x, y, z) = -\vec{J} \cdot \nabla \varphi(x, y, z) = \frac{1}{\rho(x, y, z, T)} |\nabla \varphi(x, y, z)|^2 \tag{4}$$

where P_{Joule} is the heat source of Joule heating, $\vec{J}$ is the current density, and $\vec{E}$ is the electric field distribution. The principle of electrical–thermal coupling simulation can be described by the above control equations, which is shown in Fig. 2. First, the CHI system is electrically analyzed to obtain the electrical power consumption, and then, it is thermally analyzed using this power value as a heat source to obtain the temperature distribution of the system. Subsequently, the temperature-dependent resistivity is updated according to the temperature changes. The above coupling process is iterated until numerical convergence.

Otherwise, for the heat conduction equation, the boundary conditions are expressed as follows:

$$T_S = T_n \tag{5}$$

$$\kappa \frac{\partial T}{\partial n} = -h_c (T - T_a) \tag{6}$$

where T_n denotes a temperature constant, h_c is the convective heat transfer coefficient, and T_a denotes the ambient temperature.

For the electrical voltage distribution equation, the Dirichlet boundary condition is given as

$$\phi = \phi_d \tag{7}$$

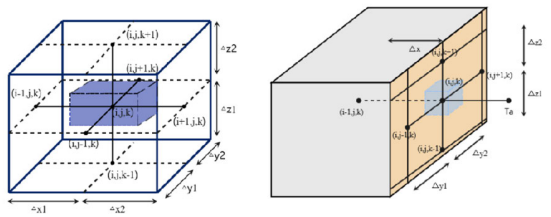
similar to the thermostatic boundary, where φ_d is a voltage constant.

Moreover, the impedance boundary with an external load is also represented as

$$\sigma \frac{\partial \varphi}{\partial n} = \frac{\varphi}{RS} \tag{8}$$

where σ is the conductivity and R and S are the resistance of the impedance boundary and the cross-sectional area, respectively. In practice, the substance of the boundary is generally air, and the conductivity of air is approximately zero; thus, the boundary condition of (8) can be simplified as

$$\sigma \frac{\partial \varphi}{\partial n} = 0. \tag{9}$$



(a) (b)

Fig. 3. Division of the grid. (a) Three-dimensional nonuniform rectangular grid for heat conduction. (b) Three-dimensional nonuniform rectangular grid for convection boundary.

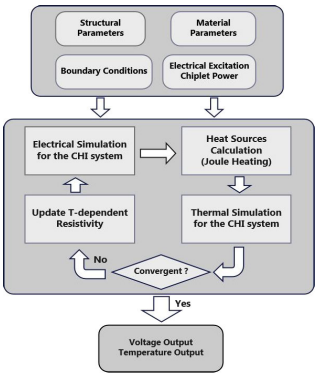


Fig. 4. Main algorithmic procedure of electrical–thermal co-simulation of the CHI system.

B. FVM Volume Method

In order to perform the simulation process, the voltage distribution equation for the resistivity versus temperature and the heat transfer equation for the Joule heating effect need to be solved simultaneously. For efficiently updating the temperature and voltage drop distributions, it is necessary to use the same mesh for both electrical and thermal co-simulations. The CHI system has large-size planes and small-size structures such as TSV, bump, and RDL, 3-D nonuniform meshes need to be used to reduce the number of unknowns and thus reduce the simulation time.

The 3-D nonuniform mesh used in the heat transfer simulation is modeled on the left of Fig. 3. $T_{i,j,k}$ denotes the temperature of the grid point, which is surrounded by six surrounding nodes. $\Delta x_1, \Delta x_2, \Delta y_1, \Delta y_2, \Delta z_1,$ and Δz_2 are the distances between the node (i, j, k) and its six neighboring nodes. The dashed cell in the figure intersects with the midpoint of the line connecting the node (i, j, k) to the six surrounding nodes. By integrating (3) over the dashed cell and applying the divergence theorem and the finite-difference approximation to the first-order derivative of T, the finite volume formulation expression of the heat transfer equation at the node (i, j, k) can be described as

$$\left(\frac{k_x l_y l_z}{\Delta x_1}+\frac{k_x l_y l_z}{\Delta x_2}+\frac{k_y l_x l_z}{\Delta y_1}+\frac{k_y l_x l_z}{\Delta y_2}+\frac{k_z l_x l_y}{\Delta z_1}+\frac{k_z l_x l_y}{\Delta z_2}\right)T_{i,j,k} - \frac{k_x l_y l_z}{\Delta x_1}T_{i-1,j,k} - \frac{k_x l_y l_z}{\Delta x_2}T_{i+1,j,k} - \frac{k_y l_x l_z}{\Delta y_1}T_{i,j-1,k} - \frac{k_y l_x l_z}{\Delta y_2}T_{i,j+1,k} - \frac{k_z l_x l_y}{\Delta z_1}T_{i,j,k-1} - \frac{k_z l_x l_y}{\Delta z_2}T_{i,j,k+1} = P_{\text{total}} \tag{10}$$

where $l_x = (\Delta x_1 + \Delta x_2)/2$, $l_y = (\Delta y_1 + \Delta y_2)/2$, and $l_z = (\Delta z_1 + \Delta z_2)/2$. k_x, k_y, and k_z are the thermal conductivity in the x-, y-, and z-directions, respectively. $P_{\text{total}} = \iint_{\text{dashed cell}} -P(x, y, z)dS$ is the total heat source in the dashed grid cell [22].

In order to obtain a realistic temperature distribution, the convective boundary condition in (6) needs to be considered. As shown in Fig. 3(b), the finite volume cell in the dashed line intersects with the midpoint of the line connecting the node (i, j, k) to the five neighboring nodes except the point in the air. The finite volume scheme for the heat transfer equation with the convective boundary condition at the node (i, j, k) can be represented as

$$\left(\frac{k_x l_y l_z}{\Delta x_1}+\frac{k_y l_x l_z}{2\Delta y_1}+\frac{k_y l_x l_z}{2\Delta y_2}+\frac{k_z l_x l_y}{2\Delta z_1}+\frac{k_z l_x l_y}{2\Delta z_2}+h_c l_y l_z\right)T_{i,j,k} - \frac{k_x l_y l_z}{\Delta x_1}T_{i-1,j,k} - \frac{k_y l_x l_z}{2\Delta y_1}T_{i,j-1,k} - \frac{k_y l_x l_z}{2\Delta y_2}T_{i,j+1,k} - \frac{k_z l_x l_y}{2\Delta z_1}T_{i,j,k-1} - \frac{k_z l_x l_y}{2\Delta z_2}T_{i,j,k+1} - h_c l_y l_z T_a = P_{\text{total}}. \tag{11}$$

As the governing equation for the voltage drop has a similar form as the heat transfer equation, the similar finite volume formulation for heat conduction can be adopted to describe the current flow in the conductor of the CHI system. Therefore, the 3-D finite volume scheme for simulating the dc IR drop at the node (i, j, k) can be given as

$$\left(\frac{l_y l_z}{\rho_x(T)\Delta x_1}+\frac{l_y l_z}{\rho_x(T)\Delta x_2}+\frac{l_x l_z}{\rho_y(T)\Delta y_1}+\frac{l_x l_z}{\rho_y(T)\Delta y_2}+\frac{l_x l_y}{\rho_z(T)\Delta z_1}+\frac{l_x l_y}{\rho_z(T)\Delta z_2}\right)\varphi_{i,j,k} - \frac{l_y l_z}{\rho_x(T)\Delta x_1}\varphi_{i-1,j,k} - \frac{l_y l_z}{\rho_x(T)\Delta x_2}\varphi_{i+1,j,k} - \frac{l_x l_z}{\rho_y(T)\Delta y_1}\varphi_{i,j-1,k} - \frac{l_x l_z}{\rho_y(T)\Delta y_2}\varphi_{i,j+1,k} - \frac{l_x l_y}{\rho_z(T)\Delta z_1}\varphi_{i,j,k-1} - \frac{l_x l_y}{\rho_z(T)\Delta z_2}\varphi_{i,j,k+1} = 0. \tag{12}$$

In order to solve the above electrical–thermal coupling equations, the detailed simulation procedure of the CHI system is shown in Fig. 4. This approach consists of the following four steps.

1) Setting input information for the CHI system. It includes material parameters, boundary conditions, structural parameters, heat sources, and electrical excitation.
2) According to the initial material parameters, a steady-state electrical simulation of the CHI system is performed to obtain the voltage distribution.
3) The Joule heat is calculated to update the heat source and the steady-state thermal simulation is performed to obtain the temperature distribution.

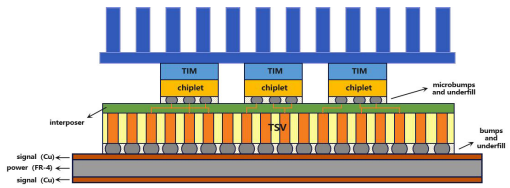


Fig. 5. Architecture of a 2.5-D CHI system.

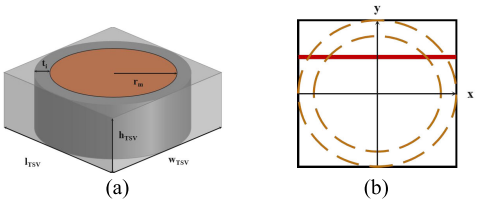


Fig. 6. (a) Schematic of TSV. (b) Top view of TSV [23].

4) Determining the convergence of the temperature distribution of the CHI system. If the temperature is convergent, the temperature and voltage distributions of the CHI system are output. Otherwise, adopting the temperature distribution to update the temperature-dependent resistivities of different materials and repeating the process of steps 2–4 until the convergence scheme is achieved.

After discretization, the algebraic equations for each grid point can be combined into an extremely large sparse matrix. Its general form is $Ax = b$. We use the Cholesky decomposition to solve this matrix equation. The specific solving algorithm is given as follows.

1) Perform Cholesky decomposition on the sparse matrix A to obtain $A = LL^{\mathrm{T}}$.
2) Treat Ax as $L(L^{\mathrm{T}}x) = Ly$, solve $Ly = b$, and obtain y.
3) Solve $L^{\mathrm{T}}x = y$ to obtain x.

The Cholesky decomposition is applied to solve steady-state heat conduction equations and its rationality is demonstrated in [27]. Following the above procedure, we ultimately achieved the iterative solution of electrical–thermal coupling for the 2.5-D CHI system.

C. Architecture of the CHI System

The architecture of the 2.5-D CHI system is shown in Fig. 5. The chiplet is connected to the RDL through microbumps and the interposer is a silicon substrate with TSV structures made by plasma etching. Bumps are connected under the silicon interposer to ultimately achieve the electrical connections between the chiplet and the package substrate, which can achieve a higher I/O density, lower transmission latency, and power consumption. The package substrate materials are Cu and FR-4. In summary, as the thermal conductivity as well as the electrical conductivity distribution in the CHI system are very complex, it is important to construct the equivalent models of TSV, RDL, and bump structures in order to simplify the electrical–thermal coupling model and accelerate the simulation efficiency of the CHI system.

D. Equivalent Modeling of TSV, Bump, and RDL

Because of the complex structures of TSV, bump, and RDL, obtaining the actual thermal conductivity and electrical conductivity is difficult. Therefore, we performed equivalent treatments for TSV, bump, and RDL. In our previous work, we proposed a new anisotropic equivalent thermal conductivity model for TSVs and bumps to capture the characteristics of their thermal conductivities and improve computational efficiency [23]. Based on this equivalent method and the electrical–thermal duality principle, we propose the equivalent electrical conductivity model and provide the calculating formulas in this section. Our approach of electrical equivalence is considered reasonable due to the validation of thermal equivalence methods in [23] and [25], as well as the thermal-electrical duality. For a single TSV, its structure is shown in Fig. 6.

The equivalent thermal conductivities [23] in the x-, y-, and z-directions are given as (13)–(15), as shown at the bottom of the next page, where r_m is the radius of metal; t_i is the thickness of insulating layer; and κ_m, κ_i, and κ_s represent the thermal conductivities of the metal, insulating layer, and substrate, respectively.

According to the electrical–thermal duality and following the similar derivation of the equivalent thermal conductivity, the equivalent electrical conductivity of the TSV structure can be obtained as follows (16)–(18), as shown at the bottom of the next page, where σ_m, σ_i, and σ_s represent the electrical conductivities of the metal, insulating layer, and substrate, respectively. The equivalent thermal conductivity of the TSV array is expressed as [23]

$$\kappa_{x\mathrm{TSVall}} = \frac{\kappa_S \cdot (w - N \cdot w_{\mathrm{TSV}})}{w} + \frac{\kappa_S \cdot N \cdot l w_{\mathrm{TSV}}}{(l - M \cdot l_{\mathrm{TSV}})w} // \frac{\kappa_{x\mathrm{TSV}} \cdot N \cdot l w_{\mathrm{TSV}}}{M \cdot l_{\mathrm{TSV}} w} \tag{19}$$

$$\kappa_{y\mathrm{TSVall}} = \frac{\kappa_S \cdot (l - M \cdot l_{\mathrm{TSV}})}{l} + \frac{\kappa_S \cdot M \cdot w l_{\mathrm{TSV}}}{(w - N \cdot w_{\mathrm{TSV}})l} // \frac{\kappa_{y\mathrm{TSV}} \cdot M \cdot w l_{\mathrm{TSV}}}{N \cdot w_{\mathrm{TSV}} l} \tag{20}$$

$$\kappa_{z\mathrm{TSVall}} = \frac{\kappa_{z\mathrm{TSV}} \cdot M \cdot N \cdot l_{\mathrm{TSV}} w_{\mathrm{TSV}} + \kappa_s \cdot (lw - M \cdot N \cdot l_{\mathrm{TSV}} w_{\mathrm{TSV}})}{lw} \tag{21}$$

where M and N represent that the TSV array has M rows and N columns. $\kappa_{x\mathrm{TSV}}$, $\kappa_{y\mathrm{TSV}}$, and $\kappa_{z\mathrm{TSV}}$ represent the equivalent thermal conductivities of a TSV in the x-, y-, and z-directions, respectively. Also, the symbol "//" is defined as $x// y = xy/(x + y)$.

Similarly, the equivalent electrical conductivity of the TSV array can be represented as follows:

$$\sigma_{x\mathrm{TSVall}} = \frac{\sigma_S \cdot (w - N \cdot w_{\mathrm{TSV}})}{w} + \frac{\sigma_S \cdot N \cdot l w_{\mathrm{TSV}}}{(l - M \cdot l_{\mathrm{TSV}})w} // \frac{\sigma_{x\mathrm{TSV}} \cdot N \cdot l w_{\mathrm{TSV}}}{M \cdot l_{\mathrm{TSV}} w} \tag{22}$$

$$\sigma_{y\mathrm{TSVall}} = \frac{\sigma_S \cdot (l - M \cdot l_{\mathrm{TSV}})}{l} + \frac{\sigma_S \cdot M \cdot w l_{\mathrm{TSV}}}{(w - N \cdot w_{\mathrm{TSV}})l} // \frac{\sigma_{y\mathrm{TSV}} \cdot M \cdot w l_{\mathrm{TSV}}}{N \cdot w_{\mathrm{TSV}} l} \tag{23}$$

$$\sigma_{z\mathrm{TSVall}} = \frac{\sigma_{z\mathrm{TSV}} \cdot M \cdot N \cdot l_{\mathrm{TSV}} w_{\mathrm{TSV}} + \sigma_s \cdot (lw - M \cdot N \cdot l_{\mathrm{TSV}} w_{\mathrm{TSV}})}{lw} \tag{24}$$

where $\sigma_{x\mathrm{TSV}}$, $\sigma_{y\mathrm{TSV}}$, and $\sigma_{z\mathrm{TSV}}$ represent the equivalent electrical conductivities of a TSV in the x-, y-, and z-directions, respectively.

The equivalent thermal conductivity for the bump arrays is given as [23]

$$\kappa_{x\mathrm{bumpall}} = \frac{\kappa_s \cdot \left(w - N \cdot w_{\mathrm{bump}}\right)}{w} + \frac{\kappa_s \cdot N \cdot l w_{\mathrm{bump}}}{\left(l - M \cdot l_{\mathrm{bump}}\right) \cdot w} // \frac{\kappa_{x\mathrm{bump}} \cdot N \cdot l w_{\mathrm{bump}}}{M \cdot l_{\mathrm{bump}} w} \tag{25}$$

$$\kappa_{y\mathrm{bumpall}} = \frac{\kappa_s \cdot \left(l - M \cdot l_{\mathrm{bump}}\right)}{l} + \frac{\kappa_s \cdot M \cdot w l_{\mathrm{bump}}}{\left(w - N \cdot w_{\mathrm{bump}}\right) \cdot l} // \frac{\kappa_{y\mathrm{bump}} \cdot M \cdot w l_{\mathrm{bump}}}{N \cdot w_{\mathrm{bump}} l} \tag{26}$$

$$\kappa_{z\mathrm{bumpall}} = \frac{\kappa_{z\mathrm{bump}} \cdot MN \cdot l_{\mathrm{bump}} w_{\mathrm{bump}} + \kappa_s \left(lw - MN \cdot l_{\mathrm{bump}} w_{\mathrm{bump}}\right)}{lw} \tag{27}$$

where $\kappa_{x\mathrm{bump}}$, $\kappa_{y\mathrm{bump}}$, and $\kappa_{z\mathrm{bump}}$ represent the equivalent thermal conductivities of a bump in the x-, y-, and z-directions, respectively; M and N represent that the bump array has M rows and N columns; and κ_s is the thermal conductivity of the underfill.

Similarly, the equivalent electrical conductivity of the bump array can be obtained as follows:

$$\sigma_{x\mathrm{bumpall}} = \frac{\sigma_s \cdot \left(w - N \cdot w_{\mathrm{bump}}\right)}{w} + \frac{\sigma_s \cdot N \cdot l w_{\mathrm{bump}}}{\left(l - M \cdot l_{\mathrm{bump}}\right)w} // \frac{\sigma_{x\mathrm{bump}} \cdot N \cdot l w_{\mathrm{bump}}}{M \cdot l_{\mathrm{bump}} w} \tag{28}$$

$$\sigma_{y\mathrm{bumpall}} = \frac{\sigma_s \cdot \left(l - M \cdot l_{\mathrm{bump}}\right)}{l} + \frac{\sigma_s \cdot M \cdot w l_{\mathrm{bump}}}{\left(w - N \cdot w_{\mathrm{bump}}\right)l} // \frac{\sigma_{y\mathrm{bump}} \cdot M \cdot w l_{\mathrm{bump}}}{N \cdot w_{\mathrm{bump}} l} \tag{29}$$

$$\sigma_{z\mathrm{bumpall}} = \frac{\sigma_{z\mathrm{bump}} \cdot MN \cdot l_{\mathrm{bump}} w_{\mathrm{bump}} + \sigma_s \left(lw - MN \cdot l_{\mathrm{bump}} w_{\mathrm{bump}}\right)}{lw} \tag{30}$$

where $\sigma_{x\mathrm{bump}}$, $\sigma_{y\mathrm{bump}}$, and $\sigma_{z\mathrm{bump}}$ represent the equivalent electrical conductivities of a bump in the x-, y-, and z-directions, respectively; and σ_s is the electrical conductivity of the underfill.

In order to reduce the complexity of the thermal model, we had constructed an algorithm of the equivalent thermal conductivity of the RDL in [25]. As for the RDL, metal wires embedded into the substrate are complex and the size of thermal model grid is much greater than the size of metal wires. After the equivalence of geometric parameters, the structure of RDL can be abstracted into a simple architecture, as shown in Fig. 7. In [25], we established an equivalent thermal conductivity model for RDL. We verified the reliability of this equivalent method through thermal simulations of the CHI systems in [25]. Based on this equivalent method, we also provide the equivalent equations for electrical conductivity. As the governing equations for heat and electricity are similar in form, the equivalent electrical conductivity obtained from this method has similar accuracy as the thermal conductivity considering the thermal–electrical duality. The simplified RDL model is shown in Fig. 7.

$$\kappa_{x\mathrm{TSV}} = \int_0^{r_m+t_i} \frac{dy}{\frac{\sqrt{(r_m^2-y^2)}H(r_m^2-y^2)}{\kappa_m} + \frac{\sqrt{(r_m+t_i)^2-y^2}-\sqrt{(r_m^2-y^2)}H(r_m^2-y^2)}{\kappa_i} + \frac{r_m+t_i-\sqrt{(r_m+t_i)^2-y^2}}{\kappa_s}} \tag{13}$$

$$\kappa_{y\mathrm{TSV}} = \int_0^{r_m+t_i} \frac{dx}{\frac{\sqrt{(r_m^2-x^2)}H(r_m^2-x^2)}{\kappa_m} + \frac{\sqrt{(r_m+t_i)^2-x^2}-\sqrt{(r_m^2-x^2)}H(r_m^2-x^2)}{\kappa_i} + \frac{r_m+t_i-\sqrt{(r_m+t_i)^2-x^2}}{\kappa_s}} \tag{14}$$

$$\kappa_{z\mathrm{TSV}} = \frac{\kappa_m \pi \cdot r_m^2 + \kappa_i \pi \cdot \left[(r_m+t_i)^2 - r_m^2\right] + \kappa_s (r_m+t_i)^2 (4-\pi)}{4(r_m+t_i)^2} \tag{15}$$

$$\sigma_{x\mathrm{TSV}} = \int_0^{r_m+t_i} \frac{dy}{\frac{\sqrt{(r_m^2-y^2)}H(r_m^2-y^2)}{\sigma_m} + \frac{\sqrt{(r_m+t_i)^2-y^2}-\sqrt{(r_m^2-y^2)}H(r_m^2-y^2)}{\sigma_i} + \frac{r_m+t_i-\sqrt{(r_m+t_i)^2-y^2}}{\sigma_s}} \tag{16}$$

$$\sigma_{y\mathrm{TSV}} = \int_0^{r_m+t_i} \frac{dx}{\frac{\sqrt{(r_m^2-x^2)}H(r_m^2-x^2)}{\sigma_m} + \frac{\sqrt{(r_m+t_i)^2-x^2}-\sqrt{(r_m^2-x^2)}H(r_m^2-x^2)}{\sigma_i} + \frac{r_m+t_i-\sqrt{(r_m+t_i)^2-x^2}}{\sigma_s}} \tag{17}$$

$$\sigma_{z\mathrm{TSV}} = \frac{\sigma_m \pi \cdot r_m^2 + \sigma_i \pi \cdot \left[(r_m+t_i)^2 - r_m^2\right] + \sigma_s (r_m+t_i)^2 (4-\pi)}{4(r_m+t_i)^2} \tag{18}$$

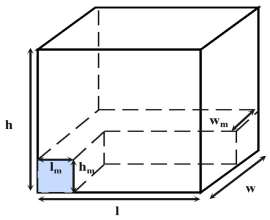


Fig. 7. Simplified RDL model [25].

Based on the simplified RDL model and combined with the similar manipulation of the bump and TSV structures, the equivalent thermal conductivity of RDL can be expressed as

$$\kappa_{x\mathrm{RDL}} = \frac{l}{wh}\cdot\left[\frac{\kappa_s w(h-h_m)+\kappa_m w h_m}{l_m} // \frac{\kappa_s(wh-w_m h_m)+\kappa_m w_m h_m}{l-l_m}\right] \tag{31}$$

$$\kappa_{y\mathrm{RDL}} = \frac{w}{lh}\cdot\left[\frac{\kappa_s l(h-h_m)+\kappa_m l h_m}{w_m} // \frac{\kappa_s(lh-l_m h_m)+\kappa_m l_m h_m}{w-w_m}\right] \tag{32}$$

$$\kappa_{z\mathrm{RDL}} = \frac{h}{lw}\cdot\left[\frac{\kappa_s lw}{h-h_m} // \frac{\kappa_s(l-l_m)(w-w_m)+\kappa_m(l w_m+l_m w-l_m w_m)}{h_m}\right] \tag{33}$$

where h_m is the sum of the heights of RDL layers; lw_m is the sum of the areas of all metal wires along the x-direction; $l_m w$ is the sum of the areas of all metal wires along the y-direction; and κ_m and κ_s represent the thermal conductivity of the metal and substrate, respectively [25].

In the same way, the equivalent electrical conductivity of RDL in th x-, y-, and z-directions is represented as

$$\sigma_{x\mathrm{RDL}} = \frac{l}{wh}\cdot\left[\frac{\sigma_s w(h-h_m)+\sigma_m w h_m}{l_m} // \frac{\sigma_s(wh-w_m h_m)+\sigma_m w_m h_m}{l-l_m}\right] \tag{34}$$

$$\sigma_{y\mathrm{RDL}} = \frac{w}{lh}\cdot\left[\frac{\sigma_s l(h-h_m)+\sigma_m l h_m}{w_m} // \frac{\sigma_s(lh-l_m h_m)+\sigma_m l_m h_m}{w-w_m}\right] \tag{35}$$

$$\sigma_{z\mathrm{RDL}} = \frac{h}{lw}\cdot\left[\frac{\sigma_s lw}{h-h_m} // \frac{\sigma_s(l-l_m)(w-w_m)+\sigma_m(l w_m+l_m w-l_m w_m)}{h_m}\right] \tag{36}$$

where σ_m and σ_s represent the electrical conductivities of the metal and substrate, respectively.

III. Model Validation

A. Three-Layer Package Substrate With Heat Conduction and Convection

A thermal convection planar structure is first simulated, which is shown in Fig. 8. The structure is a three-layer package substrate and the geometrical parameters of the structure are listed in Table I, where l, w, and h represent the length, width, and height of the structure, respectively. The 50-W heat source is given to the upper surface of the package substrate and the lower surface of the package substrate is set as a constant temperature of 298 K. The heat transfer coefficients are adjusted on the upper surface to capture the variational behavior of the temperature distributions of the top surface of the package substrate. The simulated results of the present new electrical–thermal model ChipletETSim and the analysis results of the existing literature are compared in Fig. 9. It can be observed that the temperature distribution of the top surface of the package substrate decreases with the increase in the convective heat transfer coefficient. The simulated results are consistent with the analytical solution, which indicates that the present new electrical–thermal model ChipletETSim can accurately capture the thermal dissipation behavior of the three-layer package substrate on the condition of heat conduction and convection.

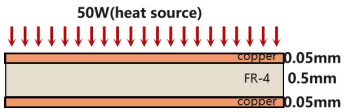


Fig. 8. Three-layer package substrate and heat source configuration [20].

TABLE I
Material Parameters Used in Fig. 8

NAME	SIZE (mm)	THERMAL CONDUCTIVITY (W/(m·K))
Copper	50 × 20 × 0.05	400
FR-4	50 × 20 × 0.5	0.5

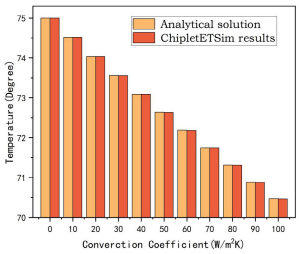


Fig. 9. Temperature distribution of the top plane with different convection coefficients.

B. Three-Layer Package Substrate With the Joule Heating Effect

Furthermore, the iterative method of the electrical–thermal coupling model is validated again to assure the accuracy of calculating Joule heating with consideration of the temperature-dependent resistivity effect. Another three-layer package substrate [20] is also introduced as a validation example of the electrical–thermal coupling model, which is illustrated in Fig. 10. A voltage of 2.5 V is applied to one side of the package substrate and the current flows through the copper plate on the upper side. In this case, the temperature coefficient of copper is 3.93×10^{-3}/K and the convective

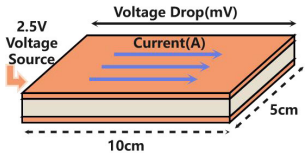


Fig. 10. Three-layer package substrate with a rectangular power plane.

TABLE II
MATERIAL PARAMETERS UTILIZED IN FIG. 10

NAME	SIZE (mm)	THERMAL CONDUCTIVITY (W/(m·K))	ELECTRICAL CONDUCTIVITY (*S*/m)
Copper	100 × 50 × 0.036	400	5.959×10^{7}
FR-4	100 × 50 × 0.35	0.8	1×10^{-10}

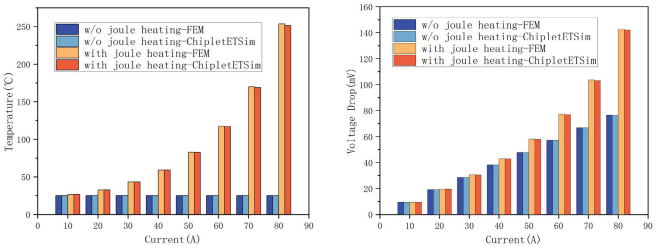


Fig. 11. (a) Comparison of the temperature distribution between ChipletETSim and FEM with and without the Joule heating effect. (b) Comparison of the IR drop between ChipletETSim and FEM with and without the Joule heating effect.

heat transfer coefficient of 5 W/(m^2·K) is applied to the upper and lower surfaces of the package substrate. In addition, the material parameters are listed in Table II.

The temperature and electrical–thermal coupling simulations of the three-layer package substrate structure were performed using ChipletETSim, and the results were compared with those of the finite element method. The maximum temperature of the package substrate and the maximum IR drop at both ends are illustrated in Fig. 11 with and without Joule heating, respectively. The maximum difference of the temperature distribution occurs at a current of 80 A, where the relative error at this point is 0.79%.

C. CHI System With Nine Chiplets

To further verify the accuracy of this model, we simulated a nine-chiplet 2.5-D CHI system, as described in Section IV. We compared the results with the data obtained using the finite element method. The voltage input points are located near the lower left corner. Each power consumption of chiplet was set to 5 W, and the current was 35 A. We collected temperature data at $y = 0.03443$ m in the RDL layer for comparison with the finite element simulation data, as shown in Fig. 12(a). The maximum relative error occurs at $x = 0.005$ m. At this point, our simulation result is 72.81 °C, while the finite element simulation result is 73.35 °C, resulting in a relative error of 0.74%. Therefore, our simulation results are compared with

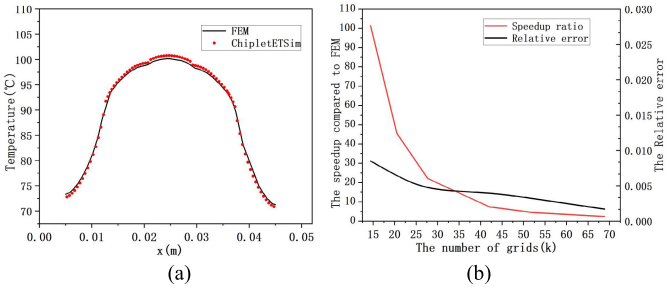


Fig. 12. (a) Temperature data at $y = 0.03443$ m in the RDL layer. (b) Speed ratio and relative error as the number of grids.

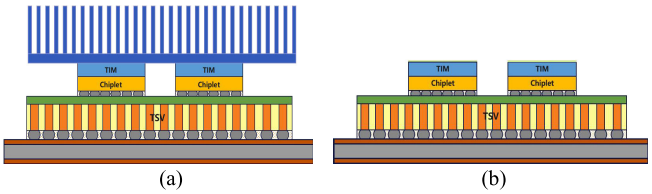


Fig. 13. (a) CHI system with a thermostatic heat sink. (b) CHI system with a fully modeled heat sink.

the data of the finite element method, with the relative error of less than 1%.

In addition, the grid number we used is 75.32k, with a maximum grid range not exceeding 8×10^{-4} m in the x- and y-directions, and 1×10^{-4} m in the z-direction. The computation time is 35 s. In comparison, a finite element method takes 70 s for the same grid number. In Fig. 12(b), we illustrate the impact of the grid number on the calculation error of junction temperature for the 2.5-D CHI system and present the trend of the speedup compared to FEM as a function of the grid number. The speedup ratio data in the figure indicate that a decrease in grid number leads to an increase in the speedup compared to FEM. When the grid number decreases to 14.4k, the speedup compared to FEM reaches 101 times. Under this grid number, the relative error of the junction temperature calculated by both methods is 0.85%. Therefore, it is reasonable to conclude that our electrical–thermal co-simulation method for CHI systems is accurate and efficient.

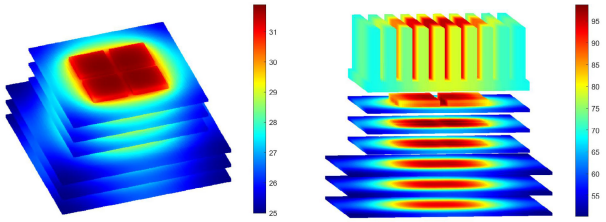
IV. MODEL GUIDELINES

A. CHI System With Four Chiplets

After verification of the present electrical–thermal coupling model ChipletETSim in Section III, the model application is performed to a CHI system with four chiplets to investigate the influence of the physical and geometrical parameters on the electrical–thermal coupling behavior in this section, where the lateral view of the CHI system is shown in Fig. 13. In our simulation, we mainly focused on modeling and simulating heat sink. It is important to note that thermal TSVs are also a method of heat dissipation used in 2.5-D CHI systems [28]. However, they are more commonly applied in 3D-IC. Therefore, in the present 2.5-D CHI systems with heat primarily transmitted through heat sinks, the thermal TSV has not been specifically considered for model simplicity. In our future work on transient electrical–thermal co-simulation of 3-D CHI

TABLE III
PARAMETERS USED IN FIG. 13

NAME	SIZE (mm)	NUMBER	THERMAL CONDUCTIVITY (W/(m·K))
Cu	50 × 50 × 0.05	/	390
FR-4	50 × 50 × 0.15	/	0.8
Bump	40 × 40 × 0.1	40 × 40	390; 0.5
TSV	40 × 40 × 0.1	40 × 40	401; 1.4; 130
RDL	40 × 40 × 0.005	/	390; 130
Microbump	10 × 10 × 0.015	50 × 50	390; 0.5
Chip	10 × 10 × 0.15	/	110
TIM	10 × 10 × 0.2	/	4
Heat Sink	40 × 40 × 0.18	/	237
Fin	2 × 40 × 0.4	10	237



(a) (b)

Fig. 14. (a) Simulation results for the heat sink considered to be thermostatic. (b) Simulation results for the heat sink fully modeled.

systems and 2.5-D CHI systems, we may consider the impact of thermal TSVs on vertical heat dissipation.

We mainly consider the impact of the heat sink on the heat distribution in the 2.5-D CHI systems. As the heat sink is assumed to be a constant of 300 K the TIM layer can also be equivalently considered as a thermostatic boundary. In the simulation, the structural parameters of the four-chiplet heterogeneous system are displayed in Table III. In addition, the convective heat dissipation coefficient of air is set to 100 W/(m^2·K). The spacing of the chiplets in the system is 2 mm and the power consumption of each chiplet is set to 10 W. The bump and TSV arrays are also set as 40 × 40. The symbols of l_{bump} and w_{bump} are 0.104 and 0.104 mm, respectively. The symbols of r_m and t_i are set to be 25 and 5 μm, respectively. The microbump array is set to 50 × 50. The symbols of $l_{\text{microbump}}$ and $w_{\text{microbump}}$ are set to be 0.06 and 0.06 mm, respectively. Moreover, the parameters of l_m, w_m, and h_m of the RDL are 3.625 mm, 3.67 mm, and 3.4 μm, respectively. It is worth noting that these parameters are only used for model demonstration in the 2.5-D CHI system.

Fig. 14(a) shows the temperature distribution of the CHI system for the case where the heat sink is considered as a constant temperature. In this case, the heat sink is omitted from the temperature distribution and the maximum temperature of the CHI system is 31.88 °C. Correspondingly, the simulated result in Fig. 14(b) with the heat sink subjected to fully thermal modeling shows a junction temperature of 98.67 °C and a minimum temperature of 50.148 °C. The large difference of the temperature distribution in (a) and (b) can be explained as follows.

When the temperature of the heat sink is set as a constant, the grid on the upper surface of the thermal interface material (TIM) is the TIM grid and the heat sink grid with constant temperature. The convective thermal resistance between the TIM grid and the surroundings can be calculated using the following formula:

$$R_1 = \frac{l_z}{2k_{\text{TIM}}l_x l_y} + \frac{l_z}{2k_{\text{sink}}l_x l_y}. \tag{37}$$

When adding the heat sink, the CHI system primarily dissipates heat through the heat sink via convection. The grid between the heat sink and the surroundings is the heat sink grid and the convective equivalent thermal resistance grid. The convective thermal resistance can be calculated using the following formula:

$$R_1 = \frac{l_z}{2k_{\text{sink}}l_x l_y} + \frac{1}{h_c l_x l_y}. \tag{38}$$

Both terms on the right-hand side of (37) represent conduction thermal resistance, while (38) contains convective thermal resistance. In thermal theory for the CHI systems, conduction thermal resistance is significantly smaller than convective thermal resistance. When the temperature of the heat sink is considered as a constant, the amount of heat dissipated by the CHI system to the surroundings exceeds that when considering convective heat transfer from the heat sink. Hence, a significant disparity of temperature distribution is observed between the two diagrams.

Moreover, as the temperature of the heat sink is treated as constant, the lower surface temperature of the heat sink is also considered as constant in the calculation. However, as the detailed shape of the heat sink is modeled with consideration of the heat consumption of chiplets, the temperature of the lower surface of the heat sink can range from tens of degrees to hundreds of degrees. This is a significant difference between the constant temperature configuration and the actual consideration of the heat sink shape. The thermal conductivity and the geometrical shape of the heat sink and the convective heat transfer coefficient of air play significant roles in the actual heat dissipation behavior of the CHI system. Treating the temperature of the heat sink as a constant value in the thermal simulation of the CHI system means that the influence of these parameters is maximized for model simplicity and the final simulation result is not reliable. Therefore, it is necessary to model the heat sink using reasonable boundary conditions and model assumption in the whole thermal simulation of the CHI system to obtain accurate temperature distribution.

In order to discuss the impact of the TSVs on the final results, we set the thickness of the insulation layer as 1×10^{-6} m and the number of TSV arrays as 300 × 300. The aspect ratio of TSV is changed and the junction temperature and the equivalent thermal conductivity are investigated. The final results are shown in Fig. 15.

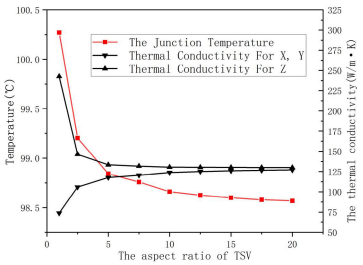
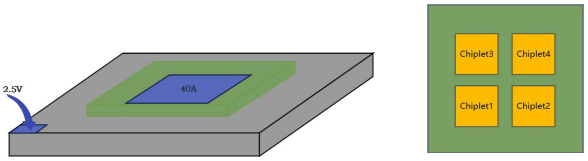


Fig. 15. Change of junction temperature and equivalent thermal conductivity as a function of the aspect ratio of TSV.



(a) (b)

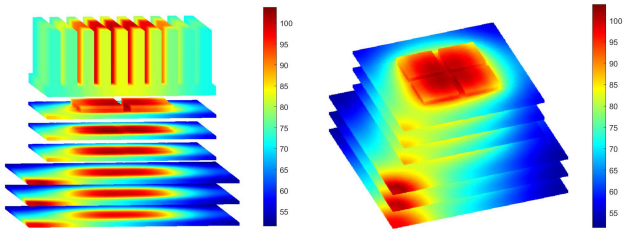
Fig. 16. (a) Voltage and current boundary conditions. (b) Layout for chiplet.

TABLE IV
ELECTRICAL MATERIAL PARAMETERS USED IN FIG. 13

NAME	ELECTRICAL CONDUCTIVITY (S/m)
Copper	5.95×10^7
FR-4	1×10^{-10}
Bump	5.95×10^7; 2×10^{-3}
TSV	5.95×10^7; 1.56×10^{-3}; 110
RDL	5.95×10^7; 1.56×10^{-3}
Microbump	5.95×10^7; 2×10^{-3}

As the aspect ratio of TSV increases, the junction temperature of the 2.5-D CHI system decreases. Moreover, the equivalent thermal conductivity of the TSV layer increases in the x- and y-directions, and the equivalent thermal conductivity decreases in the z-direction. Although increasing the aspect ratio of TSV makes heat dissipation more difficult in the vertical direction, it reduces the thermal blockage effect of the TSV layer in the lateral direction [30]. The thermal blockage effect impedes the heat transfer. As the horizontal size of the 2.5-D CHI system is much larger than that of the vertical size, the heat dissipation in the horizontal direction affects the temperature of the CHI system. The increase of the equivalent thermal conductivity of TSV in the horizontal direction is beneficial to the heat transfer, which results in reducing the junction temperature of the system. Moreover, the junction to the ambient thermal resistance R_{ja} can be expressed as: $R_{ja} = (T_j - T_a)/P$, where T_j is the junction temperature, T_a is the ambient temperature, and P is the total power dissipation of the chiplet. Increasing the aspect ratio of TSV leads to a decrease in R_{ja}, thus reducing the junction temperature.

In order to further investigate and discuss the effect of design parameters on the steady-state temperature distribution and IR drop, a supply voltage of 2.5 V was added at one point on the surface of the package substrate and the current boundary condition was set to 40 A. The specific settings of the voltage and current are shown in Fig. 16. The material parameters are listed in Table IV.



(a) (b)

Fig. 17. (a) Electrical–thermal co-simulation temperature results. (b) Side view temperature without heat sink.

TABLE V
IR DROP UNDER DIFFERENT CONDITIONS

CHIPLET	ELECTRICAL SIMULATION (mV)	ELECTRICAL-THERMAL CO-SIMULATION (mV)
1	42.22	53.63
2	42.29	53.72
3	42.29	53.72
4	42.34	53.78

The temperature distribution of the CHI system is shown in Fig. 17. The junction temperature increases to 103.72 °C and the minimum temperature of the system increases to 51.48 °C. Compared to the thermal-only simulation case, the junction temperature increases by 5.05 °C and the minimum temperature increases by 1.334 °C. The change in temperature stems from (4) in Section II, where the Joule heat leads to an increase in the overall temperature distribution of the CHI system.

Excessive IR drop may cause malfunctions in both functional mode and test mode [29]. Therefore, conducting electrical–thermal co-simulation is meaningful. The electrical simulation and the electrical–thermal co-simulation of the CHI system are performed separately and the IR drop under different conditions is shown in Table V. It can be observed that the voltage IR drop near the input side of the chiplet is lower. The standard voltage provided is 2.5 V. Taking Chiplet 1 as an example, the simulated chiplet voltage in electrical simulation is 2.45778 V, resulting in an IR drop of 42.22 mV. The voltage in electrical–thermal co-simulation is 2.44637 V, resulting in an IR drop of 53.63 mV. It can be seen that after incorporating the Joule heating effect, the IR drop increases by 27% compared to the circumstances without Joule heating effect. Similarly, for Chiplets 2–4, there is a nearly identical impact. The reasons for these IR drop variations are related to temperature-dependent resistivity, where the increase in temperature leads to the increase in material resistivity, requiring a larger IR drop for the current to flow toward the top surface of the chiplet.

The influence of the Joule heating effect on the electrical and thermal properties of the package substrate layer is shown in Fig. 18. Fig. 18(a) shows the temperature distribution of the top layer of the package substrate for the electrical–thermal co-simulation, and Fig. 18(b) shows the temperature distribution of the top layer of the package substrate for the individual temperature simulation. It can be seen

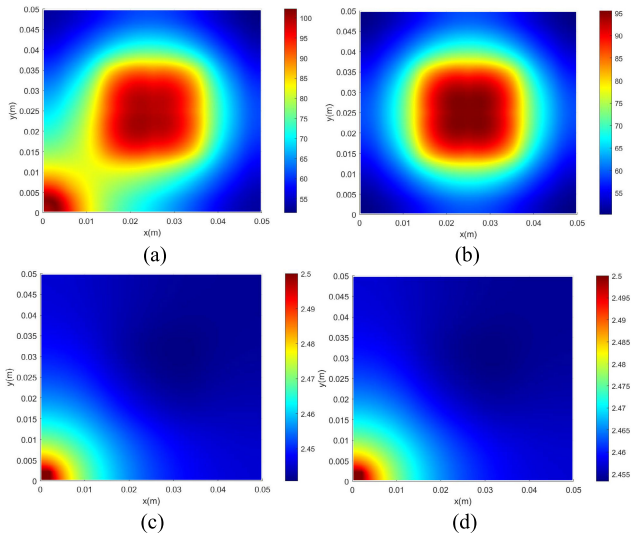


Fig. 18. Top temperature distribution of the package substrate layer for (a) electrical–thermal co-simulation and (b) thermal simulation. The top voltage distribution of the package substrate layer for (c) electrical–thermal co-simulation and (d) thermal simulation.

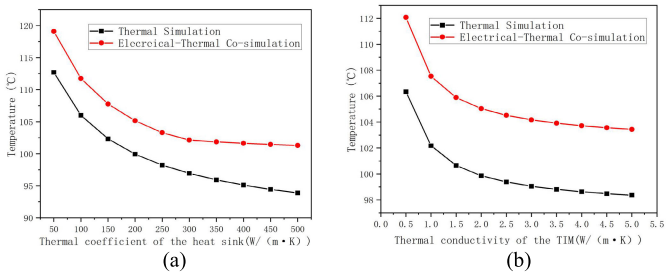


Fig. 19. (a) Relationship between the temperature and the heat sink heat conductivity. (b) Relationship between the temperature and the TIM heat conductivity.

that the hotspots after the electrical–thermal co-simulation occur at the voltage input location and the middle location. The maximum temperature for the individual temperature simulation is 95.52 °C and the maximum temperature for the electrical–thermal co-simulation is 102.2 °C. The temperature with the Joule heating effect results in 6.68 °C higher than the individual temperature simulation. Fig. 18(c) shows the voltage distribution at the top layer of the package substrate after the electrical–thermal co-simulation and the lowest voltage is 2.441 V. Fig. 18(d) shows the corresponding voltage distribution after the electrical–thermal co-simulation, where the lowest voltage is 2.453 V. Because of the Joule heating effect and the effect of the temperature-dependent resistivity, the voltage drop of the package substrate layer increases by 12 mV.

Moreover, we also investigated the relationship between the junction temperature of the CHI system and the thermal conductivity of the different materials. The simulated junction temperature of the CHI system is shown in Fig. 19(a) as a function of the thermal coefficient of the heat sink. It can be illustrated that the junction temperature of the system decreases as the thermal coefficient of the heat sink increases. When the thermal conductivity of the heat sink is increased, the thermal inhibition effect of the heat sink decreases in the thermal dissipation process of the CHI system.

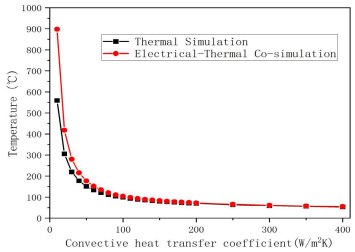


Fig. 20. Effect of the convective heat transfer coefficient of the atmosphere on the junction temperature of the CHI system.

Meanwhile, as the ambient temperature and heat source remain constant, the junction temperature of the CHI system decreases. The decrease rate of the temperature gradually becomes a saturated value as the thermal coefficient is set large enough. Because of the Joule heating effect, the predicted results of the electrical–thermal co-simulation are approximately 5 °C larger than those of the individual thermal simulation. The slower temperature drop in the electrical–thermal co-simulation compared to the thermal simulation result is presumed to be due to the fact that the voltage input point in the package substrate layer is farther away from the heat sink, and thus, the heat sink has less effect on this phenomenon. The simulated results in Fig. 19(a) show that increasing the thermal conductivity of the heat sink makes the temperature of the CHI system decrease. In addition, the thermal conductivity of the TIM also has a significant effect on the junction temperature of the heterogeneous system. The simulated results in Fig. 19(b) indicate that increasing the thermal conductivity of the TIM results in a similar variation trend of the heat dissipation behavior in the present CHI system, which can be explained similarly as in Fig. 19(a).

In addition, the effect of the convective heat transfer coefficient of the air on the temperature distribution was also simulated to capture the heat transfer mechanism of the CHI system. It can be concluded from Fig. 20 that an increase in the convective heat transfer coefficient of the atmosphere leads to a prominent temperature improvement of the CHI system as the transfer coefficient is less than 100 W/(m^2·K). When the transfer coefficient is higher than 100 W/(m^2·K), the influence of the transfer coefficient on the system temperature can be ignored. This result means that beyond a certain range of the convective heat transfer coefficient of the atmosphere, the increase in fan speed does not result in the expected better temperature cooling control. Under such circumstances, microfluidic cooling is a more effective way to dissipate heat than air cooling to decrease the whole temperature distribution of the CHI system. In the near future, we will introduce the microfluidic cooling effect into the ChipletETSim tool to further improve the applicability of the present electrical–thermal co-simulation model.

B. CHI System With Nine Chiplets

In order to further investigate the influence of the chiplet numbers on the electrical and thermal properties of the CHI system, the number of chiplets is set to nine. The chiplet layout and voltage input are shown in Fig. 21. A current

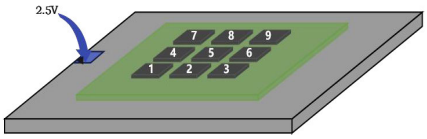


Fig. 21. Voltage input and the chiplet layout.

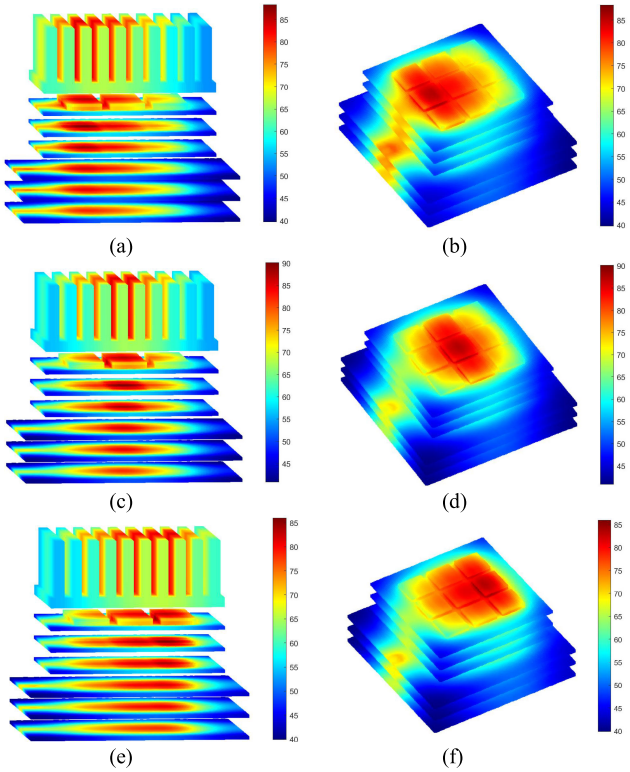


Fig. 22. (a) and (b) Views of the high power chiplets located at 1, 4, and 7 with and without heat sink. (c) and (d) Views of the high power chiplets at 2, 5, and 8 with and without heat sink. (e) and (f) Views of the high power chiplets located at 3, 6, and 9 with and without heat sink.

of 125 A in the x-direction is added to the top layer of the package substrate. The convective heat transfer coefficient of the atmosphere is changed from 100 to 200 W/ (m^2·K). First, we set the power of the three chiplets near the voltage input side to 8 W and the rest chiplets are set to 5 W. We performed the electrical–thermal co-simulator ChipletETSim by using a personal computer with Intel Core i5-12500H (2.5 GHz) and 16-GB RAM. The maximum grid sizes are 8×10^{-4} m in the x- and y-directions, and 1×10^{-4} m in the z-direction. The simulation runtime is 70 s.

The simulated results of the electrical–thermal co-simulation are shown in Fig. 22(a) and (b). On the present condition of the power setting, the junction temperature of the CHI system was 88.25 °C. Furthermore, we move the high-power chiplets toward the end away from the voltage input, and the power of chiplets 2, 5, and 8 is set to 8 W. The temperature distributions are shown in Fig. 22(c) and (d), where the junction temperature of the CHI system is 90.05 °C. Finally, we set the chiplet power furthest away from the voltage input to 8 W. In Fig. 22(e) and (f), the corresponding simulated results are illustrated. In this case, the junction temperature is 85.94 °C.

This simulation shows that the junction temperature of the CHI system does not decrease monotonically as the high-power chiplet moves away from the voltage input point. This is due to the fact that the CHI system has a smaller buffer on the interposer when the high-power chiplet is placed in the internal region. The area of the heat sink away from the edge region of the high-power chiplets is not effectively utilized in the heat dissipation process. In this case, the heat dissipation is mainly concentrated in the central position of the chiplet array. The position with the highest temperature in the chiplet array can be considered as a maximum heat source input. When the junction temperature is located in the central position, the relative heat dissipation area of the heat sink decreases, which increases the relative thermal resistance of the heat sink and results in an elevation of the CHI system temperature. Conversely, as the maximum heat source is set at the edge position, the relative heat dissipation area of the heat sink increases. This decreases the relative thermal resistance of the heat sink, resulting in a decrease in the system temperature. This finding is consistent with the conclusion given in [24] where the chiplets in peripheral environments will achieve a better thermal environment.

In addition, the junction temperature increased by 2.31 °C for the chiplet placed near the voltage point compared to the case of the chiplet placed away from the voltage point. The reason for this result is that the chiplet placement away from the voltage point increases the distance between the power dissipation hotspot of the chiplet and the Joule heating hotspot originated from the voltage input, which reduces the heat dissipation pressure of the heat sink at the highest temperature of the CHI system. In other words, high-power chiplets have a better cooling environment in the peripheral region away from the voltage input. This investigation suggests that placing high-power chiplets in the peripheral regions away from the voltage hotspots is an effective thermal management solution to decrease the entire temperature distribution of the 2.5-D CHI system.

V. Conclusion

In this article, a new steady-state electrical–thermal co-simulation model is proposed to accurately capture the dc IR drop and temperature distribution of the 2.5-D chiplet heterogeneous system, which takes convective heat transfer effects and Joule heating effects into account. More specifically, it is not reasonable to consider the heat sink as a constant temperature in the simulation, which would have a huge deviation from the actual conditions. Furthermore, the RDL, TSV, and bump structures were well modeled by means of introducing the electrical–thermal duality to accelerate the simulation efficiency of the present model. In addition, we performed electrical–thermal co-simulation considering the Joule heating effect and contribution of the air convection. The simulated temperatures and voltages are in good agreement with the finite element analysis results, and the maximum difference is less than 0.8%, thus verifying the accuracy of the electrical–thermal co-simulation model.

Finally, the influences of the physical and design parameters on the temperature control and IR drop distribution of the CHI system are investigated in detail. The simulation results indicate that the Joule heating effect leads to localized hotspots in the package substrate layer and placing a high-power chiplet in the peripheral region away from the voltage hotspot is an effective thermal management solution.

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