13.10 A 4nm 48Gb/s/wire Single-Ended NRZ Parallel Transceiver with Offset-Calibration and Equalization Schemes for Next-Generation Memory Interfaces and Chiplets

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With the development of industries, such as high-performance computing, advanced driver-assistance systems, artificial intelligence, and deep learning, demand for high-bandwidth memory, and chiplets continues to increase. Most of these applications generally use a source-synchronous single-ended parallel transceiver architecture and consist of a 2.5D package (called an advanced package) along with silicon interposer channels [1]. Applications also include a lot of high-speed I/O to process large amounts of data. In general, to achieve high-speed operation and high performance, bandwidth extension techniques, such as inductors and a continuous-time linear equalizer, and calibration schemes, such as slicer-offset calibration and skew calibration, between data and clock have been used in high-speed transceivers. However, these schemes are difficult to implement for applications that require many high-speed transceivers in a small area. For example, if an RX uses a quarter-rate architecture for high-speed operation, each slicer in the RX requires offset-calibration circuits, which require a significant area and static power consumption. Therefore, equalization techniques and the training schemes that can be implemented with low power and small area are being developed. Further, a 2D package, called standard package, with package substrate channels is being reviewed as an alternative to the advanced package for cost competitiveness [2-5]. In this work, we implement a 4nm 48Gb/s/wire single-ended NRZ parallel transceiver for next-generation memory interfaces and chiplets using standard package. The TX adopts an IQ clock divider with a high-speed clock and reset generator (HCRG) that prevents abnormal operations. We implement an on-chip Tx feedback equalizer, with a reduced feedback time and propose a duty-cycle corrector with cross-coupled inverters to minimize settling time and eliminate dynamic voltage stress. For the RX, digitally-controlled offset-calibration circuits are implemented, for each slicer, to reduce static-power consumption and area. Training algorithms for offset calibration are controlled by software. The transceiver in a 4nm FinFET CMOS technology operates up to 4 Gb/s/wire with a 10mm package substrate channel and achieves a 1.66Tb/s/mm beach-front bandwidth.

Figure 13.10.1 shows the source synchronous NZR single-ended parallel transceiver with small area and low-power consumption. The transceiver consists of four Tx and RX slices. Each TX and RX slice consists of 10 DQs for data and a DQS (DQSP and DQSN) for the strobe clock, which operates up to 48GB/s. The TX DQS includes a duty-cycle corrector (DCC) and an IQ clock divider; the duty cycle corrector, with cross-couple inverters, is implemented to minimize settling time and remove dynamic voltage stress; the IQ clock divider includes a clock and reset generator to prevent abnormal operation during high-speed operation. The digitally-controlled RX-slicer offset-calibration circuits are implemented to reduce static power consumption and chip area. The TX includes low-swing output drivers for low-power consumption; the output drivers consist of push-pull NMOS voltage-mode drivers for low swing, and a capacitive-equalizer driver to eliminate ISI. The RX includes coarse and fine de-skew circuits to compensate for the skew between DQ and DQS; NAND-based coarse delay lines and phase-interpolator based fine delay lines are used for the coarse de-skew, and phase rotators are used for the fine de-skew. To reduce phase-rotator power consumption, the common skew between DQ and DQS, which all DQs have, is compensated with the coarse de-skew circuits, and only the remaining skew is compensated with the fine-skew circuits.

Figure 13.10.2 shows a 4:1 serializer with a transmitter on-chip feedback equalizer (OFE). A quarter-rate architecture is used for the high-speed transmitter because it relieves timing constraints, such as setup and hold times. However, this architecture increases parasitic capacitance at the serializer's output node; causing inter-symbol interference (ISI), which increases jitter. In prior work, an on-chip feedback equalizer, with 2 inverters, was used to reduce the ISI [6]. A feedback time (t_f) <1UI is required to compensate for ISI that occurs at the serializer output by the OFE. An on-chip feedback equalizer, with a fast-feedback time, is proposed for high-speed operation; it can be configured as a single source follower to reduce the feedback time by up to 50%.

Figure 13.10.3 shows the proposed RX slicers with offset-calibration circuits. Transistors M1 and M2, and DACs are added to compensate for the slicer offset in prior work. The DAC voltage is applied to the transistors to compensate for slicer offset. To compensate each slicer, the number of DACs must equal the number of slicers; hence, power consumption and area increases. In this work, we implement a digitally-controlled offset-calibration circuits for slicer compensation and to minimize static power consumption and area. During offset calibration, the PAD is connected to the input common-mode voltage (V_{REF}). To find the optimal offset code, the de-serialized data (RXDATA[31:0]) is checked while sweeping the offset codes (OFSI[N:1], OFSQ[N:1], OFSIB[N:1], and OFSQB[N:1]) from minimum to maximum or vice versa. When the offset code is minimum the de-serialized data bits are all zeros, and when the offset code is maximum the de-serialized data bits are all ones. The offset codes are fixed by post-processing the codes found via the sweep operation. A pattern checker and the up-down counter FSM are implemented in software. To minimize the feedback time and compensate for the ISI, the second latch includes the DFE used [7].

The TX DQS includes a duty-cycle corrector (DCC) and a high-speed IQ clock divider (Fig. 13.10.4). Many DCCs contain an AC-coupling capacitor and resistors to compensate for duty-cycle distortion, so a setting time (t_{settle}) is required for normal clock generation. However, to transmit data without additional latency, the settling time must be minimized: for example, when retransmitting data after an idle state. Additionally, when a DCC operation starts, dynamic voltage stress occurs at the input nodes of inverters I1 and I2, due to the initial charge of the AC coupling capacitor; resulting in an inverter reliability issue. A DCC, with cross-coupled inverters, is proposed to eliminate this dynamic voltage stress and to minimize the settling time. The cross-coupled inverters are activated before the clock signal toggles, t_1. Then deactivated after the clock signal toggles, t_2. Settling time is minimized and the dynamic voltage stress is avoided as the inverters maintain the differential CMOS voltage level. The high-speed IQ clock divider receives the 24GHz 2-phase clocks (DCC_CLKP, DCC_CLKN) from the DCC and generates the 12GHz 4-phase clocks (I_{clk_12GHz}, Q_{clk_12GHz}, IB_{clk_12GHz}, QB_{clk_12GHz}). In prior work, the clock divider used either an asynchronous reset or a synchronous reset sampled with the high-speed clock and becomes active when the reset signal is released. However, as clock speeds increase, prior schemes can cause abnormal behavior: since the latch can be enabled after releasing the reset, there are periods where the pulse width is less than the clock-pulse width; the clock divider considers the short pulse as a fast-frequency signal, resulting in abnormal behavior. HCRG is proposed to eliminate abnormal divider operation due to the reset. The HCRG is implemented using high-speed latches (HSL). Synchronous-reset signals (SRST, SRSTN) are generated; then the gated clock signals (GCLKP, GCLKN) are generated using the reset signals (SAM_RST, SAM_RSTN) to guarantee an entire clock-signal pulse width; the reset is first released, and then the gated-clock signal is released.

Figure 13.10.5 shows the transceiver configuration within the package and the measurement results of the transceiver at 48Gb/s/wire. Two identical transceivers are connected inside the package with 10mm package substrate channels. The inner signal is connected to the inner signal, and the outer signal is connected to the outer signal; The connections depend on the rule constraints of the package design. Three layers are used for signal routing in the package to connect the 12 signals: 10 DQs and 2 DQS. A specific signal for measuring the TX eye diagram is assigned to the external ball without connecting it through the package-substrate channels. A measured eye-diagram at 48Gb/s with a 12.5ps/88mV margin shows that the implemented TX operates up to 48Gb/s. The measured eye-diagram is a waveform that reflects the characteristics of the package, probe card, and the internal V_{SS} equipment termination. The post-processed on-chip transceiver eye diagram at 48Gb/s shows a 12ps/85mV horizontal/vertical eye opening.

The performance summary is shown in Fig. 13.10.6. The transceiver is implemented using a standard package for next-generation memory interfaces and chiplets; it is fabricated in a 4nm CMOS technology. The transceiver operates up to 48Gb/s/wire with 10mm package substrate channels. The channel loss is -3dB at 24GHz. The transceiver achieves the best beach-front bandwidth and FoM compared to prior works. The testchip micrograph is shown in Fig. 13.10.7.

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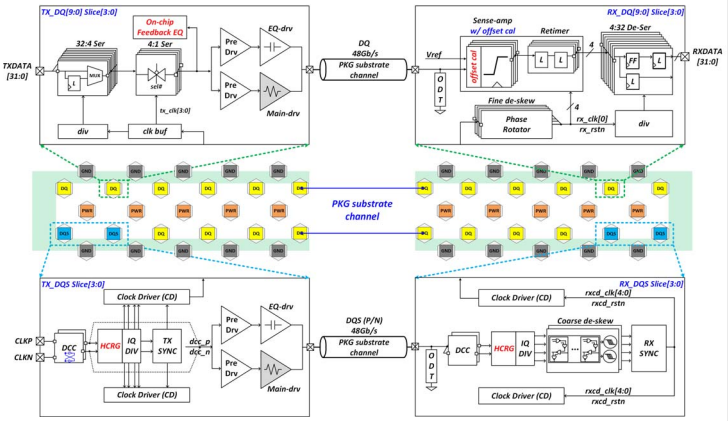


Figure 13.10.1: Implemented transceiver architecture.

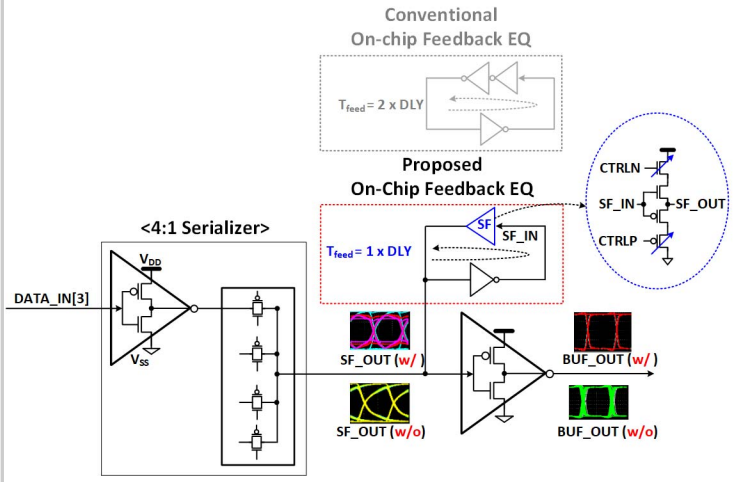


Figure 13.10.2: Implemented on-chip TX feedback equalizer.

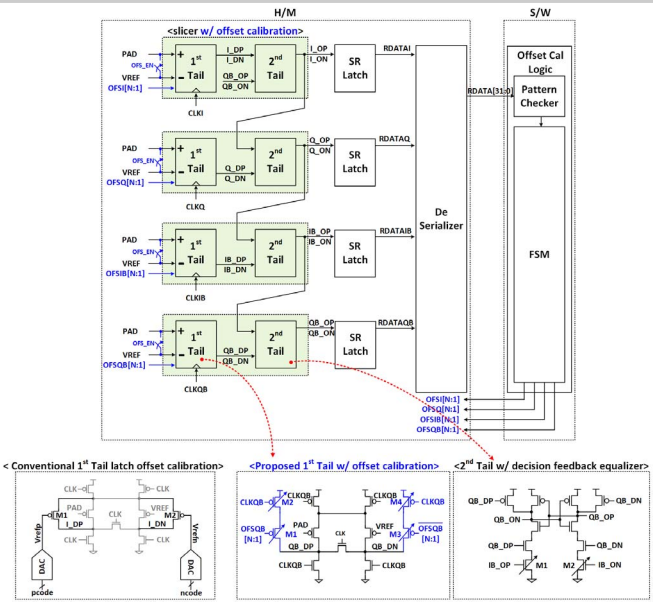


Figure 13.10.3: Conceptual view of RX offset-calibration scheme.

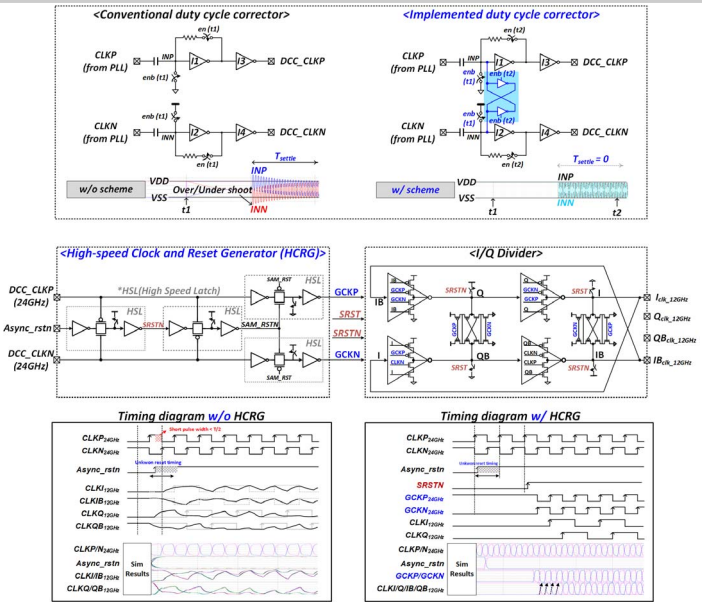


Figure 13.10.4: Implemented duty-cycle corrector and high-speed IQ clock divider.

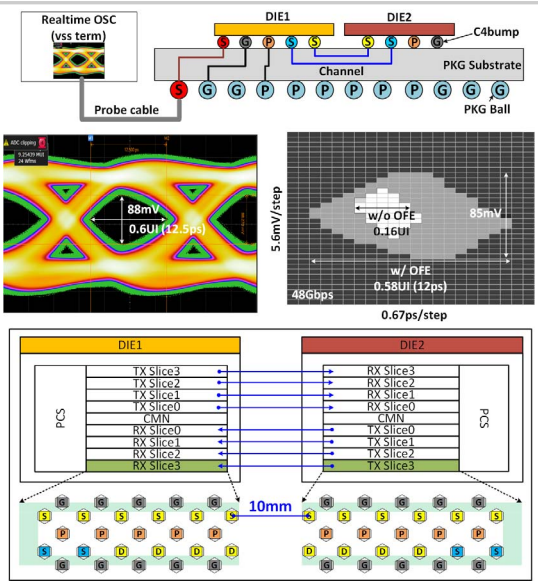
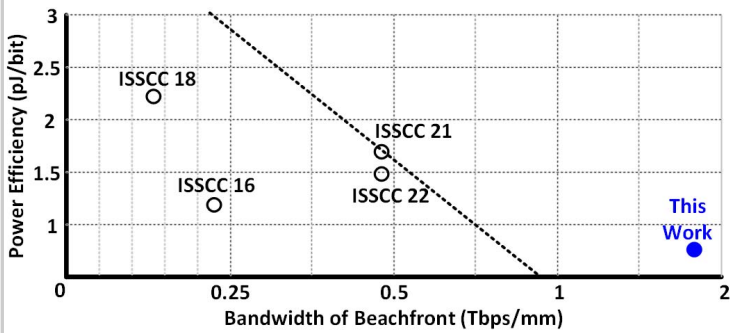


Figure 13.10.5: Measured TX eye-diagram and post-processed on-chip eye diagram at 48Gb/s.



	[2] ISSCC18	[3] ISSCC18	[4] ISSCC21	[5] ISSCC22	This work
Technology	16nm	16nm	7nm	5nm	4nm
Channel length (mm)	10/80 (PKG sub)*	25 (PKG sub)*	20 (PKG sub)*	5-80 (PKG sub)*	10 (PKG sub)*
Bump pitch (um)	-	150	130	-	130
Data rate (Gbps/pin)	25	56	40	113	48
Bandwidth of beach front (Tbps/mm)	0.2	0.168	0.45	0.46	1.85
Power efficiency (pJ/bit)	1.17	2.25	1.7	1.55	0.67
FoM ((Tbps/mm)/(pJ/bit))	0.17	0.07	0.26	0.296	2.76

*The Package substrate is used as the channels for signals.

Figure 13.10.6: Performance summary.

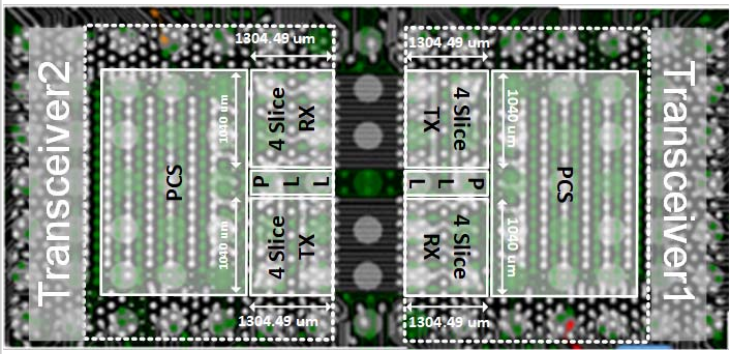


Figure 13.10.7: Package and testchip micrograph.

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