28.6 An 87% Efficient 2V-Input, 200A Voltage Regulator Chiplet Enabling Vertical Power Delivery in Multi-kW Systems-on-Package

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High-performance computing for AI and supercomputing applications are pushing the power and performance envelopes exponentially in highly volume constrained environments. This market segment is driving up the complexity of systems on package (SoP) and, power delivery in conjunction with heat removal are emerging as dominant bottlenecks. These demand reticle sized dies, and the process yields often dictate disaggregated approaches where the SoP consists of numerous stacked dies, each with varied functionality (computing, high bandwidth memory, IO) that span across many different process nodes [1]. The power delivery to these die complexes is particularly challenging as the lateral edges of the SoCs are reserved for data interfaces. This segues into the need for a VR chiplet due to the following reasons.

(i) Power delivery needs to be vertical due to unavailability of resources along die edges and due to the high distribution losses from total currents upward of 1500A. (ii) It can enable many voltage domains, therefore simultaneous performance, and power advantages. (iii) An integrated voltage regulator on component dies competes with performance blocks for key resources, causes thermal hotspots and has limited IP availability.

A representative construct of a data center product with a 1kW SoP is shown in Fig. 28.6.1. A VR chiplet may be used on landside/dieside of the package as the bare die or on the backside of the motherboard on its own package. The latter construct requires the package balls to have adequate current carrying capability for the SoP.

The key contribution of this work is a compact and low profile, scalable standalone VR chiplet for large voltage domains. It delivers 200A thermal design current (TDC) at 0.75A/mm^3 that rivals standard or custom discrete-component-based motherboard solutions. The high switching frequency of 65MHz in turn allows compaction and significantly lower decoupling requirements requirements. We demonstrate ganging capability that can support domain sizes of up to 500A. This VR comprises of 52 interleaved/parallel phases, uses distributed passives, i.e., high density MIM capacitors and on-package magnetic inductors and, native thin gate transistors on a 16 finFET CMOS foundry process providing a cost-effective solution. The low-profile factor, i.e., 2.083mm total build height including package and ball attach, makes it compatible with cooling techniques while also presenting a viable option with lower overall power consumption.

A comparative study of various power overheads from 48V to the chip show that purely looking at power delivery efficiency (conversion and distribution losses) only present the partial picture. We comprehend a third key component, i.e., how effectively the delivered power is utilized by the silicon. Factors like sharing rails across widely different functional blocks and dies, inter-die Vmin variation and the amount of high frequency decoupling in droop mitigation etc. come with the overheads of guard banding the operating voltage. Figure 28.6.1 shows power overhead comparison stacked up for a representative SoC tile of 500W, highlighting the reduced silicon power consumption in this approach resulting in ~10% lower power consumption at the 48V input, at identical workload/ performance throughput.

The VR chiplet utilizes buck converter topology with 4-phase interleaved PWM modulation and voltage mode control (Fig. 28.6.2). Special considerations in architectural choices and physical design that were crucial towards achieving high thermal design current (TDC) are delineated below. Figure 28.6.4 shows the basic building block, a phase pair called 'zoog', arranged into phase0 (1) at the top (bottom), respectively, with a channel in the middle for current sensing, phase current balancing and other miscellaneous functions. The bumps are arranged into a 3 column by 4 row arrays for each phase minimizing X dimension per phase. The Vin/Vx/Vss pattern for each bump is shown, Vin is input power, Vxbr is the power train (PTR) bridge output and Vss is ground. By tiling and mirroring the basic power train (PTR) bumps on Y axis, 13 zoogs are organized at either side of the controller that is centrally located. This symmetric arrangement further reduces the distance of the control, bias, and current sensing signals between the zoogs and the controller. In total the chiplet has 52 phases, constituting a total of 624 bumps, capable of supporting up to 624A I_{ccmax} for short duration and 200A TDC for intended 5-year lifetime in real usage. Each of the 52 phases may be configured to select 4 independent phase angles to optimize for ripple reduction and transient performance.

With the large number of phase counts and the innate limitations of a voltage mode control, active phase current balancing is an essential feature. Figure 28.6.3 shows how phase current balancing (PCB) is accomplished at a system level, and detailed implementation of the PCB block. The current sensing out from the phases (Csx phase) comes into the PCB block, generating a replica, and both get converted into voltage signals by two thin-film resistors (TFRs). The branch going through TFR-1 is proportional to current within this phase. The branch going through TFR-2 will either be connected to a global phase current balancing voltage reference (PCB_ref) wire, or unused depending on the mode. There are two modes on PCB_ref generation. In "averaging" mode, the switch is closed for all phases, thus Csx voltage is averaged to generate the reference. In "primary-secondary" mode, only for one "primary" phase this switch is closed, thus the PCB_ref is generated by this primary phase. During phase current balancing operation, each phase current voltage signal is compared against this PCB_ref voltage signal to determine the duty cycle adjustment of this phase, thus achieving desired balancing.

Figure 28.6.4 shows the bump pattern together with package inductor design. The per-phase inductors are realized on the 730µm thick core layer of the package, staggered to fit in the horizontal space. A magnetic layer that surrounds serially connected plated through-hole vias through the package core [4] increases inductance compared to air core inductors used in previous work, providing about 2.4nH per inductor.

Due to the large variation of ±2% in the thin film resistors (TFR), and 10mm long dimension of this die, trimming of TFRs is necessary. It is achieved with a single current source (tfr_trim_cs) and a voltage reference (tfr_trim_vref) from the controller used during a serialized trimming sequence, controlled by digital FSM. This is done at cold boot (addresses drift and ageing), with trim_done of one zoog launching trim_trig of the next. A 5b TFR code is generated to have the voltage across the TFR carrying tfr_trim_cs to match the tfr_trim_vref. The trimming yields matched TFR resistance within 1 LSB at 3%.

The test chip is of the shuttle container size at 12×4mm^2, with circuits occupying 11×3mm^2 as shown in Fig. 28.6.7. A standard size package of 37.5×37.5mm^2 with 5-2-5 layers, houses 2 VR chiplets and 3 load dies that provide the MIM capacitance termination and are capable of steep and controlled on-package step loads for transient measurements. This is mounted in a socket with thermal head.

Efficiency measurements (Fig. 28.6.5) at different output voltages show peak efficiency at 87%. Measured efficiency from ganging the two VR chiplets, show intended operation at a representative 100A, limited by the current and the thermal capabilities of the socket and test setup. Small signal measurements using on die stimuli show closed loop gain crossover at 5MHz, and a phase margin of 70 degrees (Fig. 28.6.6). Careful tuning of compensation and debug is expected to yield higher bandwidth. Comparison with fully integrated DC/DC converters reported earlier show current capability improvement by 40x, thereby establishing this technology as a viable option for formidable currents and large voltage domains (Fig. 28.6.7).

In conclusion, we present a 2V input VR chiplet with distributed magnetic inductors on a package that demonstrates 40× current capability over existing integrated solutions at respectable efficiency, and three orders of magnitude higher volume current density compared with discrete solutions. This work establishes the proposed VR chiplet as an attractive and cost-effective power delivery solution for high current domains in multi-kW systems-on-package, for wide scale adoption.

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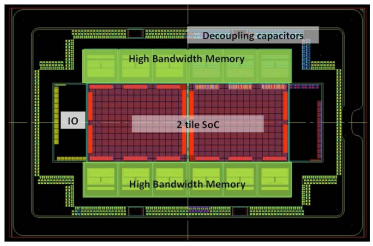
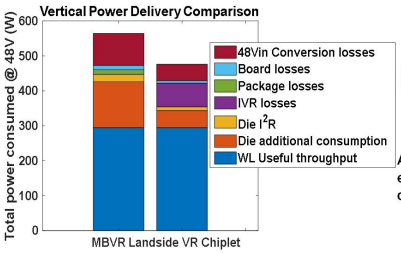
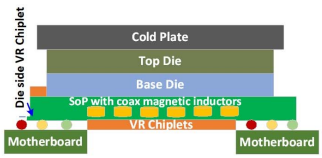
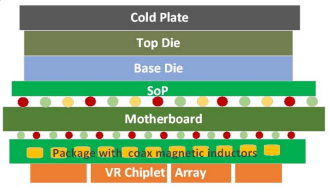


A representative 1kW System on Package for GPU (top), 500W SoC tile power breakdown(bottom)





VR Chiplet on the landside of the package, enables a thermally limited continuous current density of 6A/mm^2



Array of VR chiplets on a dedicated package, enables a ball limited continuous current density of 0.075A/mm^3

Figure 28.6.1: Multi-kW SoP using vertical power delivery constructs with VR chiplet die side/ land side on the package and backside of the motherboard.

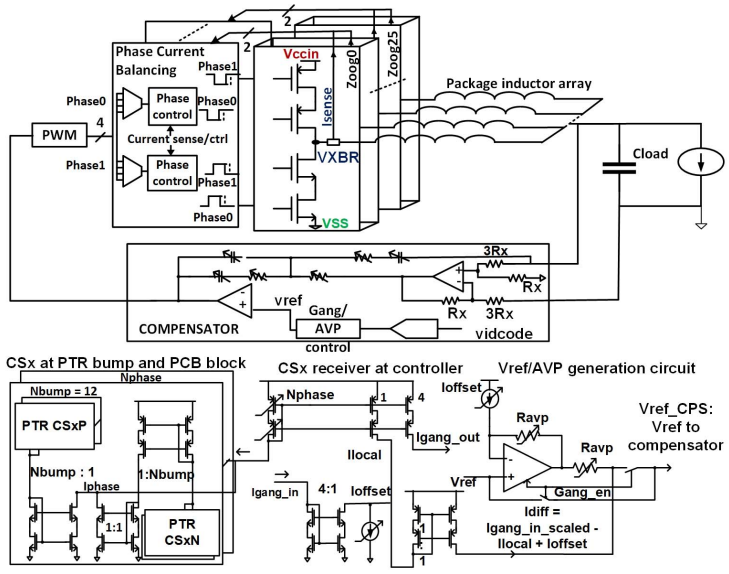
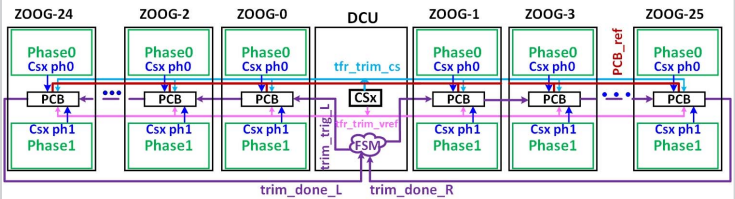


Figure 28.6.2: Block diagram of the buck converter in VR chiplet and circuit techniques enabling 2-way ganging of VR chiplets.



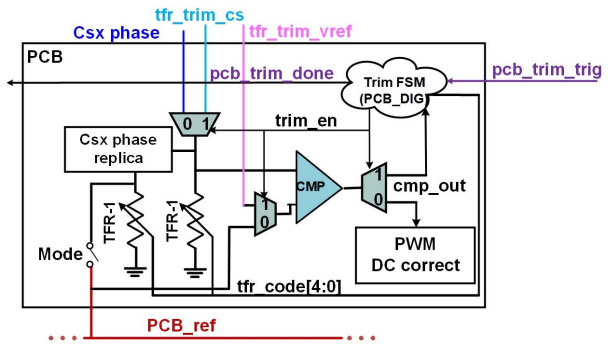
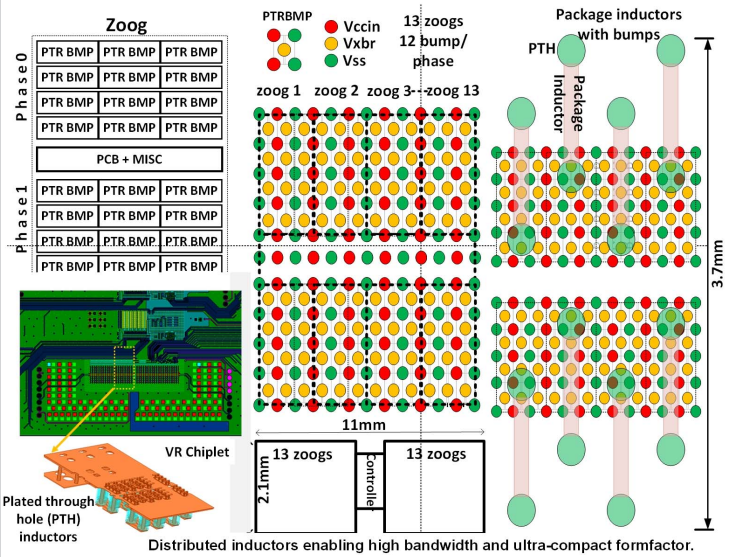
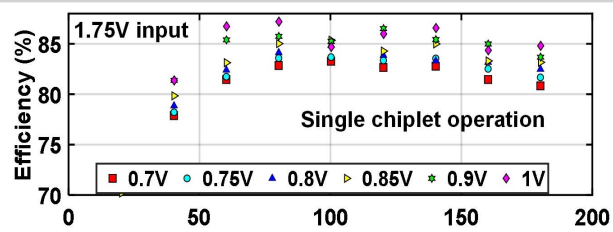


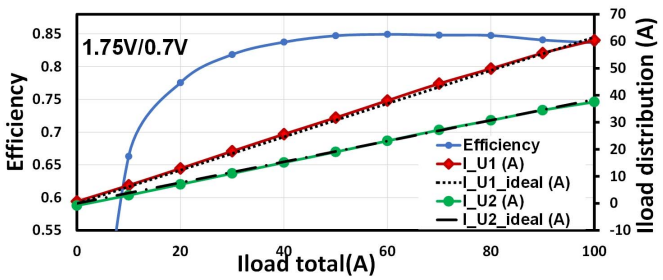
Figure 28.6.3: Phase current balancing (PCB) enabling many phases and high-thermal design current scalability upto 240A. DCU is the domain control unit.



Distributed inductors enabling high bandwidth and ultra-compact formfactor.

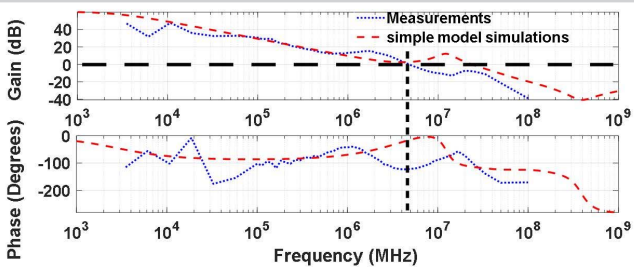
Figure 28.6.4: Physical design details: die bump pattern across the Vccin/Vxbr/Vss and distributed on-package magnetic inductors.

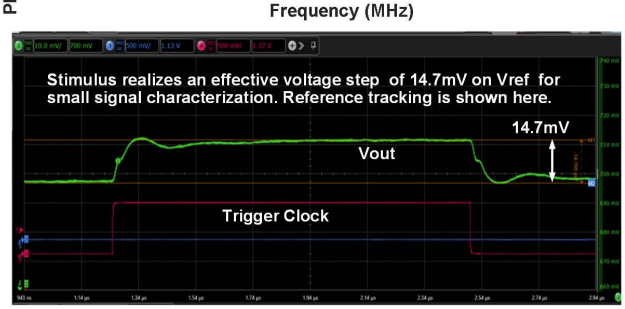




2-way ganged operation with asymmetric current sharing

Figure 28.6.5: Silicon measurements from 200A continuous-current test chip showing efficiency and bandwidth.

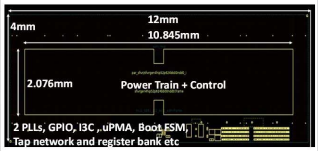




Measurements from silicon: Closed loop gain and phase

Figure 28.6.6: Small-signal measurements showing unity-gain crossover and phase margin.

Parameter	This Work	[2]	[3]	[4]
Technology	16FF Foundry	22nm	4nm	45nm
Inductor	In-package	In-package	In-package	integrated
Magnetic path	Magnetic	Air core	Magnetic	Magnetic
Fsw	65MHz	140MHz	50MHz	200MHz
L (per phase)	2.4nH	1.5nH	5nH	12.5nH
Phase Count	52	16	4	2
Vin	1.75V	1.7V	1.8V	1.8V
Vo	1V	1.05V	1V	1.1V
Imax	624A	16 A	12A	5A
Pk efficiency	87%	90%	91.5%	72%
Imax efficiency	-	-	82.5%	62%
I density, die	30A/mm²	31A/mm²	47A/mm²	1.5A/mm²



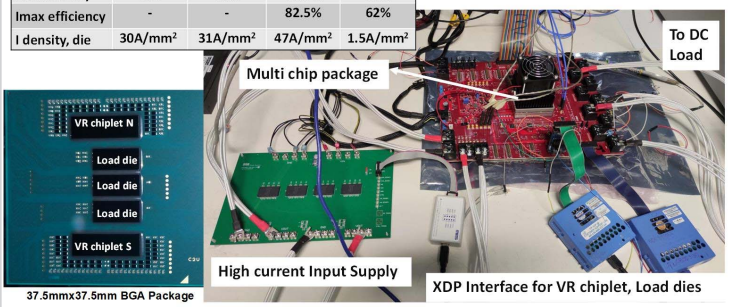


Figure 28.6.7: Die Layout, multichip package, test set up and comparison table.

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