PhD Application Interview

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Academic Experience

University of Nottingham Ningbo China (UNNC) Sept. 2021 – July 2025 *(expected)*
BSc Hons Computer Science

- Average score over the first three years: 78.3/100 (GPA equivalent: 3.82/4.0)
- The Dean's Scholarship of Academic Excellence 2022 – 2023
- 2023 Zhejiang Provincial Scholarship
- The Dean's Scholarship of Academic Excellence 2023 – 2024
- Meritorious Winner (top 4%) – The MCM/ICM 2024 (Jan. 2024)
- 2024 Dream Scholarship for Science & Technology (Dec. 2024)

University of Nottingham *(Exchange)* Sept. 2023 – June 2024
Computer Science

Research Experience – C2OPU[1]

Architecture support for Transformer-based LLMs (Large Language Models).

Two heterogeneous cores:

- CGRA core:
  - Coarse-Grained Reconfigurable Architecture
  - For general-purpose computing
- ACIM core:
  - Analog Computing-in-Memory
  - For weight-stationary multiplication

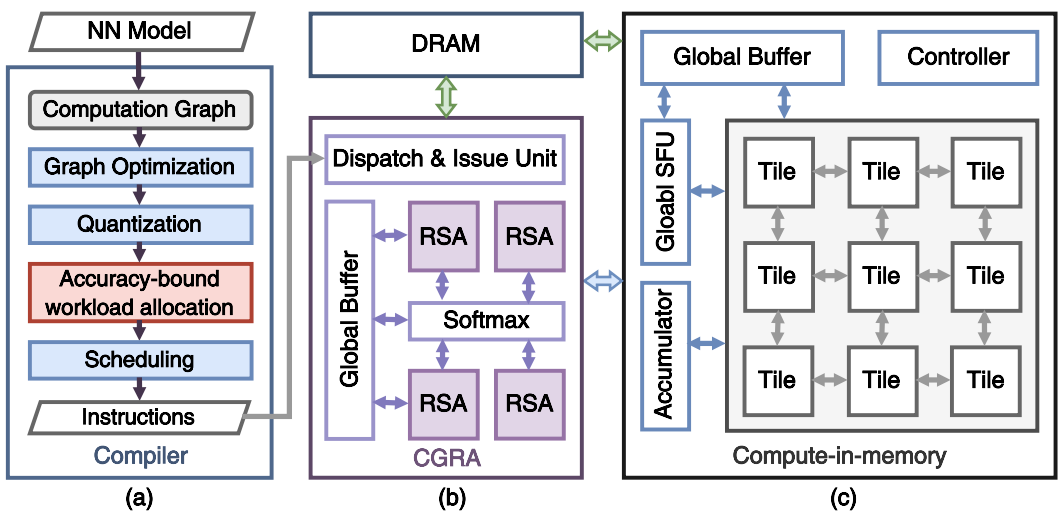

Figure 1: Overview of C2OPU

Research Experience – C2OPU[1] *continued*

Model	Variant	n_{params}	n_{layers}	n_{heads}	d_{model}	C2OPU speedup over				
						CPU	GPU	Science23	Nature23	VLSI24
BERT	Small	28M	4	4	512	133.41×	4.34×	4.25×	3.48×	1.24×
	Base	110M	12	12	768	159.22×	5.18×	5.08×	4.15×	1.48×
	Large	336M	24	24	1024	143.50×	4.67×	4.57×	3.74×	1.33×
GPT-2	Small	117M	12	12	768	158.75×	5.16×	5.06×	4.14×	1.47×
	Medium	345M	24	16	1024	146.78×	4.77×	4.68×	3.83×	1.36×
	Large	762	36	20	1280	139.36×	4.53×	4.44×	3.64×	1.29×
	XL	1.54B	48	24	1600	143.14×	4.65×	—	—	1.33×
T5	Small	61M	6	8	512	139.49×	4.54×	4.45×	3.65×	1.30×
	3B	2.85B	24	32	1024	131.21×	4.27×	—	—	—
DistilBERT		67M	6	12	768	159.22×	5.18×	5.08×	4.15×	1.48×
Average Improvements		/	/	/	/	**145.41×**	**4.73×**	**4.70×**	**3.85×**	**1.37×**

Table 1: Specifications of tested Transformer-based models and the speedup of C2OPU over different platforms

Research Experience – SYSgen[2]

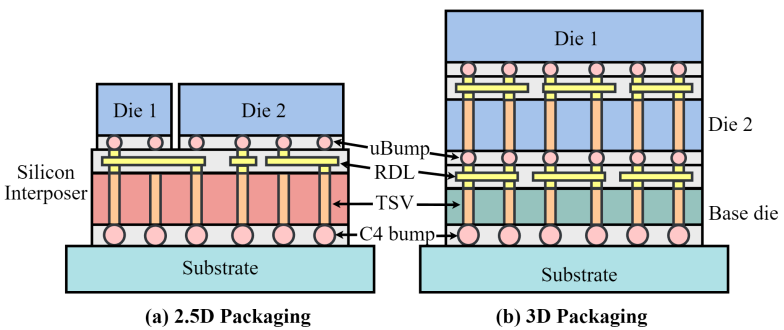

Figure 2: Illustration of advanced packaging technologies

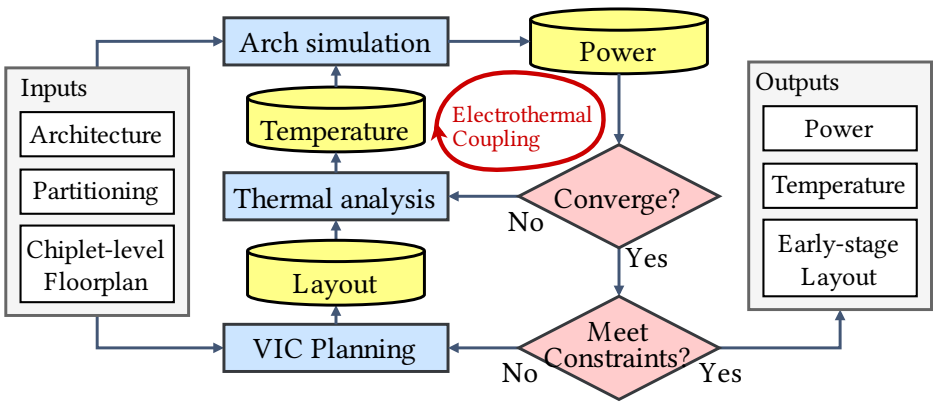

Figure 3: Overview of SYSgen

Vertical interconnects (VICs) includes:

- μbumps,
- C4 bumps, and
- through-silicon vias (TSVs)

VICs mainly serve for:

- Heat dissipation,
- Power supply, and
- Signal transmission

References

[1] S. Miao, L. Zhu, C. Wu, S. Lu, T.-J. Lin, and L. He, "C2OPU: Hybrid Computing-in-Memory and Coarse-Grained Reconfigurable Architecture for Overlay Processing of Transformers," in *2025 IEEE 33rd Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM'25)*, May 2025.

[2] S. Miao, L. Zhu, W. Yang, T. Lu, Y. Zhou, C. Wu, Z. Yu, T.-J. Lin, and L. He, "SYSgen: Electrothermal Simulation and Vertical Interconnect Planning for Integrated Chiplets," in *2025 3rd International Symposium of Electronics Design Automation (ISEDA'25)*, May 2025.

Thank you!

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