Rasool Sharifi

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Overview

My research interests lie broadly in Computer Architecture, Compilers, and Computer Security. My research explores novel hardware and software techniques to design secure machines while maintaining performance, energy efficiency, and high programmability. I'm also interested in applying novel machine learning techniques to detect and mitigate security threats. I have extensive experience in designing high performance, energy efficient FPGA and embedded systems for core consumer products. Recent research highlights include:

•**Hardware Security:** High performance and transparent capability based protection mechanism to secure unmodified source and object code against temporal and spatial memory safety exploits

•**Processing in Memory:** DRAM-based in-situ k-mer matching accelerator design for simultaneous comparisons of millions of DNA base pairs

•**Speculation-Driven Dynamic Binary Optimization:** Exploring dynamic binary optimization techniques at the processor level to speculatively generate and execute a super-optimized instruction stream

Education

University of Virginia, Charlottesville, USA — Sep. 2018 - Present
Ph.D., Computer Science

University of Tehran, Tehran, Iran — Sep. 2013 - June 2016
M.Sc., Electronics-Circuit and Systems

Isfahan University of Technology, Isfahan, Iran — Sep. 2009 - June 2013
B.Sc., Electrical Engineering

Research Experience

University of Virginia, Charlottesville, USA, — Sep. 2018 - Present
Graduate Research Assistant
Projects:
- Architecture Support for Memory Safety
- Boosting Performance via Speculation-Driven Dynamic Binary Optimization
- Processing in Memory for Bioinformatics Applications

University of Tehran, Tehran, Iran, — Sep. 2013 - June 2016
Graduate Research Assistant
Projects:
- Cluster Specific Multi-Rate Refreshing in Modern DRAM Systems

Publications

- Lingxi Wu, **Rasool Sharifi**, Marzieh Lenjani, Kevin Skadron, and Ashish Venkat, "Sieve: A Scalable In-Situ DRAM-based Accelerator for Massively Parallel K-mer Matching," in *2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture (ISCA)*, 2021, **Acceptance Rate: 18%**
- **Rasool Sharifi** and Ashish Venkat, "CHEx86: Context-Sensitive Enforcement of Memory Safety via Microcode-Enabled Capabilities," in *2020 ACM/IEEE 47th Annual International Symposium on Computer Architecture (ISCA)*, 2020, **Acceptance Rate: 18%, Top Pick in Hardware and Embedded Security – Selected from Architecture/Security/VLSI Design Conferences Held Between 2015-2020!**
- Ali Jahanshahi, **Rasool Sharifi**, Mohammadreza Rezvani, and Hadi Zamani, "Inf4Edge: Automatic Resource-aware Generation of Energy-efficient CNN Inference Accelerator for Edge Embedded FPGAs," in *2021 IEEE Workshop on Energy-Efficient Machine Learning (E2ML)*, 2021
- **Rasool Sharifi** and Zain Navabi, "Online Profiling for cluster-specific variable rate refreshing in high-density DRAM systems," in *2017 22nd IEEE European Test Symposium (ETS)*, 2017

Awards

CHEx86: Context-Sensitive Enforcement of Memory Safety via Microcode-Enabled Capabilities — Dec. 2021
Top Pick in Hardware and Embedded Security
Selected from Architecture/Security/VLSI Design Conferences Held Between 2015-2020

Skills

Programming Languages/APIs:
• C/C++, LLVM IR, Python, Bash, Assembly Programming (x86), VHDL, Verilog, SystemC

Simulators and Analyzers:
• Gem5 Architectural Simulator, McPAT, MARSSx86, Sniper Multi-Core Simulator, DRAMSim2, Ramulator, CACTI

Benchmarking and Performance Analysis:
• SPEC Benchmarks, SimPoints, Pin

Industry Software Skills:
• HSpice , Matlab , Modelsim ,Vivado, Quartus, Xilinx ISE, Xilinx EDK,Matlab System Generator

Practical Skills:
• SOC Design on FPGA, Embedded Linux on FPGA

Notable Projects

Architecture Support for Memory Safety,
Language: *C++, Python*, **Framework**: *LLVM, GEM5*

Speculation-Driven Dynamic Binary Optimization,
Language: *C++, Python*, **Framework**: *GEM5*

Processing in Memory for Bioinformatics Applications,
Language: *C++, Python*, **Framework**: *DRAMSim2*

Cluster Specific Multi-Rate Refreshing in Modern DRAM Systems,
Language: *Verilog, VHDL, C*, **Platform**: *Altera Stratix IV*

Design and Implementation of SMPTE 2022-6 Video Over IP Transmitter and Receiver Cores
Language: *VHDL, Verilog*, **Platform**: *Xilinx Virtex 7*

Design and Implementation of a Multi-touch Framework Based on ARM-M3 Micro-Controllers
Language: *C, C++, Assembly*
Automatic Resource-aware Generation of Energy-efficient CNN Inference Accelerator for Edge Embedded FPGAs,
Language: *C, C++, Chisel, Verilog*, **Platform**: *Xilinx Zynq SoC*

Professional Services

The Journal of Supercomputing (JS) - External Review Committee — 2021-present

Courses

CS6501: Interpretable Machine Learning — Spring 2022
University of Virginia

CS6501: Data Privacy — Spring 2022
University of Virginia

CS6316: Machine Learning — Fall 2019
University of Virginia

CS6501: Deep Learning for Visual Recognition — Spring 2020
University of Virginia

CS6501: Compilers — Spring 2020
University of Virginia

CS6501: Operating Systems — Spring 2021
University of Virginia

Teaching Experience

Teaching Assistant, CS4414: Undergraduate Operating System , — Fall 2021
University of Virginia

Teaching Assistant, CS3330: Undergraduate Computer Architecture , — Spring 2020, Spring 2021
University of Virginia

Teaching Assistant, CS6354: Graduate Computer Architecture, — Fall 2020
University of Virginia

Teaching Assistant, Digital Logic Design Laboratory, — September 2012 – June 2015
University of Tehran

References

Two references will be made available upon request.