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A systematic analysis of power saving techniques for wireless network-on-chip architectures

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ABSTRACT

Wireless network-on-chip (WNoC, a.k.a. WiNoC) architectures, as an emerging and viable alternative approach, overcome the communication constraints and drawbacks of network-on-chip (NoC) architectures. High scalability, high bandwidth, and low latency are the advantages of WNoCs that considerably alleviate the shortage of wired on-chip networks. Despite the great merits of WNoC, on the other hand, power-hungry wireless components cause problems regarding power consumption and temperature issues. Therefore, a significant challenge and an integral part of designing an efficient WNoC architecture would be resolving power management difficulties. Hence, the researchers have investigated various approaches to reduce and manage energy problems of WNoC structures while keeping up a trade-off between power efficiency and improving other performance parameters. This article presents a comprehensive systematic analysis on energy saving techniques in WNoCs. The goal is to classify state-of-the-art WNoCs architectures employing different approaches for reducing power consumption such as power gating, dynamic frequency/voltage scaling, enhancing transceiver structure, modifying topology and routing strategies. Some researchers investigate the impact of a wave-guiding medium type or wireless devices (e.g., transceivers) on power consumption. Besides, the voltage and frequency scaling, structure, routing and communication strategies are principal targets of energy efficiency.

1. Introduction

Continuing technology scaling is enabling the integration of a lot of processing elements to be placed in one chip, which comes with many challenges. The major challenge is to provide an efficient, low-power and reliable network infrastructure among these processing elements. Struggling with the modularity and scaling restrictions of communication, infrastructure of traditional point-to-point and bus based system-on-chip (SoC) architectures led to network-on-chip (NoC) approach. As a successful method, NoC-based many-core architectures are of remarkably pervasive [1–3]. However, the NoC architectures confront with challenges such as high latency and a great deal of power consumption stemming from long-distance multi-hop wired paths [4].

In order to alleviate the drawbacks of NoCs, several network interconnections including photonic NoC [5–8], 3D NoC architectures [9–11], radio frequency interconnections (RF-I) [12,13], millimeter-wave wireless network-on-chip (mm-Wave WNoC) [14,4,15–21], and surface wave interconnects (SWI) such as Terahertz (THz) nanocommunications [22–27] have been investigated. The basic concepts of photonic and wireless interconnections are to insert express communication links to reduce transmission latency and power dissipation. However, photonic links face technological challenges such as design of efficient transmitter and receiver components, reliability of integrated light source, and most importantly, the high manufacturing cost which prevents its commercial adoption.

WNoC, as one of the alternative architectures, has strived to address the mentioned limitations. Several designs and architectures have been offered [28,29], and many researchers have employed a hybrid wired–wireless (HWNoC) interconnection fabric within their proposed HWNoC-based architectures for performance improvements, latency, throughput, and energy efficiency (e.g., [30–33,18,34,14]). Intensive parallel applications, such as machine learning and multimedia processing, need a large amount of packet transmissions especially in the form of multicasting and broadcasting. WNoCs provide energy efficient architectures for implementing such algorithms [35,30,36–38]. Multi-chip NoC architectures [26,39–44,19,27,45–47,9,48–51,21,52,53] are partition-based communication infrastructures that facilitate traffic distribution and task allocation through independent parallel data flow. For emerging high data-intensive applications, multi-chip

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NoCs with wireless interconnections provide more parallelism and faster communication than the single-chip WNoCs.

Some comprehensive surveys related to different aspects of WNoC architectures have been presented in recent years [54–58,4,26,17,43,59,60]. For instance, Karkar et al. [54] discussed the advantages and disadvantages of some interconnection technologies, particularly the ones that support multicast. In [57], Rad et al. investigated congestion control mechanisms in WNoC architectures. In [55], a comprehensive survey on mm-Wave, terahertz and optical communication technologies was presented. The authors of [56] reviewed the standardization of mm-Wave communication, the latest progress and outcomes of the research on mm-Wave communication technologies, and their applications. An overview of terahertz nanocommunication and nanonetworking trends and requirements and applications was presented in [26]. In [17], a survey on on-chip mm-Wave wireless communication challenges such as transceivers, channel characteristics, and antenna implementation was presented. The challenges and the advances of mm-Wave wireless interconnecting a multi-chip system, including topology, physical layer, MAC and routing protocols were discussed in [43]. The authors of [60] reviewed the security threats and the countermeasures proposed so far for wired NoCs, wireless NoCs, and 3D NoCs. However, there is not any survey and systematic analysis on energy saving techniques and power consumption reduction approaches of WNoC architectures.

Despite the advantages of express wireless interconnections, the notable portion of the energy budget of overall HWNoC architectures belongs to the power dissipation of the wireless communications [61]. Since reducing power consumption is one of the most challenging issues in designing of WNoC architectures, it is very imperative to devise effective algorithmic techniques and to develop low-cost strategies addressing energy efficiency. Therefore, in this paper, a set of these research efforts was gathered to present relevant approaches for enhancing energy efficiency and reducing power consumption in WNoC architectures.

The basic idea of each approach target reducing static power dissipation or dynamic power consumption or both in some cases, due to switching activities and leakage power. The main power saving strategies for WNoC architectures are power gating (PG), physical layer of WNoC and antenna, dynamic voltage/frequency scaling (DVFS), voltage/frequency island-partitioned (VFI-partitioned), enhancing transceiver, topology, router microarchitecture, routing approach and approximate communication. Different wave-guiding mediums such as transmission line, millimeter wave and surface wave own specific characteristics regarding energy efficiency and other performance parameters [59]. Method of power gating focuses on power management by switching off idle components of the WNoC architecture and then switching them on when it requires participation in communication. The scheme in dynamic voltage frequency scaling uses a time-sliced controller to balance workloads and set voltage/frequency.

In hardware-oriented approaches like enhancing transceiver and router microarchitecture, an augmented version of each component would have a significant role in reducing power consumption. Moreover, different proposed topology and routing strategies are other influential factors of power consumption of WNoC architectures. Although different aspects of WNoC architectures have been investigated, to the best of our knowledge, this research is the first that gathers and categorizes strategies and methods of the power consumption reduction in WNoC architectures. Since in VLSI circuits, power dissipation appears in the form of heat. In reducing power dissipation techniques, as a consequence, the temperature reduction of the architecture is achievable [62]. Although some studies [63,64] address both power and thermal issues simultaneously, and some others [65] investigate power consumption regardless of thermal profiles [62].

The rest of this paper is organized as follows. Section 2 considers the basic WNoC microarchitectures. Section 3 describes the contributions of power consumption of WNoC components. Then, power saving strategies, concerning different aspects gathered from various research studies are discussed in Section 4. Section 5 is dedicated to the discussions. And finally, the conclusion and future works are presented in Section 6.

2. WNoC structure

This section is allocated to describing the basic structure of WNoC architectures. Conventionally, WNoCs consist of wired based routers (BR), hybrid wireless routers (HR) or radio-hubs, wireless interfaces (WIs) and links. The wired routers are used for short distance communication, whereas long-range wireless routers cover long distances for express communications. Generally, the wired based routers consist of input and output buffers, routing computation unit, switch and channel allocators, and a crossbar switch [1]. Fig. 1 demonstrates the augmentation of a wired-based structure along with WIs, which are required for interfacing the wired and wireless components. As the figure shows, WIs comprise of several components including modulators, demodulator, low noise amplifier (LNA), power amplifier (PA), serializer/deserializer buffers and on-chip antennas [66–70,50,43]. In most of WNoC architectures, WIs have been embedded to some of BRs to form HRs to expedite the network long-distance communications [61]. Wireless communication can be achieved by employing CMOS compatible transceiver and miniaturized on-chip antennas [4,61,71,69,36,43,42,39].

As Fig. 1 illustrates, LNA, demodulator and deserializer belong to the receiver unit, while serializer, modulator and PA belong to the transmitter unit. LNA amplifies the received signal from the antenna and the signal will be demodulated. Then, the signal will be transformed into parallel data by the deserializer component. Finally, the received data flit is ready for additional processing at the hybrid router. On transmitting part, data flit will be changed into a serial data stream; this signal will be modulated and then amplified by the PA component. Then, the data flit is sent via the antenna. In hybrid wired/wireless architectures, communication between the cores locating in short distances occurs through traditional metal wires while wireless links are used for long-distance communications. In other words, the entire architecture is divided into subnets. Each subnet includes switches and links as in a wired NoC. The cores inside each subnet are connected to a central hub through wired links. In a second-level network, making up a hierarchical structure, the hubs have been connected through both wired and wireless links.

Employing wireless feature in on-chip networks, provide wireless links with high bandwidth and energy efficiency by translating most of the multi-hop route into a single-hop route [4]. However, with regards to the higher communication energy per bit in a wireless link in comparison with a wired link, applying wireless link would be efficient if the number of hops between source and destination nodes is greater than a certain threshold [61]. As an example, in iWise [28], the threshold number was defined as three. Although WNoC has ameliorated the limitations of conventional NoC by reducing multi-hop communications, this approach, yet, has its shortages which need to be investigated. Noisy wireless channels as a reliability issue and designing transceivers that dissipating lower power are the concerns and challenges of WNoC architecture [4,72].

3. The contribution of power consumption of WNoC components

In this section, we have explained the power consumption portion of the components of WNoC architectures. Two principal parameters are involved to evaluate the power consumption; dynamic power consumption which is caused by transistor switching, and static power consumption (i.e., leakage of circuits) [1,73]. The first step to enhance energy efficiency in WNoC would be identifying the most power-hungry components.

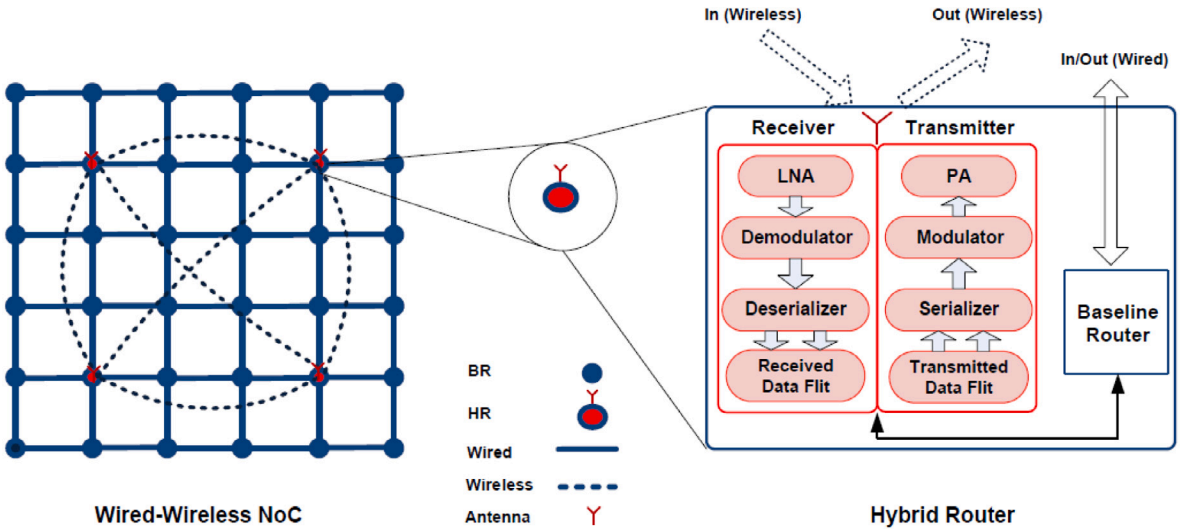

Fig. 1. Architecture of a WNoC and HR components.

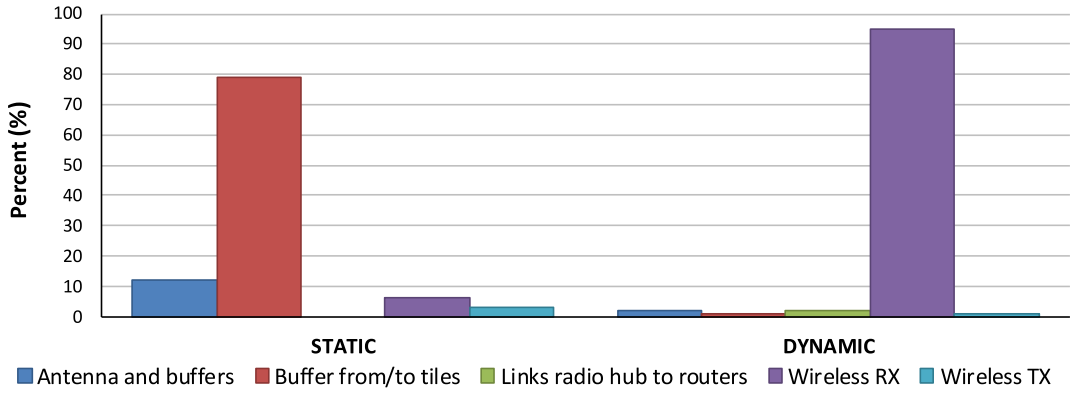

Fig. 2. Static and dynamic power breakdown of a radio-hub in details (the figure is based on [74]).

According to several investigations such as [66], some power consumption analyses of WNoC components have been reported. Catania et al. [74] present a detailed analysis of static and dynamic power consumption of different components in radio-hub (See Fig. 2). Their results demonstrate that, in a radio-hub the contribution of static power consumption is about 96% while dynamic power dissipation is 4% [74].

As Fig. 2 illustrates, input and output buffers from/to tiles (i.e., the buffers between each WI and its adjacent router) have the most static power consumption (about 79%). Moreover, it can be seen that about 96% of dynamic power consumption belongs to the wireless receiver (RX) component.

In addition, Fig. 3-a shows the power contributions of radio-hub components based on the analysis of Catania et al. [61]. The power proportion for transceiver was obtained from the result of transmitter and receiver power analysis by Yu et al. [66,75], and statistics for router and link have been estimated through a gate-level synthesis regarding 65 nm CMOS technology [61]. Power contributions in a radio-hub show that transmitter and receiver, as the most power-hungry parts, consume 39.26% and 34.64% of the total power consumption, respectively. Comparison between radio-hubs and the wire base routers in terms of energy consumption reveals that radio-hubs are higher energy-consumer than conventional routers [61]. The induced overhead by the WI, and the higher number of input and output buffers, are the culprits of causing higher energy consumption [61]. Moreover, the results of static power consumption of the investigation [66] manifest that LNA and PA parts have a great amount of power consumption. Fig. 3-b shows the percentages of power consumption breakdown of TX and RX elements. The total energy consumed by the transceiver (about 32 mW), nearly 63% implies the power consumed by PA and LNA, approximately 19% refers the energy consumption of Modulator and Demodulator, around 9% indicates the power consumption of PLL (VCO) and about 9% belongs the power budget of the baseline amplifier [66,37].

4. Energy saving techniques

This section presents the most important and effective strategies of power consumption reduction and energy saving. The main power consumption reduction and energy-saving techniques using in WNoC architectures include the following aspects.

1. Physical layer of WNoC and antenna
2. Power gating (PG)
3. DVFS/VFI-partitioned
4. PG and DVFS
5. Enhancing transceiver
6. Structure and network topology
7. Routing algorithms and congestion management
8. Heuristics approaches
9. Approximate communication

Some strategies of WNoCs power saving are similar to the methods utilized in wired NoC to reduce power consumption and save network energy [1,41]. Researchers in [58] provide a survey on methodologies

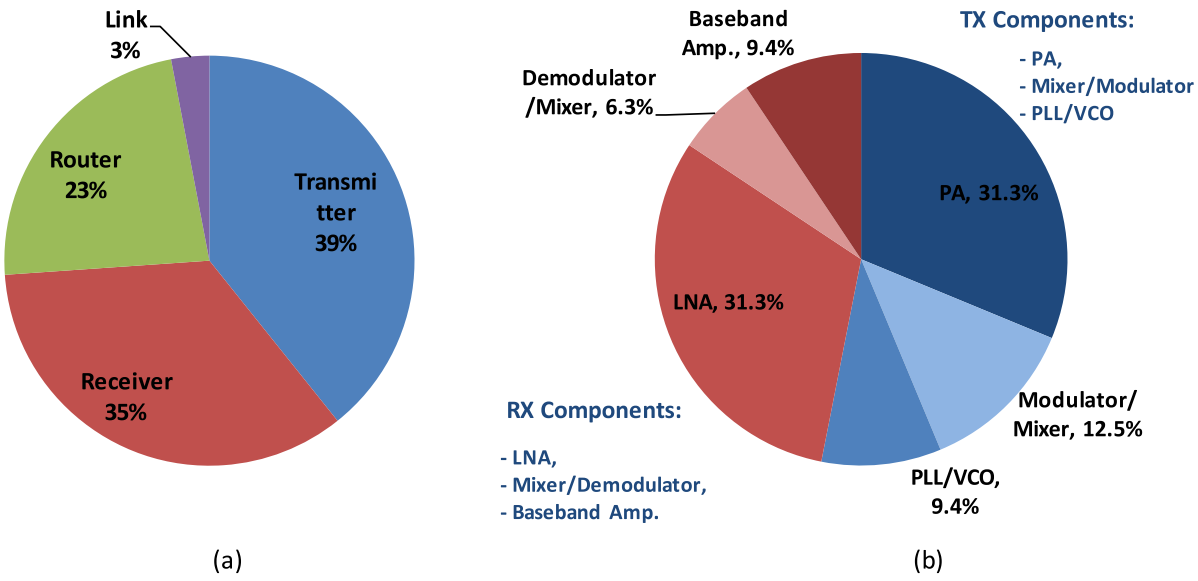

Fig. 3. (a) Power contributions of radio-hub components (the figure is based on [74]); (b) Power consumption breakdown of TX and RX elements (the figure is based on [66]).

and architectures that offer energy efficiency of NoC architectures. As an instance, PG and DVFS, are two major approaches of achieving energy efficiency in both wired NoCs and WNoCs.

The main instances of physical layer and antenna of WNoC are explained in Section 4.1. Then, the WNoC architectures employed the power gating (PG) strategy are reviewed. In the DVFS and VFI-Partitioned section, some approaches focus on varying the voltage and frequency of WNoC to decline power consumption [58]. Section 4.4 studies the offered solutions which use PG and DVFS simultaneously. Enhancing transceiver, in Section 4.5 describes the transceiver-related issues like transmitter, receiver and the research studies about achieving power efficiency through these devices. Moreover, in this section, some examples of energy-efficient and low-power WNoC with various network topologies and routing algorithms are reviewed. Further, heuristic algorithms and approximate communication are two other approaches that affect power consumptions of WNoC architectures that have been investigated far less in comparison with the mentioned strategies. In addition to distributed energy manager, adaptive and semi-adaptive NoC routing algorithms effectively manage congestions and balance network loads, and consequently, improve energy efficiency [14,1,18,3,76].

4.1. Physical layer of WNoC and antenna

The physical layer is the backbone of each wireless network. In this section, we have gathered and compared several papers regarding different wireless on-chip communication fabrics. Table 1 demonstrates some characteristics of wireless interconnections examples using the mm-Wave form, RF-I and SWI. The characteristics include technology (nm), frequency (GHz), energy (pJ/b), transmission range (mm) and type of modulation.

According to the numerous research in the literatures, different approaches have been employed for designing the physical layer of WNoC architectures by utilizing an RF/wireless interconnections [48,84,85,12] to propagate electro-magnetic (EM) signals. In [12], transmission lines as communication shortcuts are used and a two-layer hybrid wired/RF-I architecture was proposed in 90 nm CMOS technology. The transmission line was placed in a rounded Z-shaped topology, guiding waves at the speed of light with the energy consumption of 1.2 pJ/bit. By applying extremely small transceivers in 40 nm CMOS and using ASK modulation, the feasibility of mm-Wave intra-connect appropriate for short-range and high-speed I/O connections was explained in [79]. Furthermore, SWI as a 2D waveguide medium use a dielectric coated metal layer for wireless communication [22]. Among wireless interconnections with mm-Wave style, RF-I style and SWI style, mm-Wave form suffers from free-space high-power dissipation [54].

According to the research in [24], SWI saves more power over mm-Wave under both synthetic and realistic traffic patterns, due of free space propagation resulting in the signal loss in mm-Wave interconnections. An appealing aspect of WNoCs would be assessing the feasibility of using antennas on silicon integrated circuits which was investigated by many researchers for instances [86,87]. In [87], the state-of-the-art of different types of on-chip antennas including zig-zag dipole, meander dipole, loop, slot, inverted F, bow-tie, and Yagi antennas have been presented. The appropriate antenna, which provides the best power gain and least area overhead at the same time, for a WNoC architecture needs to be wideband and have high efficiency plus adequate small size [88]. A metal zig-zag antenna offering these features was presented in [89] for the distribution of a global clock signal. To implement an mm-Wave intra- and inter-chip wireless communication over free space, a metal zig-zag antenna, was illustrated and fabricated in [90]. Furthermore, an mm-Wave WNoC with WIs which have been implemented with zig-zag antenna operating at 62.5 GHz and on–off keying (OOK) transceiver with the data rate of 16 Gbps and 90 mW power dissipation, was reported in [34]. Li et al. have chosen five carrier frequencies centered at 30, 60, 90, 140, and 220 GHz for WI designs, in a way that a few numbers of routers equipped with a wireless port tuned to one of the five frequency channels [91].

Carbon nanotube technology (CNT) operates in the frequency range of terahertz/optical while decreases the size of antennas. Investigated characteristics of these antennas is found in [26,92]. A bandwidth of around 500 GHz could be achieved through CNT antennas. Besides the advantages of using a CNT antenna such as much higher data rates, CNT antennas with virtually defect-free structures do not suffer from power loss compared with conventional metallic antennas due to surface roughness and edge imperfections [93].

Furthermore, the feasibility evaluation of employing graphene-based antennas, operating in the terahertz band (0.1–10 THz), within WNoC architectures, was investigated in [94–97,92,27]. Saxena et al. in [98] provided a hybrid WNoC which utilizes a folding strategy and the graphene-based WIs at terahertz bands. According to statistics reported in [98], the comparison between proposed graphene-based folded WiNoC (GFWiNoC) architecture with an mm-Wave MFWiNoC structure demonstrates that GFWiNoC offers 2.4x lower of average

Table 1
Wireless on-chip interconnection characteristics comparison.

Scheme		Technology (nm)	Frequency (GHz)	Energy (pJ/b)	Trans. Range (mm)	Modulation
RF-I	Wu et al. [77]	65	60	1.33	5.5	ASK
	Chang et al. [12]	90	20	1.2	N/A	BPSK
	Hu et al. [78]	130	N/A	1.67	20	N/A
mm-Wave	Kawasaki et al. [79]	40	56	6.4	14	ASK
	Gade et al. [52]	45	60	1.2	20	OOK, OFDM
	Ahmed et al. [19]	65	60	2.07	20	OOK
	Subramaniam et al. [46] (only receiver)	45	60	N/A	N/A	OOK
	Li et al. [80]	28	30 200	N/A	N/A	N/A
	Yu et al. [75]	65	60	1.2	20	OOK
	Nakajima et al. [81]	65	80	9.4	20	ASK
	Byeon et al. [82]	90	60	6.26	100	OOK
SWI	Liang et al. [83]	65	140	0.32	20	ASK
	Saxena et al. [27]	65	60	0.07 pJ/bit/port	20	N/A

packet energy than MFWiNoC. In contrast to MFWiNoC architecture which has an active single wireless link, GFWiNoC use multiple wireless links at the same time.

Directional log-periodic antennas make the possibility of having multiple concurrent links over a single active connection in a token-based wireless on-chip structure. In [99], the WNoC with directional antennas (DWiNoC) architecture exceeds the token-based WNoC with a comparable topology in terms of bandwidth and energy efficiency. Moreover, antennas orientation as an effective factor on the power consumption of the wireless on-chip architectures was considered in [100]. It was concluded that optimally oriented antennas show up to 80% energy saving in comparison with antennas possessing all the same orientation [100]. Due to limited area of chips, in most of the WNoCs, directional antennas are used for avoiding multipath propagation. With emerging technology, CNT and graphene-based antennas, operating in the terahertz band are more energy efficient than the others.

4.2. Power gating strategy

In this section, we have highlighted the state-of-the-art papers in power gating (PG) as one of the main strategies applied for the energy efficiency of WNoC [101,102,61,1]. The main goal of power gating is shutting down some parts of WI, such as transmitter and receiver, when they are idle. In dark silicon phenomena, due to the power constraints of thermal design, not all of the CMOS devices such as integrated on-chip cores can operate simultaneously [73,102], and on the other hand, leakage power (static power dissipation) can occur during the idle time of WI components as well as base routers for some clock cycles [61].

By utilizing power gating as an effective technique, it will be possible to diminish leakage power. Several papers have presented energy-efficient WNoC through power gating. In [103,101,14], in order to manage power, a centralized controller activates or deactivates a transceiver by sending it into sleep or wake up mode. The power management controller (PMC) in [101] was exploited in four wireless on-chip architectures; NePA WNoC [104], WCube [86], hierarchical IWISE [28]. A major problem of a central mechanism is buffering signals that traversing from/to the central controller result in rising delay, congestion and power consumption [61,105,60,106–108].

To cut off the power consumption, in [109], researchers have proposed WIRXSleep technique. This technique focuses on turning off the receiving parts which will not participate in a certain number of following cycles to reduce both static and dynamic power consumption. An upgraded version of WIRXSleep strategy was presented in [61], namely SiESTA (smart energy saving transceiver) power managing mechanism. Although akin to WIRXSleep, SiESTA results in both static and dynamic power efficiency, the complex structure of SiESTA concentrates on both transmitting and receiving sides of WIs.

Fine-grained router architecture (FGRA) [110], by applying the power gating technique in both base and hybrid routers, can save energy. It was reported that up to 62.50% of WIs static power and up to 88.76% of BRs static power can be saved through FGRA. To decrease power in HRs, power gating was utilized in two most power consumer components of WI (PA and LNA) [110]. Addressing power consumption of LNA and PA components in [102] led into another technique. This approach was presented as a distributed power gating manager. Moreover, it was tried to ameliorate the effects of power gating technique such as voltage drop, wake-up latency, and inrush current and increasing transient energy consumption.

To boost the energy efficiency of WNoC for high-performance computing (HPC), a power gating technique, called energy-proportional multicast scheme (EMS) was introduced. In this method, the routers which should not be the receiver of the multicast message (non-multicast WIs) at the moment will be powered off. Although a fully connected WNoC (one-time sending to multiple receiver nodes) helps to improve the efficiency of cache coherence in HPC, it will result in energy dissipation because of the multicast packet transmission to non-involved members [111,76]. In addition to offering a congestion-aware wireless node, a power control mechanism was proposed in [112]. This method activates the switching off set-up on the defeated WI that competed for the radio channel. The authors of [39] evaluated two low-power multi-chip NoC architectures, one with terahertz and the others with mm-Wave wireless interconnections between sub-networks. Both the WNoCs of [39] use power gating strategy and OOk demodulation at 32 nm technology. Their results shown that terahertz wireless interconnections are more energy-efficient than mm-Wave interconnections. In [19], a wireless network-in-package architecture with multicast support, token-based management and asymmetric wireless structure was presented.

The authors of [37] presented an energy-efficient WNoC architecture for barrier synchronization utilizing power gating and OOk demodulation for 28 nm technology. The authors of [52] an energy-efficient heterogeneous CPU–GPU multi-chip NoC architecture using directional wireless interconnections in order to GPUs and CPUs have direct access to the memory modules. Replica [38] includes a power-gated low-power WNoC architecture and a software interface for supporting wireless protocol for communication intensive and approximate (ordinary) data. In Replica, partially power gating strategy is used only in the PA of its transmitter and the LNA of its receiver.

4.3. DVFS/VFI-partitioned

Following the devices scaling and increasing the number of transistors, the power density will rise quickly on the chip, which results in system temperature increase and system damage as a consequence [113–116]. By balancing the energy consumption, heat spreading on the chip will become low and subsequently keeping the system in lower temperatures [113,117].

One of the popular methodologies being used to lower the power dissipation of electronic systems is dynamic voltage and frequency scaling control technique (DVFS) [118–120]. VFI-based designs divide the

NoC architecture into multiple VFIs and through DVFS the power efficiency of these multicore architectures could become achievable [121–123]. Thus, as a strategy to decline the power consumption of the on-chip network and simultaneously not having a notable effect on the overall execution time, DVFS techniques have been applied [64]. It is possible to implement the DVFS techniques per each core separately, in a centralized or distributed approach [114,116]. Despite requiring complicated hardware in a centralized controller, this approach results in lower area overhead and power consumption, in comparison with a distributed method [116]. In [64], a dual-level DVFS (the processor-level and network-level DVFS) technique with distributed controller was introduced.

DVFS pruning for WNoC was investigated by Murray et al. [124]. They found that the required levels of Voltage/Frequency for the links of the network depend on traffic characteristics after running benchmarks. For example, for some regularly used benchmarks like SPLASH-2 and PARSEC, the majority of links and switches utilize just a few specific V/F states frequently. Due to this finding, a fine-grained DVFS strategy with many V/F states seems unnecessary and implementing a DVFS mechanism with a decreased number of V/F states might be sufficient [124].

A VFI-partitioned design for a small-world-based WNoC in [122,121], published more favorable results for the latency and energy consumption comparing with wired mesh-based counterparts. Another example for a low-power design in [123] is exploiting both VFI and wireless interconnections in running a framework of implementing big data computing on large-scale clusters, called MapReduce resulted in a multicore architecture that meets energy efficiency without imposing penalties in terms of execution time. mSWNoC, a wireless small-world based NoC was proposed in [63] to gain energy efficiency and better latency. Besides, the DVFS method as an extra aid was implemented on wired links to enhance energy consumption.

4.4. PG and DVFS

Applying the advantages of both methods of DVFS and PG simultaneously in WNoC architectures was done in the mentioned and highlighted papers of this section. Centralized nature of the applied mechanism in [103,101] requires the control signal receiving from or sending to the controller to be buffered. This mechanism results in delay, congestion and power consumption rise [61,105]. Gade et al. employed DVFS (in a centralized manner) and power gating methods for WNoC energy conservation [113]. Indeed, the centralized control unit encompasses two modules; Core control unit which is allotted to run DVFS algorithm in cores and wireless control unit which utilizes the power gating approach for WIs [113]. Likewise, the implemented centralized controller in [114], includes DVFS and PG modules which have been applied for cores and WIs respectively.

In [65] both static and dynamic power consumptions have been addressed. To implement adaptive multi-voltage scaling method as a technique for the objective of dynamic power reduction in base router, a distributed controller for managing power was proposed. Furthermore, employing power gating technique in WIs yields reducing leakage power consumption [14,65]. Three popular power saving approaches and their properties are shown in Table 2. For generating a turn-off (or on) signal, power management controller (PMC) is implemented either in centralized or distributed mode. Moreover, the effectiveness of the proposed method got shown by the percentage of power saving or energy-delay product (EDP) saving. The last column of Table 2 shows whether the proposed tactics will incur any performance penalty in terms of area, latency or execution time.

4.5. Enhancing transceiver

In this section, some notable hardware-oriented approaches of power saving have been presented. These methods address one of the main parts of WI, i.e., transceiver. Studies show that using different characteristics of each transceiver components will affect power consumption.

The authors of [126,45] have demonstrated that designs of wireless transceivers in the millimeter-wave (mm-Wave) bands can improve energy budget and increase bandwidth in WNoC and chip-to-chip interconnects. In [126] a wideband amplifier was introduced for a 60 GHz OOK receiver in 65 nm CMOS which is appropriate for using in mm-Wave WNoC transceivers to increase data rate and lessen power consumption and area overhead. Applying a two-stage cascade LNA design in mm-Wave circuits in wireless interconnects for NoC and chip-to-chip communications in [45] has yielded an ultra-low-power compact OOK transceiver. Besides, the feasibility of nano-scale double-gate MOSFETs (DG-MOSFETs) over conventional CMOS was evaluated and introduced as an alternative to implementing this architecture. A 45 nm OOK-based receiver for multiple WNoC architecture was presented in [46]. The authors of [36] designed a unicast/multicast 28 nm transceiver and analyzed the use of some channel correction techniques at 10 Gb/s.

In [27], the authors proposed energy-efficient terahertz-band and graphene-based single-chip and multi-chip WNoC architectures based on network folding approach. WiNN [35] was proposed as an energy-efficient neural network WNoC in 45 nm technology with multicast support and OOK modulation. In [80], an energy-efficient WNoC for brain-machine-body applications was presented. The authors of [80] employed machine learning approaches for networking, link configuration and routing at 30 Gb/s in 28 nm technology. The authors of [45] presented a high-speed transceiver for wireless multi-chip systems. An energy-efficient hybrid 3D WNoC was presents in [9] that employs wireless NFIC (near-field inductive coupling channel) and wired TSV (through-silicon vias) in order to double bandwidth.

An OOK-based WNoC transmitter, operating at 60 GHz with bit-energy efficiency of 1.2 pJ/bit and 19 mW power consumption was presented in [75]. Reported results show that compared with its counterparts [79,127,82,128,129] in terms of power consumption, bit-energy efficiency, active footprint and maximum data rate, the suggested transmitter outperforms them. Regarding another 60 GHz CMOS Transmitter [130] results, with 12.2 mW transmitter power dissipation and 1.1 pJ/bit bit-energy efficiency, it was shown that these results have surpassed result reports of [75]. Recently, an mm-Wave OOK transmitter was designed at circuit level at 60 GHz in [47]. This proper transmitter for both on-chip and chip-to-chip wireless interconnects in 45 nm CMOS dissipates a total power of 3.9 mW and can gain bit energy efficiency of 0.24 pJ/bit.

The architectures of [131,132] are two samples that have addressed low-noise amplifier (LNA) and demodulator parts of receiver respectively. In [131], proposed LNA, in 60 GHz, which has targeted to achieve power efficiency and high bandwidth, consumes a power of 9.4 mW. An OOK demodulator operating at 60 GHz band, fabricated in 65 nm CMOS, was presented in [132]. The implemented demodulator can achieve bit-energy efficiency of 0.25 pJ/bit and consumes 4.6 mW. Besides, a 60 GHz OOK receiver for both inter and intra-chip wireless interconnects was provided in [46]. The receiver dissipates a power of 6.1 mW and offers a bit-energy efficiency of 0.36 pJ/bit. Electromagnetic characterization of the intra chip propagation channel is presented in [84].

Table 3 demonstrates the comparison between some suggested transmitters in the literature. Other characteristics got covered in this table include technology (nm), carrier frequency (GHz), type of modulation, power consumption (mW), bit-energy efficiency (pJ/b) and FoM. FoM (figure-of-merit) [75] is defined as Eq. (1), where PDC shows

Table 2
Three popular power saving approaches and their properties.

Approach	Scheme	Power management controller (PMC)	Power savings	Penalty
PG	Mondal et al. [103]	Centralized	up to 70% (256-core)	Area: (Sleep transistor and PMC 0.2947 mm^2) Latency: 0.4099 ns
	Mondal et al. [101]	Centralized	up to 70%	Area: Sleep transistor 0.0325 μm^2 + PMC: 0.0997 mm^2 Latency: 0.4099
	Catania et al. [109]: WIRXSleep	–	25% total	Area: WIRXSleep 0.11% of radio-hub Latency: no penalty
	Catania et al. [61]: SiESTA	Distributed	up to 80%(WI) up to 25%(total)	Area: Negligible (SiESTA 0.04% of the total radio-hub area)
	Mondal et al. [110]: FGRA	Distributed	static power up to 88.76%(BR) 62.50%(HR)	Area: FGRA 2.42% of Router are wakeup latency: 0.14 ns
DVFS/VFI-Partitioned	Kim et al. [121]: VFI-mSWNoC	–	up to 47.1% (for LU) average = 22.2% EDP	Execution time: 5.8%
	Murray et al. [64]: Dual-Level DVFS WiMesh	Distributed	up to 34%	Execution time: about 7%–28%
	Kim et al. [122]	Distributed	up to 40%	–
	Duraisamy et al. [123]	–	average EDP = 33.7%	Execution time: max of 3.22%
	Kim et al. [125]	Distributed	average EDP up to 60%	Area: Controller 0.06 mm^2 (in worst case scenario)
PGand DVFS	Mondal et al. [114]	Centralized	33.085%(for 6WIs) 69.12%(for 13WIs)	Area: Controller 12.5% of total chip area (for 256 cores)
	Gade et al. [113]	Centralized	Around 6%(average) 33.085%(for 6WIs) 69.12%(for 13WIs)	Area: Controller 0.16 mm^2 (16core) Execution Time: about 8%-18.53%
	Mondal et al. [65]: AMS-based WNoC	Distributed	Overall packet energy: 20%-62.43% Static power per WI: 62.50%	Area: Less than 1%

Table 3
Examples of some transmitter characteristic.

Scheme	Technology (nm)	Carrier frequency (GHz)	Modulation	Power consumption (mW)	Bit-energy efficiency (pJ/b)	FoM
Lee et al. [128]	90 nm CMOS	60	OOK	183	73.2	0.04
Juntunen et al. [129]	90 nm CMOS	60	OOK	156	45	0.04
Chen et al. [127]	180 nm SiGe	43	Binary ASK	57	9.5	0.07
Byeon et al. [82]	90 nm CMOS	60	OOK	31	2.9	1.12
Kawasaki et al. [79]	40 nm CMOS	57	ASK	29	2.6	0.24
Yu et al. [75]	65 nm CMOS	60	OOK	19	1.2	1.19
Byeon et al. [130]	65 nm CMOS	60	OOK	12.2	1.1	1.03
Shinde et al. [47]	45 nm CMOS	60	OOK	3.9	0.24	2.055

the power consumption and OP_{1dB} demonstrates the 1-dB compression point at the RF output of the TX [75].

$$FoM(mW.\frac{bit}{pJ}) = \frac{Data\ Rate(\frac{Gb}{s}) \times OP_1dB(mW)}{P_{DC}(mW)} \quad (1)$$

Through the OOk demodulation scheme, regarding the RF signal modulation and demodulation simplicity, saving significant power in wireless communication can be attainable [75,132,133]. Comparison of some mm-Wave OOK demodulators from literature are demonstrated in Table 4. The power consumption and bit-energy efficiency of the designs, with buffer power and bit-energy included and without them, are recorded in Table 4.

By exploiting runtime tuning transmitting strategy along with a reliability constraint, depending on the receiver location, a configurable transmitter was proposed in [138] to enhance further energy efficiency in the transceiver of WNoC architecture. The variable gain amplifier (VGA) controller is a block which was added to the transceiver to control the transmitting power. Two wireless on-chip architectures, iWISE64 and McWiNoC, got equipped with VGA and compared with their original structures, without VGA, and a wired architecture in terms of energy consumption. Results show power savings in VGA-augmented architectures [138]. To resolve the main weakness of the proposed technique (offline configuration of the transmitter) in [138], an enhanced version was presented in [139].

As Fig. 4 shows, a comparison between three modulation schemes; OOK, binary phase-shift-keying (BPSK) and quadrature phase-shift-keying (QPSK) has done in [66]. With regards to the results, QPSK obtains twice the bandwidth as compared to OOK. However, in terms of power consumption, OOK provides better energy efficiency. Fig. 4 shows the power consumption and energy efficiency of OOK, BPSK and QPSK modulation schemes.

A-WiNoC (adaptable WNoC architecture), a hybrid wired/wireless NoC architecture, utilized adaptable transceivers to improve energy efficiency and performance at the same time [140,72]. For communication in this architecture, wireless channels have been adapted according to traffic patterns. [72] was introduced as an augmented version of [140], which provides the experimental results of a scalable WNoC architecture of 256 cores. The base of the applied technique in [140,72] is thoroughly efficiently employing the wireless bandwidth. Table 5 reviews examples from literature of transceivers with different modulations for short-range wireless communication.

4.6. Structure and network topology

The purpose of this section is to review several studies on the effect of node topological structure of WNoCs. A hierarchical architecture using mm-Wave wireless links in which some connected cores through traditional wired (subnets) are located at the lower level and the hubs

Table 4
Mm-Wave OOK demodulator comparison.

Scheme	Technology (nm)	Carrier frequency (GHz)	Power Consumption (w/o Buffer) (mW)	Bit-Energy efficiency (w/o Buffer) (pJ/b)	Supply Voltage (V)
Yodprasit et al. [134]	250 SiGe	60	27.5	2.4	1.6
Byeon et al. [82]	90 CMOS	60	19.2	1.8(0.56)	1.2
Foulon et al. [135]	130 SiGe	60	21	2.1	2.5
Uzunkol et al. [136]	120 SiGe	55	(0.75)	(0.13)[a]	1.5
Oncu et al. [137]	90 CMOS	60	49(35)	7(9.8)	1.2
Yu et al. [132]	65 CMOS	60	11.6(4.6)	0.62(0.25)	1
Subramaniam et al. [46] (only receiver)	45 CMOS	60	(1.3)	(0.08)	1
Gade et al. [52]	45 CMOS	60	1.2	20	1
Ahmed et al. [19]	65 CMOS	60	2.07	N/A	1
Subramaniam et al. [46] (only receiver)	45 CMOS	60	3.27 (only receiver)	0.36	1

[a]External baseband amplifier is required that consumes ~ 150 mA [132].

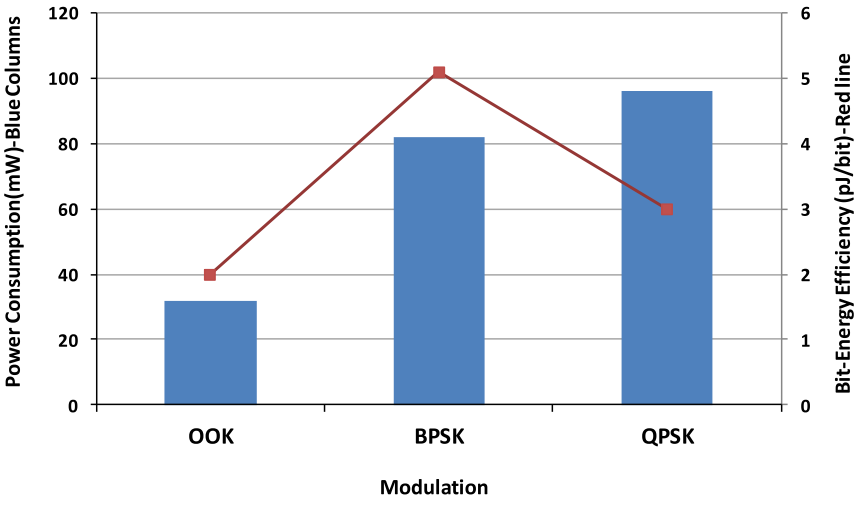

Fig. 4. Comparison between OOK, BPSK and QPSK modulation schemes (the figure is based on [66]).

Table 5
Examples for transceivers characteristic using for short-range wireless communication.

Scheme	Technology (nm)	Carrier frequency (GHz)	Modulation	Power dissipation (mW)			Energy efficiency (pJ/bit)	Data rate (Gb/s)	Chip area (mm^2)	
Byeon et al. [82]	90 CMOS	60	OOK	67	TX:31	RX:36	6.26	10.7	TX:0.15	RX:0.29
Lee et al. [128]	90 CMOS	60	OOK	286	TX:183	RX:103	86.7	3.3	TX:0.43	RX:0.68
Kawasaki et al. [79]	40 CMOS	56	ASK (Coherent)	70	TX:29	RX:41	6.4	11	TX:0.06	RX:0.07
Wang et al. [141]	65 CMOS	60	BPOOK	100	TX:78	RX:22	33.3	3	TX:1.20	RX:0.36
Chen et al. [127]	180 SiGe	43	Binary ASK		117		17	2–6	0.62	
Marcu et al. [142]	90 CMOS	60	QPSK	308	TX:170	RX:138	–	4		6.875
Juntunen at al. [129]	90 CMOS	60	OOK	264	TX:156	RX:108	TX:45, RX:31	3.5		4.14
Byeon et al. [143]	65 CMOS	60	OOK	33.1	TX:12.1	RX:21	2.65	12.5	TX:0.09	RX:0.06

are located at the upper level in a small-world-based structure with the wired and wireless links was presented in [34]. According to [34], two interconnection methodologies (mesh and ring) as samples have been illustrated in Fig. 5. Although in [34], the main goal is to show the superiority of utilizing the wireless feature over conventional wired interconnect, it was reported that mesh-mesh-based architecture with wireless shortcuts attains higher performance in terms of packet energy per bandwidth compared with ring-mesh architecture with wireless shortcuts.

Regarding the results of the average power dissipation per packet in a 256-core WNoC architecture, called iWISE in [28], iWISE saves power in comparison with WCube [86] as another wireless structure. As Fig. 6 shows, iWISE is a hybrid NoC architecture in the mm-Wave frequency range with distributed wireless hubs as opposed to a centralized hub-based structure [28]. While, WCube was defined as a recursive WNoC architecture using sub-terahertz wireless links, a hybrid topology with a two-tier structure in the form of wireless backbone and wired

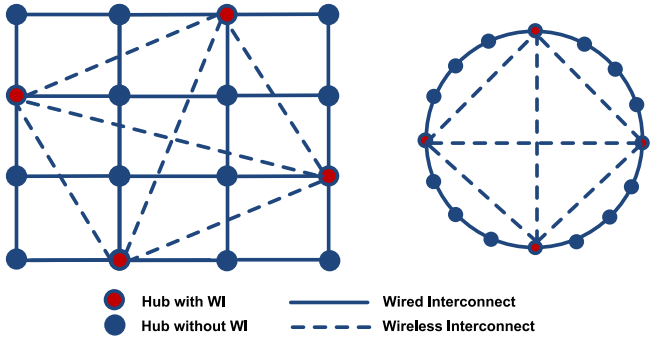

Fig. 5. Mesh and ring topologies using for hub interconnection [34].

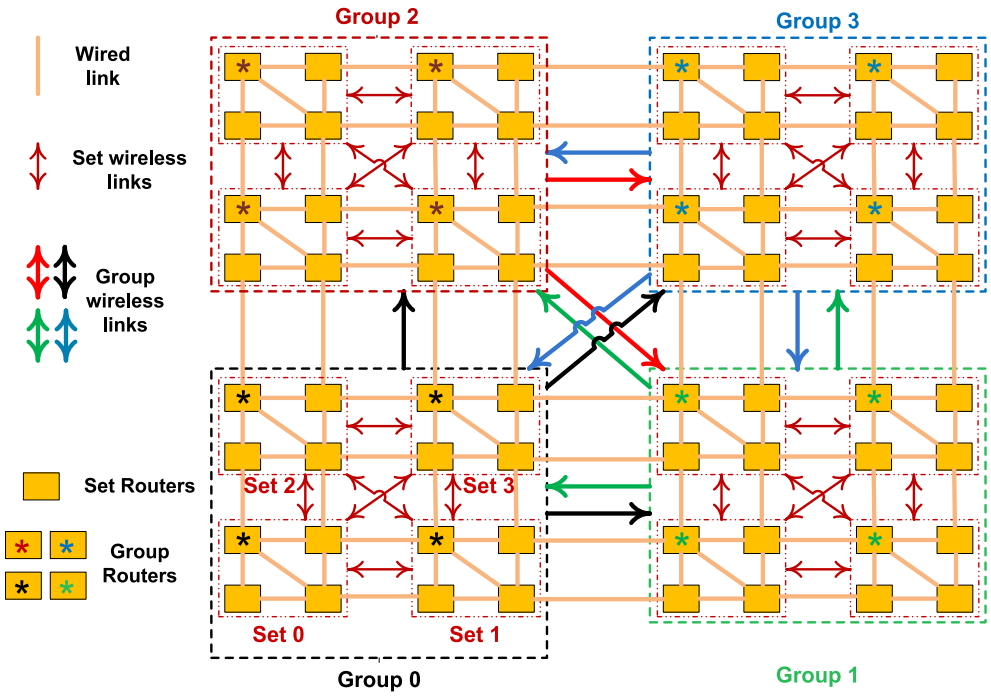

Fig. 6. iWISE architecture [28].

edges [86]. As another instance of low-power WNoC, [32] reported power consumption of HiWA (hierarchical wireless-based architecture), a mesh-based structure which was divided into square subnets, versus conventional WNoC architecture.

A partitioned and directory-based architecture, equipped with wireless routers was presented in [144]. Faster routing decision could be possible since the centralized directory holds track of each subnet by using customized MESI protocol. Although comparing with traditional WNoC in terms of power consumption, the WNoC architecture proposed in [144] saves more energy, it has some disadvantages including delay and hop count.

With the aim of lessening communication delay, hop count and power consumption, the authors of [145] presented a WNoC architecture with distributed directories (WNoC-DDs). Fig. 7 illustrates WNoC-DDs architecture. The directory is responsible for offering an adaptive minimal routing path, and a wireless router is located in each subnet of a partition-based structure. Experimental results depict the superiority of WNoC-DD in comparison with WNoC-CD [144] architecture especially in terms of power consumption. Partitioning the network into subnets through a uniform WNoC-DD (with the same number of cores) and non-uniform WNoC-DD (with different sizes of each subnet) was investigated in [146]. The results have illustrated that the non-uniform structure consumes lower power than the uniform one.

As another example, by applying a two-level hierarchical interconnection scheme, a hybrid mesh-based WNoC was proposed in [147]. Furthermore, combining wireless and photonic technology led to optical-wireless NoC [148,7,149,8] as a high-cost and energy-efficient hybrid architecture. It was demonstrated that OWN consumes lower power comparing with wireless-CMESH [86]. It is important to mention that the energy-saving strategies (e.g., clustering and zoning) that utilized in wireless sensor networks [150–155], are efficient to be employed in WNoC architectures for reducing power consumption and improving energy efficiency.

Compared to mesh-based architectures, on-chip network architectures with honeycomb topology [14,156,33,18] provide higher performance especially in terms of energy consumption and delay, with the same regularity, symmetry and scalability. HoneyWiN [33,18] is an energy-efficient hybrid WNoC and is based on honeycomb topology

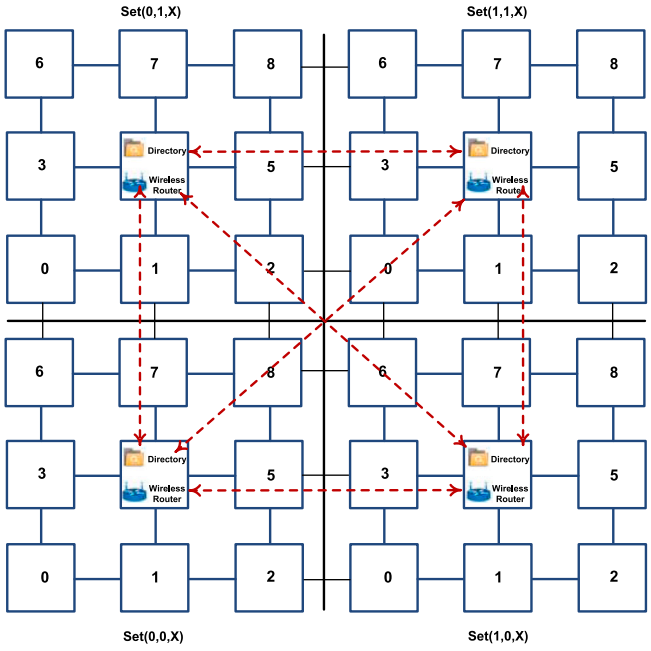

Fig. 7. WNoC-DDs architecture [145].

(Fig. 8). HoneyWiN outperforms its mesh-based hybrid WNoC counterpart in terms of power savings while still raises the network throughput. Indeed, HoneyWin tried to challenge the prevailing assumptions of the superiority of mesh as the backbone topology of WNoCs. Another Honeycomb-based architecture is H^2WNoC [14] as an energy-efficient WNoC architecture aiming at reducing hardware resources and network cost. The routing algorithms of HoneyWin and H^2WNoC are adaptive and based on XYZ and the ant colony optimization approach for honeycomb zones. H^2WNoC structure is very compatible with the internal structure of reconfigurable devices like FPGA architectures. Alaei et al. demonstrated that H^2WNoC provides less power consumption

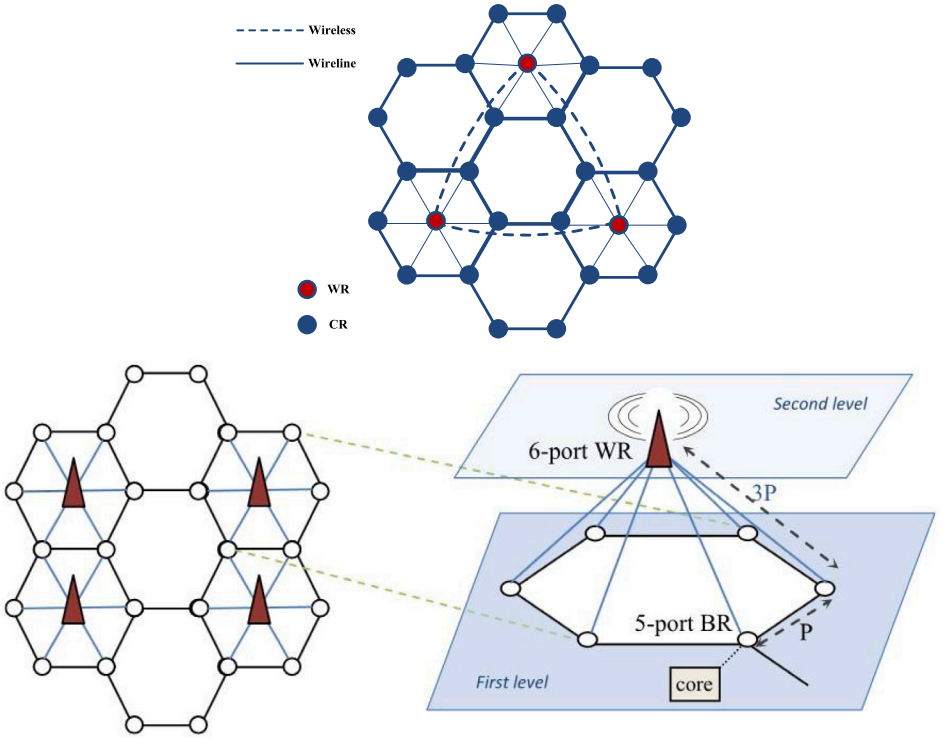

Fig. 8. HoneyWiN architectures [33,18,14].

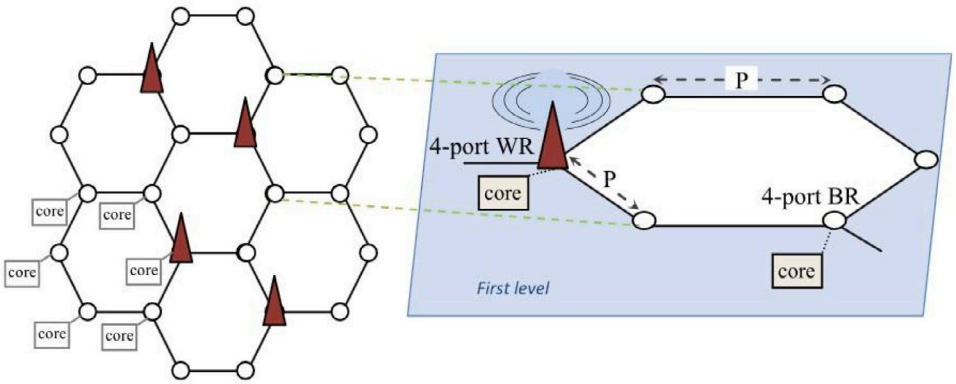

Fig. 9. H^2WNoC architectures [14].

and less average delay than relevant WNoC architectures, e.g., HoneyWiN, HiWA and amsWNoC with higher network throughput [14]. (See Fig. 9).

4.7. Routing algorithms and congestion management

Routing algorithms have significant effects on the performance of on-chip network architectures [157,158,72]. The complexity and cost of routing algorithms according to their characteristics such as using tables, adaptivity, using virtual channels affects the amount of power consumption of NoC and WNoC architectures. It is important to mention that deadlocks and livelocks considerably degrade the performance of on-chip network architectures. Deadlocks and livelocks reduce network throughput and power consumption, and also increase average latency. Therefore, it is essential to prevent or remove deadlocks and livelocks by designing efficient low-cost routing algorithms [14,1].

By applying the parameter of the local router range which was determined at the design phase statically, a dynamic energy-aware algorithm was introduced in [159]. In a multi-level NoC, the routing algorithm ascertains the optimum local router range by dynamically changing the traversal direction of packets to enhance routing decisions. Optimizing the energy profile of the NoC architecture ends in declining both energy consumption and delay of the network at the same time [159,14].

Three irregular routing strategies for mSWNoC architecture were investigated in terms of latency, energy dissipation, and thermal profiles in [160,161]. The first routing approach is multiple tree roots (MROOTS) [162]; an up/down tree-based routing structure. The second routing approach is LASH algorithm that using the layered shortest-path routing algorithm along with the multiple virtual channels in every port of on-chop routers [162]. ALASH algorithm [162] is the third routing method that is made upon the layered shortest path (LASH) algorithm with the advantage of more flexibility by allowing the message to choose its path in an adaptive way. Regarding the present condition of the network like virtual channel availability and current communication density, the decision for switching path is being made. By applying these three routing strategies in mSWNoC, lower latency and energy dissipation is achievable comparing with wired counterparts [160,161].

The authors of [157] studied the effect of virtual channels, partitioning and routing algorithm on performance and energy consumption of WNoC architecture. The authors of [163] presented a low-power, congestion-aware, pre-avoidance and load-balanced WNoC with a dynamic routing algorithm according to learning approaches. With the goal of congestion management and energy conservation, a multi-channel mm-Wave WNoC architecture with a dynamic medium access control (MAC) mechanism was presented in [108]. NeuMAC [164] is as an adaptive and dynamic MAC protocol for WNoCs. NeuMaC combined the features of neural networks and deep learning for congestion control and rapid adaption with the network load and traffic using 45 nm technology.

4.8. Heuristic approaches

In WNoCs, bio-inspired, heuristic/meta-heuristic algorithms (e.g., simulated annealing (SA), particle swarm optimization (PSO), and ant colony optimization (ACO)) have been used for routing, load balancing, congestion control, energy consumption management, task mapping and link allocations and also for finding the optimal place and number of WIs. The optimal number and the optimal location of the WIs have been investigated by several researchers for instance [32,1,31,18]. In order to find the optimal position of WIs to get maximum benefits of using the wireless links and to be energy-efficient, in [31], the simulated annealing optimization technique was utilized. In [32,14,18], routing algorithms based on the ant colony optimization (ACO) heuristic were adapted for improving energy efficiency. It is noticeable that fuzzy-based NoC routing algorithms provide high-performance and energy-efficient architectures [76,165,156,166], but with considerable area overhead due to fuzzy-based control and its database storage.

Task mapping of high computing applications on processing elements of on-chip architectures is a non-deterministic hard problem that should be solved using optimization approaches. Obviously, the NoC performance metrics (i.e., latency, power consumption, reliability, area, and thermal distribution) mainly depends on efficient task mapping technique. Different mapping policies using heuristic algorithms, have been explored to analysis their effect on power consumptions of wired and wireless NoC architectures [167–176,10,177–181]. An analytical survey on task mapping strategies presented in [182]. Most of these approaches provide high performance and energy-efficient NoC architectures and are usable for application mapping on WNoC architectures.

4.9. Approximate communication

Approximate communication as another approach is employed to manage power consumption of WNoC architectures [183,184,38]. According to this concept, reducing the voltage swing of a bit-line resulted in reducing energy consumption. Although, this reduction may cause reducing the link reliability, the router was expanded by a hardware module, tuning the voltage swing of a link at the run-time and simultaneously considering the trade-off between energy and BER as the link reliability factor [183]. Approximate communication approach has not vastly been utilized due to challenging implementation and reducing reliability of the whole architecture. The methods for compensating the reliability lost come with the cost of area and complexity.

As an extension of the approximate computing paradigm and a trade-off between energy consumption and communication reliability, Ascia et al. proposed the xWiNoC architecture [184]. For the wired part of architecture, they have applied reconfigurable voltage swing links. Furthermore, addressing WIs, according to the required reliability level, they used tunable transmitting power for the wireless elements, which is possible to utilize different voltage swing levels. Utilizing this approach, up to 50% of communication energy saving can be achieved. The cost of this approach is reducing reliability [184].

5. Discussions

High performance computing architectures including dataflow and/or von-Neumann processors [185] and application-specific accelerators [186,187] should be able to handle large amount of parallelisms. Different levels of parallelism are achieved using a large amount of processing elements [185,188]. NoCs and WNoCs are the promising network infrastructure for connecting these processing elements. Since, energy efficiency is one of the principal design constraints of on-chip networks; the scope of this research is energy conservation approaches. In the previous section, we classified the energy saving techniques and analyzed the structural characteristics and the architectural features of each technique.

In Table 6, the main examples of WNoC proposals are categorized based on power saving strategies. In addition, the table manifests whether the offered methods are utilized and simulated (or implemented) in some WNoCs instances. As the table shows, most of the state-of-the-art WNoCs are complete architectures and based on mesh topology. Some related research, such as the papers in Section 4.5, are merely hardware-oriented. These approaches concentrate on presenting a circuit-level design with a complete list of characteristics and comparison with other circuit-level designs characteristics. In the most proposed schemes in enhancing transceiver section, the researchers focus on the only circuit-level design. Although exploiting such augmented versions of transceivers of WNoC architectures have not been investigated in the existing papers, using a power-efficient component might improve the whole network energy efficiency.

As a common approach for designing energy-efficient multicore chips, VFI-based designs rely on partitioning the whole chip into several clusters and then designating each core to one group with regards to the computation and communication aspects of the cores. Moreover, determining a proper voltage/frequency (V/F) pair for each cluster and fine-tuning of each V/F pairs, considering the performance limitations, help to obtain energy efficiency. The main overheads of VFI-based architectures are area, and also execution time in some cases.

In power gating technique, a management unit controls the activity of the modules (transmitter, receiver, buffers and router) and runs a mechanism of activating or deactivating WI components to achieve power efficiency. The motivation behind this approach is to reduce the static power consumption. Although the power gating technique is the most common approaches for reducing the power consumption in the wired and hybrid wire/wireless routers, the main overhead of power gating technique is area. Using dynamic and distributed power gating considerably alleviates the area overhead [1]. In addition, the clock gating strategy and global-to-local link conversion helps to reduce power consumption and to reduce area overhead [1].

The goal of most of the routing algorithms of the on-chip networks is providing low latency routing and balancing network loads. One of the main results of fast and congestion-aware routing algorithms is energy conservation. The challenging issue of this strategy is specific designing of a high-performance routing algorithm considering all situations but this imposes area overhead. Employing different heuristic algorithms for energy-efficient routing, task mapping and WI placement introduce area and complexity cost.

In WNoCs, the wired routers consume high energy, thus employing any power saving strategy in routers causes reducing power consumption of the whole architectures [1]. These strategies include power gating, dynamic buffer allocation, bypass-paths and designing the router control unit in a reconfigurable and distributed manner [3,14,1,189,72,190,191,28,192]. In addition, the policies and strategies for improving fault-tolerance and reliability of WNoC architectures cause to increase power consumption and area due to more complex routing algorithms and more hardware resources [193–195,60,196,197]. Therefore, various energy saving techniques should be employed in designing fault-tolerant WNoC architectures.

Table 6
Summary of the state-of-the-art WNoC architectures.

Approach	Scheme	A complete architecture	Base structure
Physical layer	(Using mm-wave)		
	Kawasaki et al. [79]	×	×
	Yu et al. [75]	–	Small-world[a]
	Nakajima et al. [81]	×	×
	Byeon et al. [82]	×	×
	(Using SWI)		
	Liang et al. [83]	×	×
	Karkar et al. [22]	✓	Mesh
	Agyeman et al. [24]	✓	Mesh
	Saxena et al. [98]: GFWiNoC	✓	Mesh
	Shamim et al. [99]: DWiNoC	✓	Small-world
	Mineo et al. [100]	✓	Mesh
Power gating	Mondal et al. [103]	✓	Mesh
	Mondal et al. [101]	–[b]	Mesh
	Catania et al. [109]:	✓	Mesh
	WIRXSleep	✓	Mesh
	Catania et al. [61]: SiESTA	✓	Mesh
	Mondal et al. [110]	✓	Mesh
	Baharloo et al. [39]	✓	Mesh
	Ahmed et al. [19]	✓	Mesh
	Mondal et al. [37]		
DVFS/VFI-partitioned	Kim et al. [121]: VFI-mSWNoC	✓	Small-world
	Murray et al. [64]: Dual-Level	✓	Mesh
	DVFS WiMesh	✓	Small-world
	Kim et al. [122]	✓	Small-world
	Duraisamy et al. [123]	✓	small-world
	Kim et al. [125]		
PG and DVFS	Mondal et al. [114]	✓	StarRing
	Gade et al. [113]	✓	Star-Ring-hubs
	Mondal et al. [65]: AMS-based	✓	with Mesh
	WNoC		Mesh
Enhancing transceiver	Lee et al. [128]	×	×
	Juntunen et al. [129]	×	×
	Chen et al. [127]	×	×
	Byeon et al. [130]	×	×
	Shinde et al. [47]	×	×
	Yu et al. [132]	×	×
	Yu et al. [66][c]	✓	Small-world
	DiTomaso et al. [140]:	✓	Mesh
	A-WiNoC	✓	Mesh
	DiTomaso et al. [72]:	✓	Multi-chip mesh
	A-WiNoC (extended version)	✓	Multi-chip mesh
	Subramaniam et al. [46]	✓	Multi-chip mesh
	Sosa et al. [36]	✓	Multi-chip mesh
	Saxena et al. [27]	✓	Multi-chip mesh
	Liu et al. [35]	✓	Multi-chip mesh
	Li et al. [80]		
Structure and network topology	Deb et al. [34]	✓	Mesh and Ring
	Lee et al. [86]: Wcube	✓	k-way
	DiTomaso et al. [28]: iWISE	✓	concentration
	Rezaei et al. [32]: HiWA	✓	Mesh
	Afsharmazayejani et al. [33]:	✓	Mesh
	HoneyWin	✓	Mesh
	Yazdanpanah et al. [18]	✓	Honeycomb
	Alaei et al. [14]: H2WNoC	✓	Honeycomb
	Asaduzzaman et al. [144]	✓	Honeycomb
	Chidella et al. [145]:	✓	Mesh
	WNoC-DD		Mesh
	Chidella et al. [146]		Mesh
Routing algorithm	Pano et al. [159]	✓	Mesh
	Wettin et al. [161]	✓	Small-world
	Wettin et al. [160][d]	✓	Small-world
	Jog et al. [164]: NeuMAC	✓	Mesh
Approximate Communication	Ascia et al. [183]	✓	Mesh
	Ascia et al. [184]: xWiNoC	✓	Mesh

[a]Proposing of using a hierarchical WNoC architecture.
[b]Evaluating four WNoC architectures from [28,86,104].
[c]Using mSWNoC (a multi-channel mm-Wave small-world wireless NoC).
[d]Evaluating mSWNoC along with three irregular routing methodologies (MROOTS, LASH, and ALASH [162]).

The amount of energy consumption of a WNoC is related to the number of hop when the traffic is uniform and static. In real applications, the packet distributions is non-uniform and dynamic, therefore, we cannot determine the optimal number of hop counts. Routing packets through the paths with several hops without congestion consumes less energy than using the shorter paths (less number of hops) with congestion and or blocked nodes. Since buffers are one of the most power-hungry components in WNoCs, removing the buffers of routers and WIs would considerably decrease the power consumption, but the throughput and reliability considerable decrease. The optimal number of buffers to trade-off power consumption and throughput would be determined through a complete design space exploration of the whole WNoC considering routing algorithm, topology, injection rate, traffic pattern, packet and buffer sizes, and the microarchitecture of router.

6. Conclusion

Reducing power consumption as one of the fundamental challenges of WNoC architectures has inspired many researchers to explore the techniques and approaches toward energy efficiency. In this paper, we presented a systematic and categorized review of energy-saving strategies for WNoC architectures. We analyzed different aspects of WNoC architectures, from the physical layer, topology and hardware components to routing and managing energy during execution time. We discussed the advances, trends, corresponding research gaps and open challenges of various energy saving techniques. Researchers can provide new solutions around the declining power consumption of WNoC by conducting the following research suggestions. As some mentioned approaches in this paper using a combined manner such as DVFS and PG, it might inspire researchers to investigate the feasibility of using other hybrid methods of energy efficiency (like utilizing SWI as a two-dimensional media and PG simultaneously) in future research works. In addition, for WNoC architectures, different task mapping and link allocation approaches using heuristic approaches can be explored to analyze the effect of different mapping policies on the power consumption of WNoCs. Furthermore, due to heat and temperature challenges stemming from the high amount of power consumption, novel cooling techniques can be targeted as interesting issues for researchers. Finally, Other based topologies such as tree, torus, butterfly fat-tree (BFT) and 3D NoC can be studied to find out more details about the effect of topology and structure on the energy efficiency of WNoCs.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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