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Roadmap for machine learning based network-on-chip (M/L NoC) technology and its analysis for researchers

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Abstract

A few decades ago, communication inside the chip is done by transferring signals between the cores. This conventional method is not worthy because of the increase in latency and power consumption. To rectify this issue Network-on-Chip (NoC) technology has emerged. NoC technology is invented to transfer data packets instead of signals. Machine Learning NoC (M/LNoC) is a very fast-growing technology in today's Integrated Circuit world for the communication between Intellectual property (IP) cores. The machine learning algorithms are used in the existing and emerging novel NoCs. In this paper, various evolving NoC technologies to decrease the transfer latency, power consumption of the IC is addressed for the implementation of the machine learning algorithm. The NoCs working with machine learning algorithms are called M/L NoC. We also provided the security issues to be focused-on in the M/L NoC. Also, we have provided the available NoC tools for the NoC researchers.

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1. Introduction

Multicore Integrated Circuits are popular nowadays due to its high performance. Interconnection inside a chip is very important for proper communication between the Intellectual property (IP) cores. In multicore chips, the delay is mainly due to lengthy wires that affects the overall performance of the chip. The wire temperature also increases during the signal transfer between two distant IP cores. To eliminate those disadvantages in the conventional method, the NoC technology has emerged. This technology transmits digital packets instead of analog signals. The architecture of NoC contains (i) Intellectual Property (IP) core (ii) NoC Router (iii) Network Interface (iv) Topology (v) Channel.

IP core is a chip that provides the Intellectual property of the vendors. In a multicore processor, many IPs are incorporated in a single chip as illustrated in figure 1. These IPs inside the chip can be homogeneous or heterogeneous. Homogenous SoC contains IP cores with the same characteristics and Heterogeneous contains IP cores with different characteristics [1].

The router in the NoC architecture is to route the packets to the exact destinations. Most of the NoCs follow the multicast routing technique to achieve high speed. Multicast routing is the method to send packets from a single source to different destinations. NoC router needs an algorithm to route the packets via shortest path. The NoC algorithm plays a significant role in the transmission and reception of packets. Designing a perfect NoC router may reduce the area of multicore chip as illustrated by the authors in the work [2]. Researchers in this NoC area concentrate in developing NoC algorithms for achieving high-speed communication. The NoC routers use either circuit switching or packet switching technology for data transfer. Circuit switching and packet switching are useful for less complex and high complex switching paths respectively. The speed of the circuit switching depends on the distance between the source and the end node. The speed of the packet switching depends on the type of router used. Packet switching has more advantage than circuit switching in terms of traffic, data transfer speed etc [3]. Most of the NoC architectures are designed to use packet switching instead of circuit switching. Compare to the other packet switching, wormhole packet switching is accurate and fast. Hence, researchers are giving priority to wormhole packet switching. In this switching, messages travelling from a core to another core are divided into several data packets. This process is called Packetization.

The router communicates with the IP core through Network Interface (NI). The NI is connected with IP core in one side and the router in the other side. NI divides the data packet into flits (Flow Control Units) to speed up the data transfer. This process is called the Flitization process. The flitization process occurs at the source node and at the destination node these flits are recombined to form packets. Each flit is made up of one or more physical unit called as Phits. For Example, a message is divided into 'p' number of packets; Each packet is splitted into 'm' number of flits; Each flit is again splitted into 'n' number of phits [2]. Each flit contains a header, body, and tail flit. The header flit consist of the routing information such as the address details of the source, destination, and the path details from the source to destination. The other flits like body flit and tail flit followed the header flit. The NI assembles the order of flits and inserts the header information.

The topology used in the NoC plays an important role to reduce the latency and the power consumption [4]. The important parameter in the design of algorithm is the NoC topology. Each node of the NoC topology contains the IP core and the router. The IP core and the router is connected via NI. Some of the topologies used by the researchers [5] in their work are Ring, Star, Mesh, Torus, Binary-Tree, Fat Binary Tree, Butterfly, and SPIN. The authors of [6] stated various factors to be considered in topology research are node degree, diameter, link complexity and the bisection width.

Channel is a medium of NoC through which the packets are transferred from the source node to the destination node. There are two types of medium available in NoCs. They are (1) Wired medium (2) Wireless medium. The components of NoC architecture explained above are obligatory to design any type of NoC. NoCs are designed with different routing algorithms, modes of data transfer and additional features. Recently, machine learning algorithm is used to develop the routing algorithm of NoC to improve its performance.

In this paper, section 2 illustrates the various NoC technologies available for the implementation of Machine Learning. Section 3 focuses on the emerging research area in NoC. Section 4 illustrates various tools available for NoC research. Chapter 5 illustrates the conclusion.

2. NoC Technologies for the implementation of machine Learning

As the conventional communication consumes more power because of the lengthy interconnection wires, express channels (also called low power express channels) are introduced on the wire. As these express channels are also basically metal wires, it also consumes more power [7]. It leads to the emerging of other NoC technologies such as Wireless/RF/Millimeter-wave Network-on-Chip, Hybrid Wireless Network-on-Chip, 3D NoC, Photonic Network-on-Chip, etc are proposed to reduce these problems. Recently Machine Learning (M/L) techniques is implemented on the above NoCs to achieve high performance.

2.1. Wired NoC

Wired NoC is the conventional NoC communication inside the chip [8]. This method can use any of the available topologies according to the usage of the chip. In Wired NoC, metal wire is used to connect two nodes. The data transfer process can be done only through this metal wire. A lot of researches were already done in this area to improve its performance parameters. In this structure, each node contains an IP core. The IP core is attached to the NoC wired router through the Network Interface Unit. As communication is through the metal wire, the speed of the data transfer is considerably higher than a few of the other NoCs [9]. Many algorithms are developed to reduce the latency and the power consumption of this NoC. This wired NoC can be designed with 2D and 3D architectures.

2.2. Wireless/RF/millimeter-waveNoC

Wireless NoC is the emerging NoC technology [10]. The wired routers at the nodes are replaced with wireless routers. The router in a node is communicating with the other routers through wireless technology. The same procedure is followed for both neighbour nodes as well as the long-distance node. This requires a lot of power for the transmission. The latency is also not considerably reduced in this technology. By using this method, the area of the chip will be considerably reduced, as it does not use the metal wire for the connection between the nodes [11]. The physical faults due to the metal interconnection will be avoided in this method. Wireless NoC does not achieve 100% throughput during communication due to the packet loss. The packet loss of wireless NoC is higher than wired NoC.

2.3. Hybrid network on chip

Hybrid NoC or Hybrid wireless NoC performs both wired communication and wireless communication for its operation visualized in figure 2. This NoC uses wired communication for short distance communication and wireless communication for long-distance communication. Compare to the wireless NoC, this hybrid NoC shows improved performance results [12]. In some research, the wired NoC router is replaced with wireless

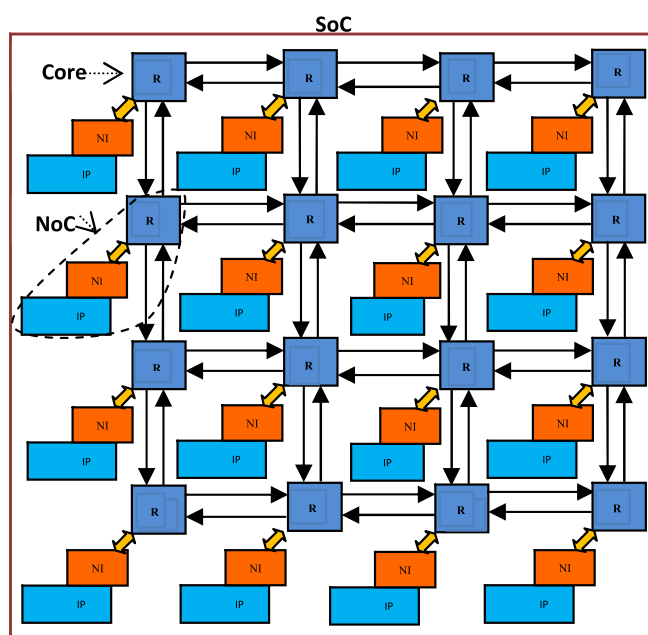


Figure 1. Hybrid NoC structure.

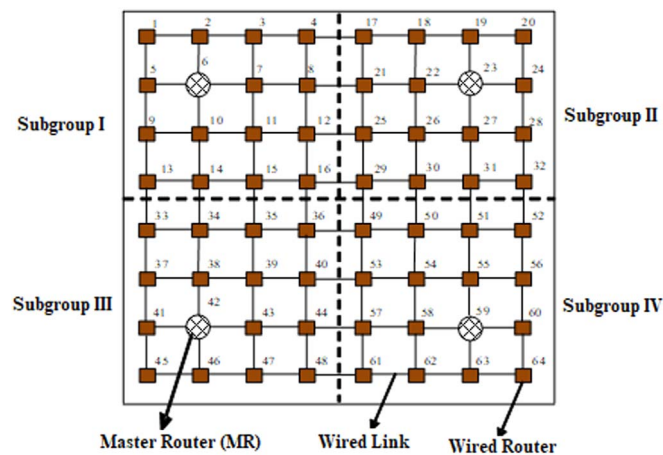


Figure 2. Hybrid NoC structure.

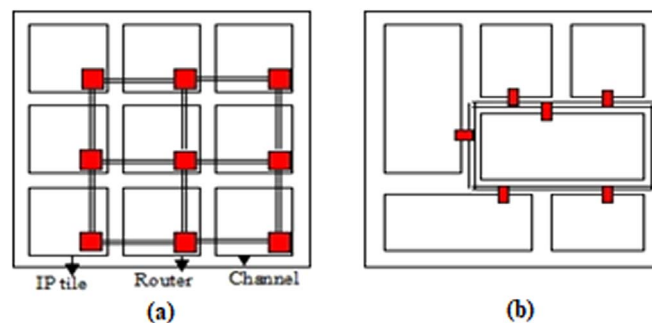


Figure 3. Structure of 2.5D NoC (a) Homogeneous (b) Heterogeneous.

router but in some cases, additional wireless routers will be added along with the required number of wired routers.

2.4. Two-point five dimensional (2.5 D) NoC

The 2.5D NoC architecture has two silicon substrates placed on the top of the parent silicon substrate. The authors of [13] stated that out of the two silicon layers, one is homogeneous and another one is heterogeneous. In the homogeneous layer, the IP cores are arranged uniformly by perfect floor planning techniques [14] as shown in figure 3(a). In the heterogeneous silicon layer, the IP cores are not arranged uniformly but randomly by floorplanning techniques as shown in figure 3(b). Layers in SoC provides improved performance by using appropriate buffer size, mesh size, optimized virtual channels. The authors in the work [14] specified the advantages of using a heterogeneous compact layer by providing optimal floor planning and wiring. Their experimental results shows considerable amount of performance improvement compared to 2D NoC. The authors of [15] proposed another 2.5D integrated multicore network-on-chip with heterogeneous components in each of the two silicon die. The heterogeneous components in the silicon die are 8 MIPS microprocessor core, memory, and accelerator. The designed 2.5D NoC architecture is verified for many digital applications. They designed a 65 nm technology chip operated at 0.5 GHz with 1.08 W power dissipation for a 1.2 V supply. To avoid the thermal challenges, the authors proposed 2.5D NoC which uses an interposer. The interposer in the chip is a normal silicon chip in which metal layers are facing the upward direction. The interposer is designed with small input-output pads, clock generation, and all other types of signalling, etc. Many IP cores [15] such as CPU, GPU, DRAM, NVRAM, are placed on the top of the silicon interposer. These IP cores are mounted horizontally on the interposer. The IP cores are communicated through metal contact and the interposer. The metal connectors are used for the core to core communication and TSVs (Through Silicon Via) are used for vertical communication. In this 2.5 D technology, complete wireless technology is not yet used so far.

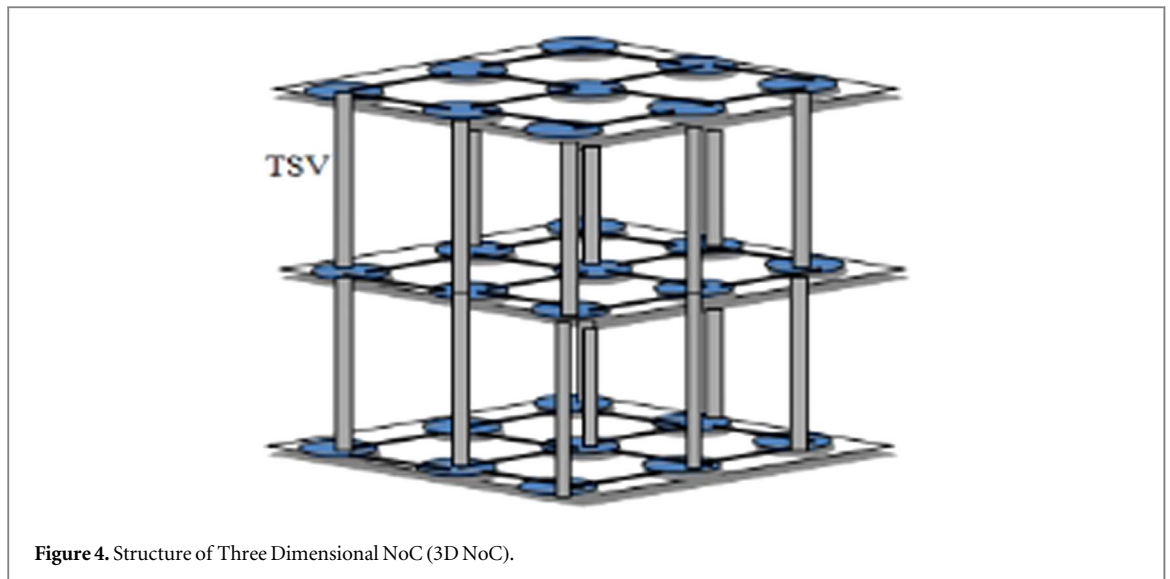


Figure 4. Structure of Three Dimensional NoC (3D NoC).

2.5. Three dimensional (3D) NoC

The two dimensional (2D) NoC performs an efficient operation for many applications. As the functions of electronic devices such as computers, laptops, mobile phones, notebooks, etc are getting more and more complex, the chip designer looks for other options in the NoC area. This leads to the invention of 3D NoCs. Three-dimensional (3D) NoCs are a very popular and fast-growing technology in the IC era to achieve high-speed data transfer in SoCs. The performance parameters such as the size of the chip, speed, power consumption are considered during the design of 3D NoC. In 3D NoC, three number of 2D NoC layers are arranged one above the other using vertical interconnects (TSV) as illustrated in figure 4. In 3D NoC, hundreds or thousands of chips are integrated on a single IC. The authors of [16] stated that the new two layers of the silicon substrate are grown on the top of the parent substrate in a sequence to build 3D NoC. The growth of silicon over the top of the parent silicon substrate is done by the fabrication technologies such as silicon epitaxial growth, recrystallization process, and solid-phase crystallization. There are two integration techniques [17] to build the 3D IC architecture (1) 3D Through Silicon-Vias (TSV) and (2) 3D monolithic integration. The advantages of 3D NoCs are (1) Improved Latency (2) Global interconnects are shorter (3) Power consumption is low (4) High Density. Even though many advantages are there in 3D NoC, there are a few disadvantages that are also available. They are (1) As the density of the 3D IC is more, the power density also increases which leads to thermal heating. Sometimes the thermal power will not dissipate fully from the second layer of the three-layer 3D NoC. This causes a serious problem in the 3D ICs. (2) The size of the 3D IC reduces horizontally but it increases vertically. The TSV [18] used to connect the layers vertically takes more area compared to the conventional connecting wires. TSVs are like a waveguide that requires $5\mu \times 5\mu$ space and it needs more area to fix it on the substrate or layer. (3) Increase in cost: TSV uses copper for its waveguide, so this increases the manufacturing cost of the chip. The Monolithic 3D ICs are having a base silicon substrate and at the top of the base layer, additional metalized layers, and circuitry is formed. The purpose of the Via is to connect the layers of the IC vertically. Network-on-Chip (NoC) circuitry is made above the silicon substrate [19]. This is known as 3D monolithic NoC. Monolithic 3D NoC.

2.6. Three-point five dimensional (3.5 D) NoC

Three-point five (3.5D) NoC is the hybrid technology of 3D NoC. It uses monolithic integration technology and TSV vertical integration technology. Hence this technology is named 3.5D Technology. A case study [20] is done with 288 core Multiprocessor System on Chip and predicted that the cost of manufacturing and testing. It is proved that this 3.5 D technology decreased by 20% of the manufacturing cost and 30% of the test cost compared to other 3D Integration technology. This work is done by connecting all the cores of the SoC. Also, it is proved that the overall performance of the chip is increased by an average of 11.5% and the latency is improved by 25.4% compared to the 3D Integration technology. The researchers can use 3.5D technology according to their applications for N number of cores.

2.7. Photonic network-on-chip

Another method to improve the performance parameters of NoC is Photonic or Optical NoC. The Photonic NoC has a laser source to send light energy through optical waveguides (optical fiber) with different wavelengths.

As the data travels with the speed of light ($3 \times 10^8 \text{ m s}^{-1}$), these photonic NoC chips are emerging nowadays. The optical coupler couples the optical fiber and the optical waveguide. The waveguide can allow a different range of wavelengths, so parallel communication can be done on the same waveguide. Another component named MR (Microring Resonator) is used for the modulation technique and segregate the wavelength of the parallel signals [21]. The MR can also be used to encode the received data. The signal sent by the sender is received at the receiver side by the photo-detectors. The photo-detectors detect and also convert photons into electrons for a wide spectrum of signals. As per the statement of [22], there are two types of buses available for Optical NoC. They are (1) Single-Writer-Multiple-Reader (SWMR) bus (2) Multiple-Writer-Single-Reader (MWSR) bus. In MWSR, each sender sends its modulated signals with separate wavelengths to the single receiver. Hence the receiver receives multiple signals with different wavelengths from many senders [22]. The receiver receives the signal and the data is decoded. The router transfers the data to the Intellectual Property (IP) core via Network Interface (NI) for further process [23].

As different wavelength is used for the signals there is no possibility for any interference or collision of signals. In SWMR, many receivers will receive the same signal sent by a single sender. It is concluded that the Photonic NoC will have low crosstalk, less power consumption, and less chip area.

Authors of [24] have provided an idea to alter the source of Photonic NoC by Silicon avalanche light-emitting devices (SiAvLEDs). They also proved that the light emission point of SiAvLED is about one micron just below the silicon-silicon oxide interface. They have proved that the SiAvLED optical source achieved high performance compared to other Optical sources.

Authors of [25] used Si field-effect LED (SiFELED) as the optical source and obtained its performance in Optical network. They compared SiAvLED with SiFELED and proved that SiFELED is better than SiAvLED in terms of its performance parameters such as speed, throughput etc.

3. Emerging research in NoC

Although many NoC architectures are there for the communication inside the chip, every day new technologies are emerging. As the world is moving towards the miniaturization of electronic devices, the size of the chip also decreases. This in turn affects the NoC architecture and this leads to the innovation of new NoCs.

3.1. Machine learning NoC

The Machine Learning techniques can be adopted for the NoC Technologies such as wired NoC, Wireless NoC, Hybrid NoC, 3D NoC, 3.5D NoC, 2.5D NoC, Photonic NoC. Machine Learning NoC (M/L NoC) depends on the characteristics of the NoCs mentioned above. As monitoring is needed for the NoC operation, most of the M/L NoCs are using supervised learning algorithms such as classification and regression. The routers in the NoCs will be trained by the M/L algorithm to transfer the packets from the source router to the destination routers. These supervised learning-based M/L algorithms are very efficient in terms of speed and power consumption. Some of the popular M/L algorithms used by the researchers [26] are linear regression algorithm, decision tree algorithm, random forest algorithm, K-nearest neighbour algorithm. Hence M/L based NoCs may be the choice of many upcoming researchers.

The data set for the N core NoC is developed by considering every node as the source node and the possible paths for the data packet. The data set is divided into 80% and 20% for training and testing NoC respectively. Any one of the M/L algorithms can be used. Once the required performance is achieved by the NoC model, then it is considered to use in the real-time scenario. The M/L algorithm can also be used to predict the accurate delay before sending the packet from source to destination. Figure 5 illustrates the implementation of a machine learning algorithm in NoC in the process of sending the data from source to destination [27]. The input details such as source address, a destination address, data length are given to the M/L algorithm. With the aid of the data set generated, the M/L algorithm determines the efficient path to reach the destination. If any congestion due to traffic exists, then the M/L algorithm will determine the alternate path to reach the destination.

The parameters are to be considered during the architecture design of M/LNoC are (1) Grid features (2) Topological features, (3) Selection of routing, (4) Traffic Features, (5) Quality of service, (6) Size of the buffer and (7) Deadlock, livelock avoidance. Grid features contain the size of the buffer, number of I/O ports, the total number of agents, total power, total voltage, clock-frequency, and NoC protocols [28]. Traffic Features provides the end-to-end connection between agents, types of interfaces/channels, and bandwidth, latency requirements for each agent, QoS, and real-time requirements. Topological features provide the type and size of the topology of the chip, algorithm for routing, size of agents, area for NoC routing in SoC, and the thickness of the routing wire. The authors applied the M/Lbased NoC technique in various SoCs and compared M/L NoC with other conventional NoCs. It is proved that M/L-based NoC is superior to others in terms of performance.

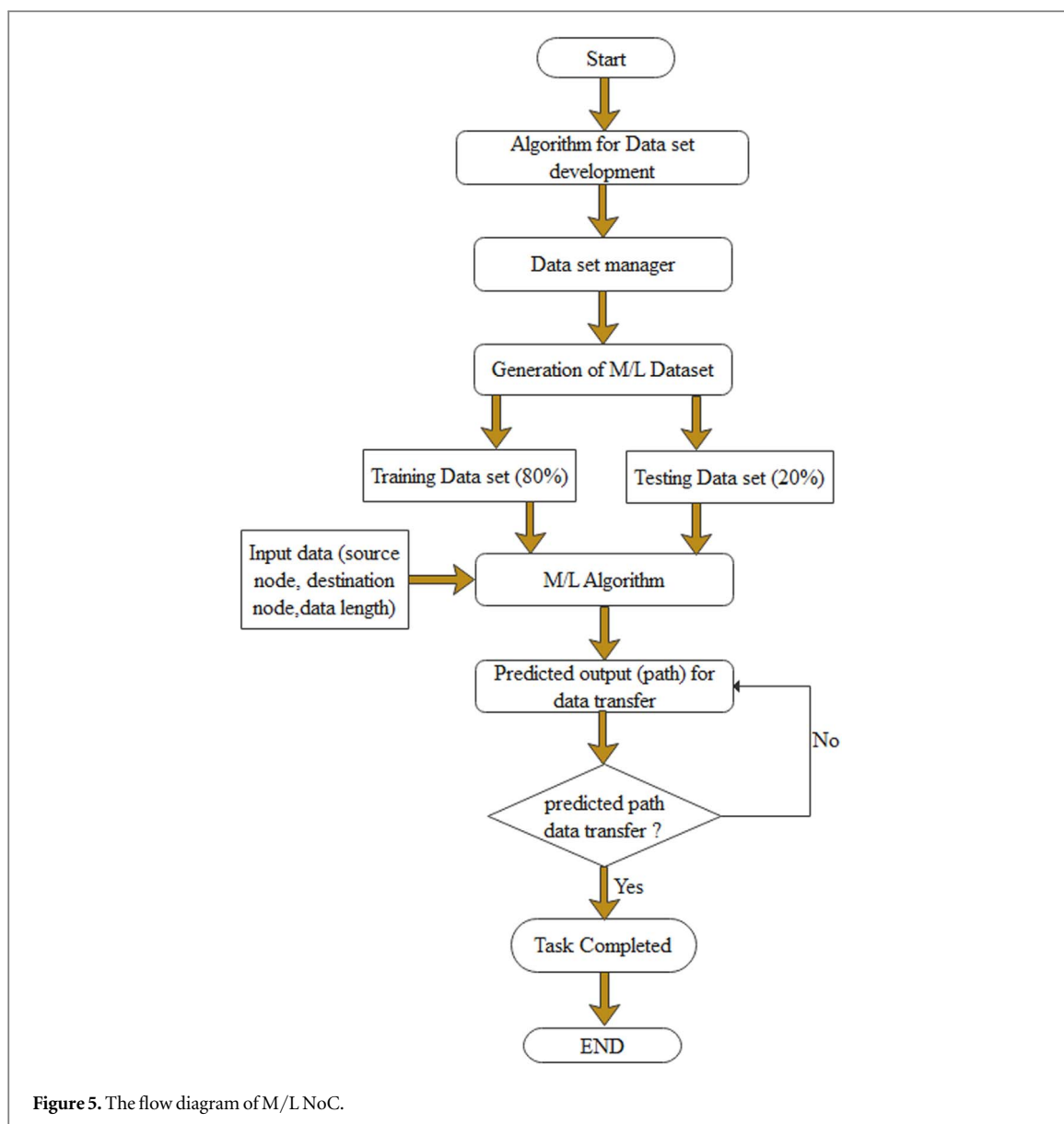
By using thousands of SoC designs, the authors of [29] have generated training data with many characteristics. Next, the predictive models are generated using algorithms such as random forest, neural network, multi-variant linear regression, vector machines, or pattern matching. After the training, the generated model is used to determine the steps to design an optimal interconnect system using linear regression. Similarly, after the completion of training and model generation, the new specification is applied to the preferred Machine Learning predictor. Based on the values provided, the predictor develops different strategies. This M/L technique allows the routers in a core of the chip to decide itself to communicate with the other core if the fault exists. The authors used 30 numbers of real-time SoC for their evaluation of M/L NoC. Also, three predictive models such as balanced, performance, and area are used for the experimental analysis.

The performance model deals with the performance of the chip. In the Area Model, the MLNoC is looking for possible ways to minimize the area of the chip. The authors of proposed the Regression-based M/L model in the training phase and the testing phase. During the testing phase, the machine learning algorithm of NoC predicted the results.

Similarly, the Machine Learning Technique is used to develop the framework of NoC that is helpful to evaluate the performance of NoC and it can be used to improve the performance. The authors of [29] developed an NoC framework and compared it with the cycle-accurate simulator-Books. It is proved that the machine learning based framework is more efficient than Booksim.

3.2. Machine learning based NoC security

Another important feature in M/L NoC is the security issues. Security of NoC is very much important nowadays to protect the IP cores from hackers. Nowadays, Hackers are extracting the data from the IP core itself. Hackers can able to malfunction the IC by using anonymous threats. This kind of anomaly affects the hardware part of the NoC such as routers, network interfaces, IP cores which in turn affects the electronics devices such as mobile phones, laptops, tablets, etc [30]. Nowadays the Internet of Things (IoT) is also emerging drastically. This IoT



device uses ICs which work with the Internet. This paves the way for hackers to send cyber anomalies through the internet. They can alter the data packet in the NoC channel to collapse the system. This NoC security is the emerging research area for the researchers.

The authors of [31] stated that security issues are mainly because of third-party IP companies. As most of the IC design companies are using IP cores from third parties, it leads to the insecurity of NoC. The detection and mitigation of cyber threats can be done by many techniques. The researchers used firewalls to secure the NoC. The authors of [32] created their theft detection mechanism and they avoided the theft done by the hackers. To experiment, they inserted some malicious data to rob the data. The algorithm developed by the authors detected the possibility of theft and it protects the data by encryption. The authors of [33] stated that cyber threats affect the Look-up table of the routers. Because of these security issues in NoC, energy consumption also increases. So, to reduce the energy consumption of NoC the authors used Cyclic Redundancy Check (CRC) and AES encryption system to avoid faults or attacks. Machine Learning-based technique is a very efficient technique to identify and suppress anomalies or threats. The authors explain the Machine Learning techniques used in the security of NoC. They stated that many techniques are there to predict the malfunction. The prediction is based on any of the regression such as Linear regression (LR), Multiple Linear regression (MLR), Decision Tree regression (DTR), Random Forest Regression (RFR), Artificial neural networks, Bayesian learning, computational learning, instance-based learning, genetic algorithms, and reinforcement learning.

4. NoC tools

One more difficulty in carry-out the research in NoC is the NoC Tools. By using the simulation tool, the performance parameters of NoC can be obtained. Table 1 denotes some of the effective NoC simulation tools, the operating system, languages or software used, and the organization that developed those tools. This helps the researchers to select the appropriate tool for their research work.

NS2, NS3 are network simulators [34] useful for any network to determine the performance of the network. NS2 and NS3 can be used for NoC to determine its performance such as speed and power consumption. This simulator is used to design and analyze various components of NoC and its routing. Noxim [35] is the simulator for NoC to determine its parameters. By using this simulator, one can customize the structure of NoC, routing algorithm, data transmission and reception control, Synthetic traffic generation and distribution etc DARSIM [36] is a simulator for designing the architecture of NoC. It uses wormhole router in the NoC structure. To speed up the data transmission and reception, it uses a table-based routing methodology. This simulator also uses Virtual Channel (VC) allocation scheme for routing inside the NoC. Visualsim [37] is a new simulator for NoC research. It is a user-friendly simulator helpful to obtain the delay and power consumption of NoC. ATLAS [38] simulator environment is useful for building the NoC architecture. The NoC can be simulated without traffic and with traffic. The simulator itself creates the traffic for the data flow. By using the ATLAS simulator the performance such as power estimation, delay etc can be determined. ATLAS is a graphical-based simulator that can generate performance tables and output reports. ATLAS uses the VLSI tool Modelsim for simulation. It also uses the GNU plot tool for generating the output graphs. HORNET [39] is a simulator helpful for the multicore NoC simulation. It has the capability of generating the algorithms for the Virtual channel allocation and the routing for the NoC. The performance evaluation of the NoC can be obtained both for traffic scenario and no traffic. X-pipes compiler [40] is a simulator useful for simulating NoC of the heterogeneous System on chip (SoC). This simulator automatically optimizes the building blocks of NoC. It is useful to get optimized results in terms of latency and power consumption. Mspider [41] is a CAD-based simulation tool for NoC. It generates the VHDL code for the NoC design. The generated VHDL code can be synthesizable on FPGA platforms. It uses PHP for generating the output graphs. Mspider is very much useful for getting the performance parameters of NoC such as delay, power consumption and area.

NoCGEN [42] is a simulator used to generate the mesh topology based networks in NoC. Using NoCGEN one can design the components of NoC and its routing. The user can vary the number of cores, routers, data length and buffer size. Wormhole based routing can be used with this simulator. The simulator generates the VHDL code for the NoC. FlexNoC [43] is a commercial simulator designed by With Arteris. FlexNoC is one of the best simulators for NoC interconnection.

FlexNoC concentrates on the congestion during data transfer, delay, area and the power consumption of the NoC. FlexNoC provides the details of data throughput also. The users can achieve high throughput by adjusting the parameters of the NoC. INSEE [44] is a simulation environment that can generate the traffic for the NoC simulation. INSEE is a lightweight tool that can inject data packets in the designed NoC architecture and the performance of the network can be determined. OMNeT++ [45] is a framework for designing the Network simulator. This simulator is useful for the on-chip wired and wireless simulation. It is a GUI based simulator with eclipse based IDE. The components of NoC are designed using C++. PIRATE [46] simulator is used to design the NoC architecture with Intellectual Property (IP) core. This Tool is also used to design the routers and other interconnection components such as channels etc. This tool can be used in any of the network topologies of NoC. By adjusting the load of the network, high-performance NoC in terms of power and delay can be designed. OCCN [47] is the short form of On-Chip Communication Network. It is a framework developed for NoC research. It can develop the communication drivers for the NoC using a universal Application Programming Interface (API). It concentrates on the area of the NoC design and the performance issues of NoC. AcENoCs [48] is the FPGA emulation platform for NoC architectures. It is a flexible tool that provides the Hardware-Software framework for NoC research. The tool has traffic generators, reconfigurable NoC components and analysis modules. This tool has additional features to reconfigure the system. AdapNoC [49] and DucNoC [50] are also the configurable, flexible NoC research tools. Both AdapNoC and DucNoC uses the table based NoC algorithm for increasing the speed of NoC. It has both Traffic Generators and Traffic Receptors. It can generate synthetic traffic and also it can work with real-time traffics.

BookSim is a standard cycle-accurate interconnection network simulator. Booksim is used to customize the router of the NoC. By customizing the NoC router the performance parameters of NoCs can be improved. Booksim can use the topologies such as mesh, torus and flattened butterfly networks. It also provides routing algorithms with numerous options. NETMAKER [51] is also a general-purpose efficient simulator for Network simulation. Netmaker can be used for developing the topologies of NoC and the simulation results can be taken. NIRGAM [52] is a tool for NoC research. This tool works for the 2D mesh and torus network. It uses the wormhole based switching mechanism. The tool can generate the routing algorithms such as deterministic XY,

Table 1. List of various NoC simulation tools.

Name of the simulation tool	Developed by	OS	Language/Software
Network Simulator [34]	Lawrence Berkeley National Lab	Linux, FreeBSD, macOS	C++, Python
Noxim [35]	University of Catania	Linux	SystemC, C++
Darsim [36]	Massachusetts IT	Linux	C++, Python
Visualsim [37]	Mirabilis Design	Windows, Linux	System C
Atlas [38]	GAPH research group	Windows	Java, VHDL
HORNET [39]	Massachusetts IT	Linux	C++, Python
Xpipes compiler [40]	Bologne—Stanford Univ.	Linux	SystemC
μ spider [41]	LAB-STICC	Linux	VHDL
NoCGEN [42]	LaNoC-UFC	Windows, Linux	VHDL/Verilog
FlexNoC [43]	Arteris	Windows/Linux	SystemC
Insee [44]	Manchester University	Linux	ANSI C
OMNeT++ [45]	OpenSim Ltd	Windows/Linux	C++
Pirate [46]	Politecnico di Milano	Linux	SystemC
OCCN [47]	STM, AST Grenoble Lab	Unix/Linux	SystemC, C++
AcENoC [48]	Texas A&M University	Windows/Linux	Xilinx Microblaze
AdapNoC [49]	Sharif University of Tech.	Windows/Linux	Xilinx Microblaze
DuCNoC [50]	Sharif University of Tech.	Windows/Linux	C++, Verilog HDL
BookSim [24]	Stanford University	Windows/Linux	C++
Netmaker [51]	University of Cambridge	Linux	SystemVerilog
NIRGAM [52]	Soton university	Linux	System C
ARTEMIS (3D) [53]	Colorado State University	Linux/Windows	MATLAB
Gem5 [54]	University of Michigan	Linux	System C

Adaptive odd–even(OE), Source Routing. ARTEMIS [53] is the tool for analyzing the NoC system. This tool is useful for determining the efficiency of the NoC components such as routers and cores. This tool can also be used for analyzing 2D and 3D NoC systems. The gem5 [54] is an open-source simulator used for the NoC research, system-level research and processor research. The tool has caches, crossbar switches, filters, DRAM controllers etc to make the NoC unique and fast. Using this tool, homogeneous and heterogeneous multi-core architectures can be designed.

Most of the NoC tools are working in Linux operating system. Few Tools are working in both Linux, windows and MAC operating system. Researchers with C++ knowledge can use many NoC tools in the list provided. Less number of Tools are working with RTL languages such as VHDL, Verilog. AcENoC [48] and AdapNoC [49] uses Xilinx-Microblaze. As Microblaze is a very user friendly software most of the researchers may use it.

5. Conclusion and future scope

This paper summarizes the research work carried out by the researchers of Network-on-Chip (NoC). This paper explains the various NoC technologies such as wired NoC, wireless/RF NoC, hybrid NoC, photonic NoC, 2.5D NoC, 3D NoC, 3.5 D NoC which are helpful for the emerging Machine Learning based research work. The security issues of NoC is also addressed. This paper also highlights the current research in Machine Learning-based NoC security. This paper provides various tools available to carry out the research in the NoC area which are popular and efficient nowadays.

Data availability statement

No new data were created or analysed in this study.

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