Postgraduate (Government of Ireland)

Overview

Application details

Application type	Postgraduate (Government of Ireland)
Create date	13/09/2024 02:40:00
Application deadline	**2024-10-10 16:00:00 Ireland time**
Please select the appropriate scholarship theme for which you are applying	Government of Ireland Postgraduate Scholarship
Project ID	GOIPG/2025/6674
Irish Research Body	Trinity College Dublin
Project title	Optimising Network-on-Chip Architecture for Deep Learning Accelerators at Scale
Department	Electronic & Electrical Engineering
Application in Irish	No

Applicant details

Name	Lingyu Gong
Email address	gongl@tcd.ie
Please select the gender you identify with	Woman
Date of birth	16/05/2001

ORCID identifier:

> Please ensure that you only enter numbers for your ORCID. eg 1234567891011121

0009-0003-2758-8342

What is your nationality, i.e. your passport-issuing country?
China

Are you a national of a European Union member state (including the Republic of Ireland) **OR** Iceland, Norway, Liechtenstein, Switzerland, the United Kingdom or Ukraine?
No

Will you have been ordinarily resident* in a European Union member state (including the Republic of Ireland) OR Iceland, Norway, Liechtenstein, Switzerland, the United Kingdom or Ukraine for a continuous period of three of the five years preceding 1 October 2025?
No

Primary and additional participants

Primary supervisor details

Name	Shreejith Shanker	**Higher education institution**	Trinity College Dublin

Secondary supervisor details (if applicable)

Name		**Higher education institution**	

Track record

> The IRC reserves the right to request the original and/or certified copy of your undergraduate and postgraduate degree certificate(s) or transcript(s) at conditional offer stage and at any stage of the award. Failure to submit the required documents may result in the withdrawal of the conditional offer, suspension, or termination of the award. The IRC's decision on this matter is final.

Bachelor's degree (or equivalent)

> If your degree results refer to a grading system other than the 0-4 Grade Point Average scale or the Irish honours grading system (e.g. First Class Honours (1.1), Upper Second Class Honours (2.1)…), please explain the grading system being referred to in the free text box provided. Equivalency of degree can be found in the Irish National Framework of Qualifications.

Institution	Other
Institution name	Capital Normal University
Country	China
Graduation date	01/07/2023
Qualification type and name	Bachelor's degree in Engineering
Is this degree complete?	Yes

Final grade or grade point average	3.51
Any additional information relating to this degree or your final grade can be included here	3.51 out of 5.0, The thesis was awarded the title of outstanding thesis at the university level, and was awarded the title of outstanding graduate.

Second bachelor's degree (if applicable)

> If your degree results refer to a grading system other than the 0-4 Grade Point Average scale or the Irish honours grading system (e.g. First Class Honours (1.1), Upper Second Class Honours (2.1)…), please explain the grading system being referred to in the free text box provided. Equivalency of degree can be found in the Irish National Framework of Qualifications.

Institution	
Graduation date	
Qualification type and name	
Is this degree complete?	
Any additional information relating to this degree or your final grade can be included here	

Master's degree (if applicable)

> If your degree results refer to a grading system other than the 0-4 Grade Point Average scale or the Irish honours grading system (e.g. First Class Honours (1.1), Upper Second Class Honours (2.1)…), please explain the grading system being referred to in the free text box provided. Equivalency of degree can be found in the Irish National Framework of Qualifications.

Type	Taught
Institution	Trinity College Dublin
Graduation date	01/10/2024
Qualification type and name	Masters in Electronic Information Engineering
Is this degree complete	Yes
Final grade or grade	66

point average	
Any additional information relating to this degree or your final grade can be included here	66 out of 100, Upper Second Class Honours (2.1).

Second master's degree (if applicable)

> If your degree results refer to a grading system other than the 0-4 Grade Point Average scale or the Irish honours grading system (e.g. First Class Honours (1.1), Upper Second Class Honours (2.1)…), please explain the grading system being referred to in the free text box provided. Equivalency of degree can be found in the Irish National Framework of Qualifications.

Type	
Institution	
Graduation date	
Qualification type and name	
Is this degree complete?	
Any additional information relating to this degree or your final grade can be included here	

Other education

Please provide any additional information relevant to your academic background which should include the name, location and date(s) of any training courses attended:

> If your degree results refer to a grading system other than the 0-4 Grade Point Average scale or the Irish honours grading system (e.g. First Class Honours (1.1), Upper Second Class Honours (2.1)…), please explain the grading system being referred to in the free text box provided. Equivalency of degree can be found in the Irish National Framework of Qualifications.

Massachusetts Institute of Technology (MIT), Boston, United States – Engineering, Design, Gaming, and Entrepreneurship (EDGE) Program for STEM (08.2022 – 05.2023):
In this program, I learned the entire process of game development, from defining user needs to creating system models. I developed technical proficiency with tools like Tale Blazer and APP Inventor and worked collaboratively with a team to design a physics history popular science game. This experience not only strengthened my technical and creative skills but also taught me the importance of interdisciplinary collaboration and problem-solving in STEM fields.

Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China – Visiting Student (08.2022 – 05.2023):
During this time, I was responsible for researching and implementing Network-on-Chip (NoC) modules, enhancing my expertise in high-performance computing systems. I also contributed to organizing project materials, attending regular group

meetings, and solving complex challenges collaboratively. This experience allowed me to develop advanced programming skills, strengthen my information system development capabilities, and refine my collaboration and problem-solving skills in a research-driven environment.

Research achievements

Please provide any additional information regarding your research achievements to date such as publications, research awards, creation of data sets and databases, conference papers, patents, excavations, public broadcasts, stage performances, creative writing, creative productions and/or exhibitions:

1. Design & Research of a 3D Modeling Course – Led a project that integrated AI with Rhino software to improve 3D modeling efficiency and creativity. Awarded first prize in a laboratory fund project.

2. Exploring Solutions for Data Restoration Using Protection Cards – Participated in a project on computer configuration and data protection, earning third prize in a laboratory fund project.

3. Research on Open Source NoC Based on Intelligent Routing Algorithm – Graduation project on NoC routing algorithms, awarded Excellent Thesis.

Work experience

Please provide details of any relevant work experience, including voluntary work, to date which should include employers' names, job titles, nature of duties and responsibilities, as well as duration of employment:

1. Visiting Student, Institute of Computing Technology, Chinese Academy of Sciences (08.2022-05.2023)
Researched and implemented NoC modules, organized project materials, attended group meetings, and contributed to discussions regularly.

2. Trainee IT Teacher, Capital Normal University High School (09.2022-11.2022)
Taught C++ lessons, designed IT course materials, and provided personalized learning plans to engage and guide students.

3. Part-time Bartender, The Auld Dubliner, Dublin, Ireland (01.2023-04.2024)
Improved English communication skills, developed social interaction abilities, and gained experience handling stress in a fast-paced environment.

Personal statement

Statement

> Please highlight any additional information which has not been included elsewhere in the application, e.g.:
> • Why do you wish to pursue a higher degree by research?
> • Why have you proposed this research topic?
> • Why do you feel there is a specific demand for the skill set that you wish to build?
> • Why are you particularly suited to this research field?
> • Which of your attributes demonstrate your capability to be a good researcher, e.g. motivation, commitment, thirst for knowledge?

My passion for scientific research, particularly in the chip field, has grown with each experience, whether it's soldering circuit boards, diving into lines of code, or tackling challenging debugging sessions. Every interaction with hardware feels like a conversation with future technology, sparking my excitement for innovation. My research journey has not only matured my skills but also solidified my determination to pursue this path. Overcoming setbacks has strengthened my resilience, and now I'm eager to contribute to the chip industry, driven by a thirst for knowledge and respect for technological progress. My dream is to break existing boundaries and develop more efficient, intelligent, and reliable chip solutions.

During my undergraduate studies in computer science, my interests ranged from software system design to hardware. However, my academic turning point came with my first hardware course, Digital Logic Circuits. It was here that hardware design truly captivated me. The gates and triggers of digital circuits became more than just components; they embodied endless creativity and wisdom. The joy I felt from designing, debugging, and seeing complex functions come to life fuelled my passion for further exploration.

While Moore's Law has long guided hardware advancements, its limitations are now evident. As we face unprecedented challenges, the demand for high-end talent in hardware is more urgent than ever. This technological revolution requires people with the courage to explore new paths beyond traditional frameworks, and I am determined to be at the forefront of this wave. My research direction is closely tied to AI, which today demands unprecedented hardware acceleration to unlock its full potential. I am convinced that my work holds not only theoretical value but also the potential to impact the world.

I view a PhD as a golden opportunity to immerse myself deeply in this field. With more time and resources, I can explore, experiment, and innovate without distractions. While four years may seem long, I see it as a critical period for refining my scientific research abilities, sharpening my innovative thinking, and developing the perseverance needed to achieve great success. This journey will be challenging but invaluable for my future.

I possess a deep love for scientific research, driven by an insatiable desire to explore and learn. My project experiences have sharpened my skills and allowed me to challenge my limits. Each successful project has been a source of immense encouragement. Whenever I’m in the lab, surrounded by complex circuit diagrams and boards, I feel an indescribable excitement. My pursuit of knowledge and my determination to solve problems at their root are what motivate me.

In addition to my technical skills, I have developed strong communication and organizational abilities through leadership roles in project teams and student unions. These experiences have taught me how to manage teams, coordinate resources, and foster collaboration—essential skills for my PhD journey.

Training and career development plan

Career Training and Development Plan:

> Please highlight any additional information which has not been included elsewhere in the application, e.g.:
>
> What are your career goals and how would this scholarship help you to achieve them?
> How will you go about acquiring the expert knowledge and transferable skills necessary for your professional development, e.g. technical skills, communication skills, analytical skills?
> How would this scholarship enable you to gain skills relevant to employment outside the traditional academic sector?
> How can the scholarship transform your existing skills in those identified as being required to pursue the chosen career?

My ultimate goal is to delve deeply into advanced hardware design and artificial intelligence (AI), gaining a comprehensive understanding and mastery of these areas. I aspire to take the knowledge and skills acquired during my Ph.D. studies and apply them in the industrial sector, identifying gaps, innovating solutions, and contributing to technological advancements that push the boundaries of modern technology. This scholarship will provide me with the financial support and resources necessary to access advanced technologies, collaborate with like-minded professionals, and develop into a well-rounded expert ready to contribute to society.

To acquire expert knowledge and develop the necessary skills for my professional growth, I intend to adopt a multifaceted approach. I plan to immerse myself in the latest research by conducting extensive literature reviews, keeping myself updated with cutting-edge concepts, methodologies, data analysis techniques, and evaluation metrics. I will continuously enhance my data summarization and presentation skills through practical applications in both academic and industrial settings.

A prime example of my ability to acquire expert knowledge is my personal journey with programming languages. I initially

developed a strong foundation by systematically learning C, which paved the way for mastering other languages like C++, Python, Matlab, and Java. I adapted each language based on the specific needs of the project I was working on, enhancing my knowledge transfer and problem-solving abilities. I aim to apply a similar approach to hardware design and AI, where mastery requires a continuous cycle of learning, applying, and integrating new technologies.

The technical skills I acquire will be supported by rigorous academic training and hands-on experiments. I will stay abreast of evolving technologies through cutting-edge literature and active participation in academic conferences. Conferences and research collaborations will provide me with valuable insights into the latest research trends and methodologies. Being part of advanced research teams will further sharpen my leadership, teamwork, and communication skills, which are critical for managing complex projects and leading innovation in an industrial context.

This scholarship will transform my career trajectory by providing access to cutting-edge projects and a platform for interdisciplinary collaboration. Working closely with experts from various academic and industrial backgrounds will hone my collaboration and problem-solving skills. Moreover, the rigorous nature of the research projects will require me to strengthen my project management abilities, analytical insights, and programming skills. These competencies are not only foundational for academic research but are widely applicable across multiple industries, including technology, finance, and management.

In addition to technical expertise, the scholarship will enable me to foster essential soft skills. Recognizing the importance of communication, I aim to expand my network and improve my leadership and coordination skills. I will actively participate in group projects and interdisciplinary collaborations, refining my ability to work inclusively and guide teams toward successful outcomes. Furthermore, I value a well-rounded life, and this scholarship will allow me to take part in social activities, develop meaningful friendships, and explore new cultures, all of which will enhance my empathy and communication skills—qualities that are invaluable in both professional and personal settings.

The skills I gain during my Ph.D. studies will be directly transferable to employment outside the traditional academic sector. With the help of this scholarship, I will develop expertise in advanced hardware design and AI, areas critical to industries such as semiconductor manufacturing, AI hardware development, and technology consulting. Mastering a series of core technologies and professional knowledge directly related to these high-tech industries will position me to excel in various professional environments. Furthermore, interdisciplinary collaboration will provide me with a holistic understanding of different research approaches and problem-solving techniques, enhancing my adaptability and making me a more versatile professional.

The scholarship will act as a catalyst, transforming my existing skills into those required to pursue my chosen career. Currently, I possess a solid foundation in hardware design, programming, and research methodologies—key competencies for success in fields like chip technology and AI acceleration. However, this scholarship will provide me with the resources to deepen my expertise by allowing me to work on advanced research projects that integrate AI with hardware design. These opportunities will enable me to develop a nuanced understanding of complex system design, optimization, and real-world application.

In summary, this scholarship is much more than financial support; it represents a unique opportunity for me to fully dedicate myself to my research and professional development. By providing access to cutting-edge technologies, expert collaboration, and opportunities for interdisciplinary exchange, the scholarship will allow me to acquire the knowledge and skills needed to become an expert in advanced hardware design and AI. This comprehensive development plan will enable me to excel both in academia and in industrial sectors, where I will contribute to innovative solutions that address current and future technological challenges. Ultimately, I aspire to give back to society by contributing to humanity’s progress, with a deep sense of gratitude for the support I have received throughout my academic journey.

Proposed research

Overview

If successful, will you be a new entrant to the degree for which you are seeking Irish Research Council funding on 1 September 2025?
Yes

Please specify the scholarship type for which you are applying
48-month structured doctoral degree

Will you be in receipt of any additional awards or research / academic salary during the scholarship period, e.g. scholarships, positions, bursaries, travel grants etc.?

> Failure to provide this information may render your application ineligible.

No

Have you previously submitted all or part of this proposal to an Irish Research Council scheme and been unsuccessful?
No

Do you currently hold, or have you previously held, any other Irish Research Council awards?
No

Project title	Optimising Network-on-Chip Architecture for Deep Learning Accelerators at Scale
Primary area	Engineering
Discipline	Electrical Engineering, Electronic Engineering, Information Engineering
Other research area(s)	
Second categorisation – if interdisciplinary	
Keywords describing proposed research	Network-on-Chip (NoC), Deep Learning Accelerators, AMD VERSAL Architecture, Energy Efficiency, NoC Configuration Optimization.

Please provide a lay abstract for your proposed research. This will be used to inform a non-specialist audience.
The rapid growth of multimedia streaming and artificial intelligence (AI) has placed significant demands on modern computer systems. At the heart of these systems is the Network-on-Chip (NoC) architecture, which connects different processing units within a Multi-Processor System-on-Chip (MPSoC). This research focuses on optimizing the NoC in AI accelerators, particularly in AMD's VERSAL platform, to improve the performance of MPSoC systems, which are widely used in devices handling streaming media.

Streaming media requires high bandwidth and low latency to deliver smooth and high-quality content. However, the current NoC designs can cause bottlenecks, slowing down data transfer between different parts of the system. This project aims to identify these bottlenecks and develop tools to optimize the NoC architecture, improving the speed and efficiency of data processing.

The research will also explore how to reduce energy consumption in MPSoC systems without sacrificing performance, striking a balance between power usage and processing speed. By examining different ways to transfer and manage data, the project seeks to enhance both energy efficiency and streaming quality.

Ultimately, this research will offer practical solutions for improving streaming performance and energy efficiency in MPSoC systems, which are crucial for the future of AI-powered multimedia devices. The findings will benefit not only academic research but also have real-world applications in industries that rely on high-performance computing, such as video streaming, gaming, and AI hardware development.

Detailed proposal

Please provide details of your proposed research to include (a) aims, objectives and central research questions of the project, (b) how existing literature on the topic has been used to inform the proposal and (c) how the project will advance state of the art and make a contribution to existing knowledge:

(a) Aims, Objectives, and Central Research Questions:

The primary objective of this research is to optimize the Network-on-Chip (NoC) architecture in AI accelerators, particularly focusing on AMD's VERSAL platform, to elevate the performance of Multi-Processor System-on-Chip (MPSoC), and ultimately to augment the quality of streaming media. In light of the considerable bandwidth and low latency demands of multimedia streaming, it is imperative to optimize NoC within MPSoC systems.

The objective is to develop tools and methodologies to:

1.Benchmark the NoC interconnect to identify performance bottlenecks that may arise in media streaming within MPSoC systems.

2.Determine optimal NoC configuration parameters to minimize latency and maximize throughput for multimedia data processing across multiple cores.

3.Perform an energy-performance trade-off analysis for streaming applications to optimize speed and power consumption in MPSoC environments.

4.Investigate potential optimizations in data transfer formats and precision across processing units while maintaining requisite streaming quality and AI model accuracy.

The central research questions are as follows:

1.What modifications to the NoC configuration in VERSAL AI accelerators can reduce latency and improve throughput in media streaming tasks within MPSoC systems?

2.What are the performance-energy trade-offs associated with different NoC configurations for MPSoC, particularly in the context of streaming applications?

3.How can data representation formats be optimized to improve energy efficiency without compromising the quality of streaming or AI model accuracy?

(b) Existing Literature and Its Influence on the Proposal:

The extant literature shows that NoC optimization is critical for improving media streaming performance in AI accelerators, particularly within MPSoC environments. Studies on VERSAL AI engines and packet switching have highlighted the challenges of managing data transfers in high-bandwidth, low-latency environments, such as those encountered in streaming. However, the existing body of research often lacks user-driven tools capable of optimizing NoC for multi-core streaming workloads in MPSoC. Furthermore, research on energy efficiency in large-scale AI models, especially those used for high-resolution media processing, further underscores the necessity of hardware-level optimizations in MPSoC systems. This proposal builds on the aforementioned findings to develop practical tools that address the complexities of NoC configuration complexities, focusing on real-time streaming applications within MPSoC platforms.

(c) Advancing the State of the Art and Contribution to Knowledge:

This project represents a significant advancement in the state of the art, offering a novel framework for optimizing NoC in AI accelerators with the specific aim of improving MPSoC performance for streaming media applications. In contrast to existing tools that concentrate on task mapping, this research will focus on fine-tuning NoC configurations for enhanced performance, energy efficiency, and scalability in streaming applications. By examining NoC configurations, energy-performance trade-offs, and data transfer optimizations, the project introduces novel methodologies for the management of intricate workloads in MPSoC systems. The collaboration with AMD's Versal research team will provide empirical validation, ensuring that the research outcomes are both practical and impactful. Ultimately, this research delivers scalable solutions for enhancing hardware performance in MPSoC systems, addressing the high demands of streaming media in terms of bandwidth, latency, and energy efficiency.

Please detail the research design and methodologies to be employed in carrying out your scholarship which should be described in sufficient detail to demonstrate your thorough understanding of the research topic:

This research employs a multi-phase approach to optimize the NoC architecture in AMD's VERSAL AI accelerators for MPSoC systems, with a particular emphasis on streaming applications. The design is centered around sustainability by benchmarking state-of-the-art implementations and maximizing the reuse of components.

Benchmarking the State-of-the-Art (SOTA) and Analysis:
In this phase, existing NoC implementations on AMD's VERSAL platform will be benchmarked using custom profiling scripts. The evaluation of key metrics, such as latency, congestion points, and bandwidth limitations will be conducted under AI streaming workloads in an MPSoC environment. By benchmarking against current SOTA designs, the performance bottlenecks and gaps will be identified, providing critical insights into how NoC configurations affect streaming applications within MPSoC systems. The results of this analysis will inform the implementation of targeted optimizations.

Optimization of NoC Configuration Parameters:
By employing tools such as BookSim2 and AMD's NoC modeling software, the NoC configuration parameters such as routing algorithms, buffer sizes, and link widths will be optimized. This phase aims to reduce latency and maximize throughput for MPSoC-based streaming applications. We will leverage genetic algorithms and other automated search methods to efficiently explore the design space. The optimization process will prioritize sustainability by reusing existing components and ensuring that any enhancements to the NoC are seamlessly integrated with minimal changes to the current system.

Energy-Aware Task Scheduling:
Building on energy-efficient scheduling methods, the Dynamic Voltage and Frequency Scaling (DVFS) will be implemented to optimize energy consumption. Task scheduling will balance workloads across multiple MPSoC cores, ensuring resource efficiency while adhering to system memory constraints. These optimizations will reduce power consumption and latency, tailored specifically for streaming applications where sustained data transfer and low latency are crucial.

Domain-Specific Energy-Performance Trade-off Analysis:
An in-depth energy-performance analysis will be performed using AMD's VERSAL toolkit, focusing on the balance between performance and energy consumption in streaming applications. This phase will evaluate how NoC configurations and DVFS contribute to real-time energy efficiency. The goal is to optimize energy use while maintaining high throughput, ensuring relevance for MPSoC-based streaming applications.

Low-level Data Transfer Optimization:
This phase will explore custom data encoding, compression techniques, and precision management, specifically designed to reduce data size and bandwidth usage across the NoC. These optimizations will ensure efficient bandwidth use without compromising AI model accuracy or performance in real-time streaming tasks.

Validation in the Application Domain:
The final phase will validate the proposed NoC optimizations in real-world MPSoC streaming applications, using AMD's VERSAL hardware. We will test the system against existing interfaces to demonstrate seamless integration with minimal modifications, reinforcing sustainability objectives. Key performance metrics such as frames per second, energy per inference, and bandwidth efficiency will be measured. The goal is to validate that the NoC optimizations provide significant performance gains while maximizing component reuse and energy efficiency in streaming environments.

Please provide a schedule to include (a) milestones and deliverables for completion of the proposed research, (b) risks that might endanger reaching these deliverables and (c) the contingency plans to be put in place in order to mitigate these risks:
Year 1: Foundation and Setup
The initial phase will concentrate on establishing a robust foundation, entailing a comprehensive examination of the extant literature on NoC architecture within MPSoC systems, AMD VERSAL platforms, and the requirements for streaming applications. This will culminate in the production of a report delineating the research gaps, particularly in the context of streaming and sustainability. By the second quarter, the research environment will be established, including the provision of AMD VERSAL development kits and the implementation of simulation tools such as BookSim2. In the third quarter, the VERSAL NoC will be benchmarked under AI streaming workloads, resulting in the production of a baseline performance report. In the final quarter, preliminary models for optimizing the NoC for MPSoC streaming applications will be developed.

Risks: Delays in hardware access.
Mitigation: Use alternative simulation tools and maintain collaboration with AMD.

Year 2: Exploration and Optimization
In the second yeae of the programme, the emphasis will be on examing NoC configurations and developing optimization algorithms. In the first half, simulation tools will be employed to investigate routing algorithms, buffer sizes, and other NoC parameters, leading to a detailed analysis. The third quarter will be dedicated to the development of optimization algorithms to enhance NoC performance and energy efficiency for MPSoC streaming applications. In the fourth quarter, an energy-performance trade-off analysis will begin, resulting in an interim report.

Risks: Algorithm failure or insufficient computational resources.
Mitigation: Iteratively refine algorithms and seek additional computational resources through cloud services or institutional support.

Year 3: Data Transfer Optimization and Validation
In Year 3, the focus will be on the optimization of low-level data transfer and the validation of these processes. The first two quarters will involve optimizing data encoding and compression techniques to reduce bandwidth usage for real-time NoC transfers in MPSoC systems. The third quarter will integrate optimized NoC configurations into a unified framework, and the fourth quarter will then validate these configurations on AMD's VERSAL hardware, with performance metrics such as frames per second, energy consumption, and bandwidth efficiency being measured.

Risks: Hardware limitations or insufficient performance improvements.
Mitigation: Collaborate with AMD for troubleshooting and iterative tuning to address performance issues.

Year 4: Final Evaluation and Dissemination
The fourth year of the programme will ne dedicated to the final evaluation and dissemination of the findings. The first two quarters will compare the optimized NoC performance to the baseline established in Year 1, focusing on streaming performance and sustainability. The findings will be documented in a performance evaluation report. The third quarter will focus on documenting energy efficiency improvements, and the final quarter will be devoted to the preparation of the research for publication in academic journals and submission to conferences.

Risks: Delays in finalizing research or meeting publication standards.
Mitigation: Allocate buffer time to address unforeseen challenges and seek early feedback for refinement.

Please describe any specialist knowledge or data required to undertake your proposed research, such as language competency, technical skills or use of specialist software. If this knowledge or data is not already in place, details should be provided as to how it will be acquired over the course of the scholarship:
This research necessitates a combination of specialized knowledge, technical expertise, and sophisticated software tools to optimize the NoC architecture in AMD VERSAL AI accelerators, particularly within MPSoC systems for streaming media applications.

Technical Skills and Knowledge:
1. Network-on-Chip (NoC) Architecture:
A comprehensive grasp of NoC design, encompassing routing algorithms, buffer management, and data flow optimization within MPSoC systems, is essential. I have a robust foundation in these domains and will further augment my expertise through experimentation and a review of the literature on NoC optimization for real-time streaming tasks.

2. Deep Learning Accelerators and Hardware Design:
Expertise in deep learning accelerators, particularly the AMD VERSAL architecture, is crucial for optimizing NoC within MPSoC systems. My background in hardware design provides a solid base, which I will further develop this through direct engagement with VERSAL development kits, focusing on streaming application optimization.

3. Data Transfer and Encoding Techniques:

Understanding data encoding and compression techniques is key to optimizing NoC data movement, especially for real-time streaming tasks in MPSoC environments. While I am familiar with basic methods, I will further deepen this knowledge through targeted experimentation and literature review on bandwidth-efficient streaming solutions.

Specialist Software and Tools:
1. Simulation Tools (e.g., BookSim, AMD NoC Modeling Software):
A proficiency in the utilization of NoC simulation tools, such as BookSim and AMD's NoC modeling software is essential for exploring and optimizing NoC configurations. I will gain expertise through tutorials and hands-on experimentation with these tools.

2. Programming Languages (Python, C++):
Strong programming skills in Python and C++ are required for algorithm development and simulation. My proficiency in these languages allows me to efficiently implement and test NoC configurations tailored for MPSoC systems and streaming applications.

3. Power Modeling and Profiling Tools:
Familiarity with AMD's power modeling tools is crucial for conducting energy-performance trade-off analysis. I will develop proficiency by working within AMD's development environment, focusing on energy-efficient solutions for MPSoC-based streaming applications.

Data and Access Requirements:
1. Access to AMD VERSAL Development Kits:
Access to AMD VERSAL development kits and the HPC platform HACC is crucial for validating NoC optimizations in real-world settings. These resources are secured through a collaborative effort between AMD and ETH Zurich.

2. Literature and Documentation:
Maintain ongoing access to the latest research papers and technical documentation is essential to stay current with industry advancements, guiding the direction of the NoC optimization efforts.

By building on my current skillset and acquiring additional expertise through targeted learning, experimentation, and collaboration, I am well-positioned to undertake this research. This combination of specialized knowledge and access to necessary resources ensures the successful optimization of NoC for MPSoC systems, particularly for streaming media applications and sustainable design.

Please outline your plans for the dissemination and knowledge exchange of your research, including publications, conference attendance, poster presentations, reports and outreach activities. Details should also be provided as to how the impact of your research will be measured:
Publications:
The primary method of disseminating research findings will be through high-impact, peer-reviewed journals like IEEE Transactions on Computers, ACM Transactions on Design Automation of Electronic Systems, and the Journal of Parallel and Distributed Computing. These journals cover key domains like computer architecture, AI hardware, and energy-efficient design, making them ideal for sharing insights on NoC optimization for streaming media and sustainable design. Research will be published in phases, from initial NoC benchmarking to configuration optimization, energy-performance trade-offs, and the development of a sustainable NoC framework. Each paper will offer detailed methodologies and results, providing valuable insights to academic and industrial communities.

Conference Attendance and Reporting:
Presenting at international conferences is crucial to the dissemination strategy. I plan to submit papers and present findings at conferences such as the IEEE/ACM International Networks-on-Chip Symposium (NoCS), the International Conference on Field-Programmable Logic and Applications (FPL), and the Design Automation Conference (DAC). These platforms are ideal for sharing research on NoC for AI streaming applications and fostering collaboration. Conference feedback will aid in refining the research and open doors to new collaborations with peers.

Poster Presentations and Workshops:

In addition to oral presentations, poster sessions at events like the IEEE Symposium on High-Performance Computing Architecture (HPCA) will enable direct interaction with researchers and the exchange of ideas. These platforms are crucial for disseminating sustainable NoC designs for real-time multimedia applications. Participation in AI accelerator and hardware optimization workshops will further encourage detailed discussions and explore potential real-world applications.

Reporting and Industry Collaboration:
Regular progress reports will be shared with partners, particularly the AMD Versal research team, including methodology, findings, and insights from NoC optimization deployment. These reports will encourage ongoing collaboration, influencing future product designs. Internal seminars and webinars with industry partners will also be conducted to ensure the practical application of research outcomes in industrial settings.

Outreach Activities:
Outreach efforts will include writing articles for technology blogs and contributing to open-access platforms to simplify research findings for a broader audience, including those interested in NoC optimization for streaming media. Workshops and lectures at academic institutions will also promote sustainable NoC designs in courses, inspiring future research directions.

Impact Assessment:
The impact of the research will be measured through publications, citation counts, conference feedback, and industry collaboration, particularly with AMD. Adoption of NoC optimization techniques in academic and industrial settings will further gauge research success. Outreach activities will be assessed using blog post views, open-access downloads, and audience engagement, ensuring a broader societal impact.

Please outline **your** reasons for choosing your proposed (a) academic supervisor(s) and (b) higher education institution making particular reference to how the chosen supervisor and institution

> Please outline your reasons for choosing your proposed (a) academic supervisor(s) and (b) higher education institution making particular reference to how the chosen supervisor and institution:
>
> • can support the acquiring of methods and knowledge necessary to completing the proposed project
> • can provide any facilities and infrastructures or other supports relevant to completing the proposed project
> • can provide an appropriate and comprehensive training programme; consider highlighting the HEI's training programme, which is expected to be comprehensive
>
> Avoid using only an institutional template and include a personal justification explaining why the facilities are appropriate for the researcher, the proposed project and the knowledge, support and expertise required to complete the project.

I have selected Professor Shreejith Shanker as my academic supervisor due to his expertise in computer architecture, AI hardware acceleration, and NoC design. His involvement in projects focused on energy-efficient compute flows in the media industry is closely aligned with my own research on optimizing NoC for streaming applications. Additionally, Professor Shanker’s involvement in a Horizon Europe (HEU) project investigating energy consumption in the movie industry’s compute flows complements my focus on energy-performance trade-offs in real-time streaming tasks. His extensive experience with the AMD VERSAL architecture provides invaluable insights into optimizing NoC for real-time, energy-intensive applications. Furthermore, his established collaborations with industry partners such as AMD ensure that my research will have practical relevance and access to cutting-edge resources. Under his supervision, I will receive guidance that integrates both academic rigor and industrial applications, which is essential for the success of my research.

Trinity College Dublin (TCD) offers an ideal platform for my research, distinguished by its reputation for excellence in engineering, AI, and computer architecture. The School of Computer Science and Statistics provides access to cutting-edge facilities, including AMD VERSAL platforms, which are essential for my NoC optimization efforts. TCD’s involvement in Horizon Europe projects related to sustainable computing in media applications aligns perfectly with my focus on energy-efficient NoC designs for streaming tasks. Moreover, TCD’s strong partnerships with industry leaders such as AMD will

facilitate valuable collaboration, allowing my research to tackle both theoretical and practical challenges. TCD's dynamic research community encourages innovation and societal impact, ensuring that my work contributes to the expanding field of AI hardware optimization.

By selecting Professor Shreejith Shanker and Trinity College Dublin, I will benefit from exceptional mentorship, cutting-edge resources, and industry connections, all of which are crucial for advancing my research on NoC optimization for AI accelerators, particularly in the areas of streaming media and sustainable design. This combination of expertise and support will ensure that my research makes a significant contribution to both academic knowledge and industrial practice.

Please provide details of any proposed research trip(s) of more than four weeks duration which you believe will be necessary for the successful completion of your award:
Proposed Local Research Trip

Location: AMD Research Lab, Dublin

Duration: 6 weeks

Objective: This research trip aims to collaborate directly with AMD's research team and gain hands-on access to the VERSAL hardware platform. Access to this hardware is critical for testing and validating the NoC optimization techniques developed in my research.

Reason for the Trip: While based at Trinity College Dublin, having extended access to AMD's facilities will allow for hands-on experimentation with the VERSAL devices and enable real-time collaboration with AMD engineers. Such direct engagement is essential for troubleshooting and fine-tuning NoC configurations, ensuring that the research meets the requisite industry standards and real-world requirements. The six-week period will allow for uninterrupted access, facilitating comprehensive testing and validation of the proposed optimizations.

Expected Outcomes: During this six-week trip, I will conduct detailed experiments to quantify essential performance metrics such as latency, throughput, and energy efficiency on AMD's VERSAL hardware platform. These results will be instrumental in the refinement of NoC optimization techniques and providing real-world validation for my research, ensuring that the methods are both academically rigorous and industrially relevant.

Contribution to the Project: This research trip is a vital component of my project. It enables me to test the NoC optimizations directly on industry-grade hardware and receive immediate feedback from AMD engineers. This collaboration will guarantee that the optimization techniques developed are not only theoretical but also practical and impactful for AI hardware optimization.

This local research trip will provide indispensable resources and expertise, ensuring the successful completion of my project.

Ethics

Does your research proposal involve any of the following ethical issues of special relevance?
None of the above

Does your research proposal require approval by the relevant institutional Ethics Committee?
No

Please provide a statement detailing the careful consideration you have given to the ethical implications of the proposed research (where ethical issues may arise) and how you plan to address these over the course of your award:
The proposed research on Network-on-Chip (NoC) optimization for AI accelerators involves technical work with potential ethical implications, particularly concerning data privacy, environmental impact, and the broader societal influence of AI.

1. Data Privacy and Security:

While this research does not directly involve personal data, it uses AI models and datasets for testing. To ensure ethical compliance, only anonymized, publicly available datasets will be used. AI models employed will focus solely on performance evaluation, with no processing of sensitive information. All data handling will adhere to the ethical guidelines of Trinity

College Dublin and data protection regulations like GDPR, ensuring integrity and security throughout the project.

2. Environmental Impact:
A core goal of this research is to improve the energy efficiency of AI hardware, reducing the carbon footprint of AI systems. Through energy-performance trade-off analysis, the NoC optimizations proposed will aim to significantly lower energy consumption without sacrificing performance. This focus aligns with ethical responsibilities to foster environmentally sustainable technologies.

3. Societal Impact of AI:
Enhanced AI hardware efficiency can impact various sectors, raising issues of fairness and transparency. To address these concerns, I will engage with interdisciplinary discussions on AI ethics, ensuring that hardware-level optimizations align with ethical AI practices and societal values. This will help guide the research to support responsible AI deployment.

4. Ethical Oversight and Compliance:
I will work closely with my academic supervisor and Trinity College Dublin's ethical review board to ensure compliance with ethical standards. Ethical approval will be sought where necessary, and I will remain vigilant to any evolving ethical considerations throughout the research.

This plan underscores a commitment to ethical research practices, focusing on data privacy, sustainability, and societal impact to ensure the work contributes positively to both technology and society.

Sex/gender dimension

Does your proposed research involve any of the following?
None of the above

Please provide a statement detailing whether there is a potential sex/gender dimension to be considered in carrying out your research. If your research involves any of the above, please indicate how potential sex/gender issues will be handled. If your research does not involve any of the above, please explain why there is no potential biological sex and/or social gender dimension to be considered in your proposed research. In particular, you are asked to reference the points mentioned in the 'checklist for sex/gender in research content' in the Call Document:
The proposed research on optimizing the Network-on-Chip (NoC) architecture for AI accelerators is primarily technical, focusing on hardware design, energy efficiency, and system performance. As such, it does not directly involve human participants, biological sex, or social gender aspects. The core of this study revolves around the development and evaluation of algorithms and hardware configurations, which are inherently neutral to sex and gender considerations.

Given the nature of the research, the primary objective is to enhance the technical performance of AI systems, and this process does not involve any sex- or gender-specific elements. The methodologies employed, such as simulation, benchmarking, and energy-performance analysis, are applied uniformly to hardware and software systems without any interaction or impact on human subjects. Therefore, issues related to sex and gender are not applicable in this context.

However, in acknowledging the broader implications of technological advancements, the research will be conducted with an awareness of the importance of diversity and inclusivity in the field of AI. While this specific study does not engage with sex or gender issues, it supports the notion that advancements in technology should be accessible and beneficial to all, regardless of gender.

To ensure a holistic approach, the findings and results of the research will be communicated in a manner that promotes inclusivity. Any outreach activities, publications, and presentations will be made with consideration for diverse audiences, aiming to encourage participation and interest across different gender groups in the field of AI and computer hardware research.

In summary, there is no direct sex or gender dimension in the technical content of this research. The project focuses on hardware and performance optimization, which does not involve human participants. Nonetheless, the broader dissemination of the research outcomes will be handled with an inclusive approach.

Data management

Data Management

> Please provide a data management plan which addresses the following:
> - How will data be exploited and/or shared/made accessible for verification and reuse?
> - How data will be curated and preserved?
> - If applicable, how do you plan to make data FAIR (findable, accessible, interoperable and reusable)?
> - If data cannot be made available, why?

Data Management Plan:

1. Data Exploitation and Sharing:
The research will generate NoC simulation results, benchmarking data, and performance metrics. These datasets will be shared through publicly accessible repositories like Zenodo or Figshare, including detailed documentation for verification and reuse. The data will cover the experimental setup, parameters used, and NoC configurations. Proprietary data from industry partners, if any, will be managed according to confidentiality agreements, ensuring compliance and appropriate data sharing.

2. Data Curation and Preservation:
Data will be curated by organizing it with comprehensive metadata, describing the experimental setup, data formats, and parameters. Preservation will be ensured by storing data in secure, long-term digital repositories with persistent identifiers (DOIs). Regular backups will be maintained. Each dataset will include a README file with usage instructions, licensing terms, and contact details for further inquiries.

3. Making Data FAIR:
To ensure data is FAIR:
Findable: Data will have unique DOIs and be indexed in public repositories.
Accessible: Data will be available in open-access repositories, with clear access conditions.
Interoperable: Data will use standard formats compatible with common tools.
Reusable: Detailed documentation and metadata will be provided, with clear licensing (e.g., Creative Commons) for reuse.

4. Data Availability and Restrictions:
Most data will be publicly available. If any data involve proprietary information (e.g., from AMD), restrictions will apply. In such cases, aggregated or anonymized data will be shared to protect intellectual property and comply with confidentiality. Documentation will outline any restrictions and access conditions.

This plan ensures research data is curated, preserved, and accessible for future use, fostering transparency and reuse in the research community.

Applicant declaration

I hereby declare that I have read and accept the applicant requirements as set out in the Call Document and Terms and Conditions and Guide for Applicants on the Irish Research Council **WEBSITE**:
I agree

I confirm that the information supplied in this application is correct and recognise that should it become apparent that any of the information provided is inaccurate or unverifiable with appropriate documentation, it will result in the application automatically being deemed ineligible:
I agree

I hereby declare that this application is entirely my own work and understand that it will be subject to plagiarism checks.

Please note that random sampling for evidence of plagiarism will be carried out during the assessment process. Applicants who have been found to plagiarise will be prohibited from applying for Irish Research Council funding in the future. Suspected instances of plagiarism will be brought to the attention of the higher education institution:

I agree