



**VietNam National University  
University of Engineering and Technology**

# **Simulating using ModelSim**

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**Laboratory for Smart Integrated Systems**

# Objectives

- In this lecture you will be introduced to:
  - Simulating your design by ModelSim tool

# ModelSim Overview

- **Mentor Graphics**

- **Target Use:**

- ✓ *A verification and simulation tool for VHDL, Verilog, SystemVerilog, SystemC, and mixed-language designs*

- **ModelSim PE Student Edition**

- ✓ Free download at:  
[http://www.mentor.com/company/higher\\_ed/modelsim-student-edition](http://www.mentor.com/company/higher_ed/modelsim-student-edition)
- ✓ Support for both VHDL and Verilog designs (non-mixed)
- ✓ Capacity: 10,000 lines of executable code
- ✓ Suitable for student to do academic coursework and basic educational projects.

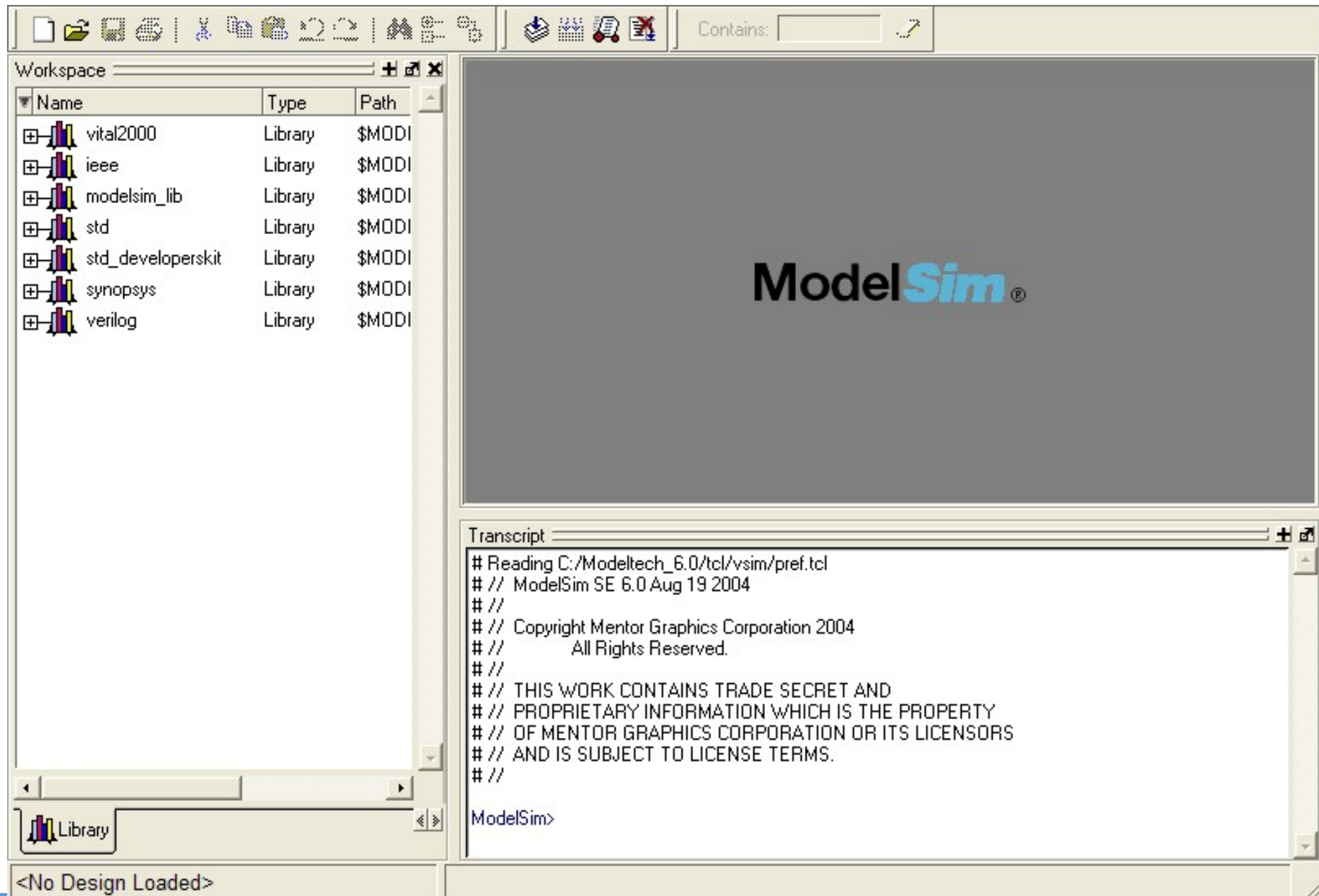
# Where to Find ModelSim Documentation

| Document  | Format       | How to get it  |
|---|--------------|--|
| <i>Installation &amp; Licensing Guide</i>                   | PDF          | <b>Help &gt; PDF Bookcase</b>                                    |
|   | HTML and PDF | <b>Help &gt; InfoHub</b>   |
| <i>Quick Guide</i><br>(command and feature quick-reference) | PDF          | <b>Help &gt; PDF Bookcase</b><br>and<br><b>Help &gt; InfoHub</b> |
| <i>Tutorial</i>   | PDF          | <b>Help &gt; PDF Bookcase</b>                                    |
|   | HTML and PDF | <b>Help &gt; InfoHub</b>   |
| <i>User's Manual</i>  | PDF          | <b>Help &gt; PDF Bookcase</b>                                    |
|   | HTML and PDF | <b>Help &gt; InfoHub</b>   |
| <i>Reference Manual</i>                                     | PDF          | <b>Help &gt; PDF Bookcase</b>                                    |
|   | HTML and PDF | <b>Help &gt; InfoHub</b>   |

# How to Use ModelSim

- **Create a new directory for this course** (*e.g.* `C:/work_station/ELT6061_LSI_design/`)
- **Run ModelSim**
- **Select *File > Change Directory* and change to the directory you created in step 1**

# Main Windows

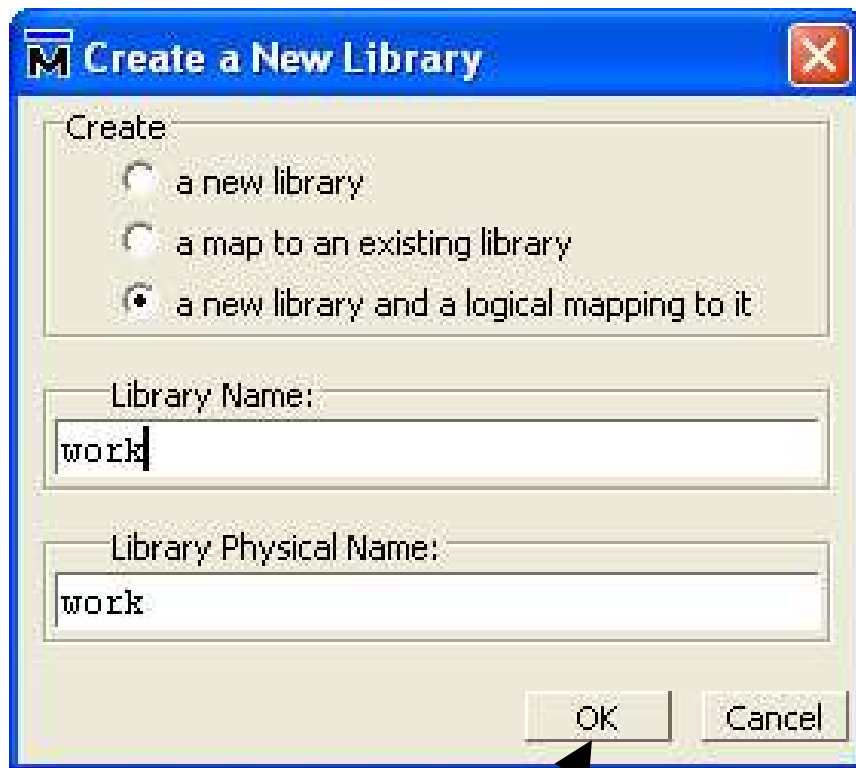


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# How to Use ModelSim

## ➤ Create the working Library

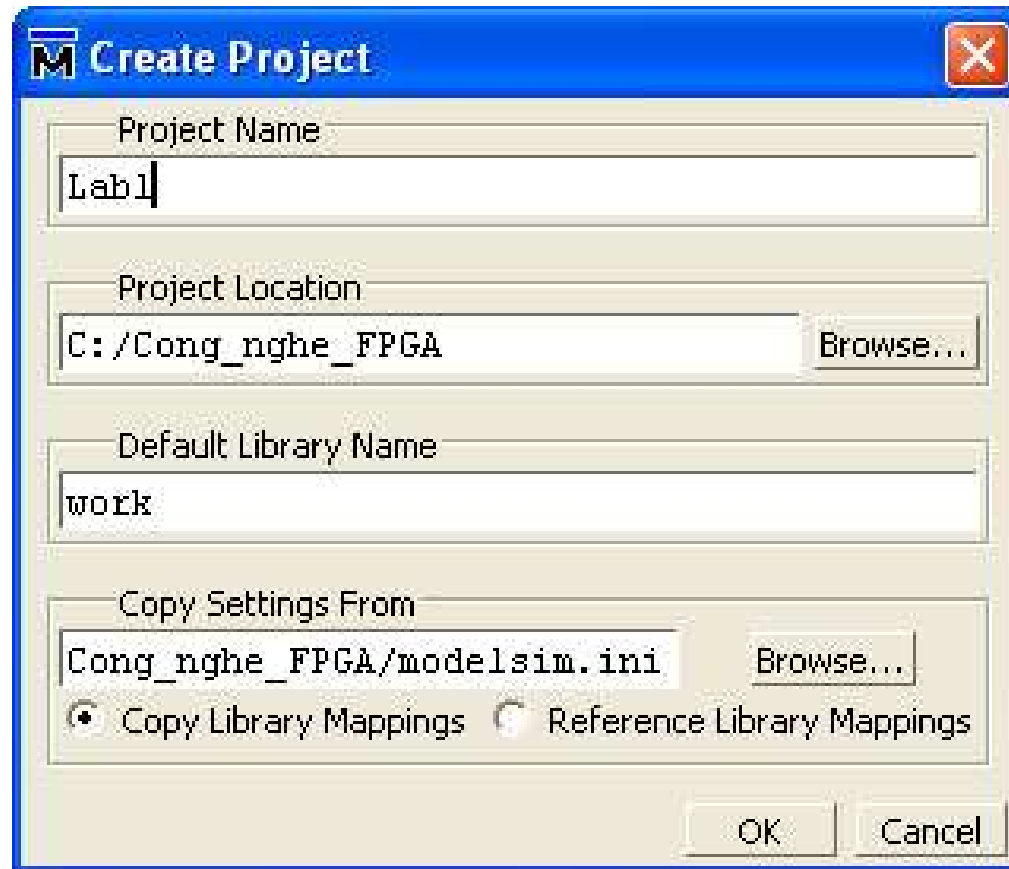
- ✓ Select **File > New > Library**
- ✓ Type **work** in the Library Name field
- ✓ Click **OK**.



| Name              | Type    | Path                             |
|-------------------|---------|----------------------------------|
| work              | Library | work                             |
| floatfixlib       | Library | \$MODEL_TECH/./floatfixlib       |
| mtiAvm            | Library | \$MODEL_TECH/./avm               |
| mtiOvm            | Library | \$MODEL_TECH/./ovm-2.0.2         |
| mtiPA             | Library | \$MODEL_TECH/./pa_lib            |
| mtiUPF            | Library | \$MODEL_TECH/./upf_lib           |
| sv_std            | Library | \$MODEL_TECH/./sv_std            |
| vital2000         | Library | \$MODEL_TECH/./vital2000         |
| ieee              | Library | \$MODEL_TECH/./ieee              |
| modelsim_lib      | Library | \$MODEL_TECH/./modelsim_lib      |
| std               | Library | \$MODEL_TECH/./std               |
| std_developerskit | Library | \$MODEL_TECH/./std_developerskit |
| synopsys          | Library | \$MODEL_TECH/./synopsys          |
| verilog           | Library | \$MODEL_TECH/./verilog           |

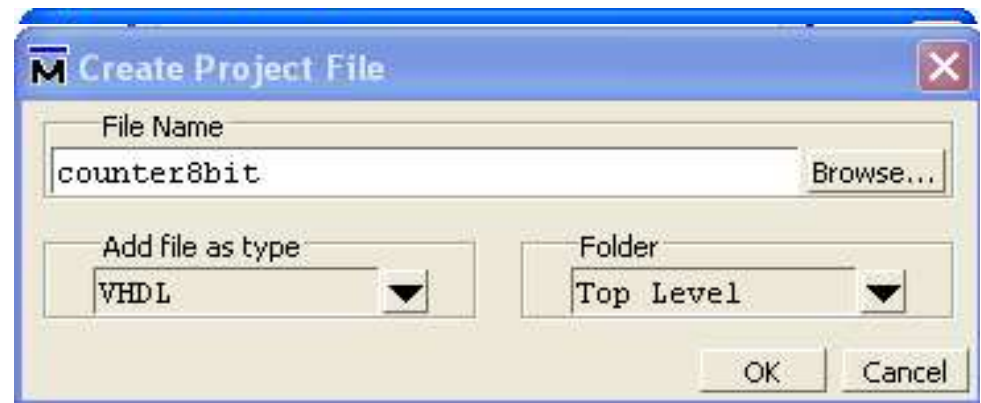
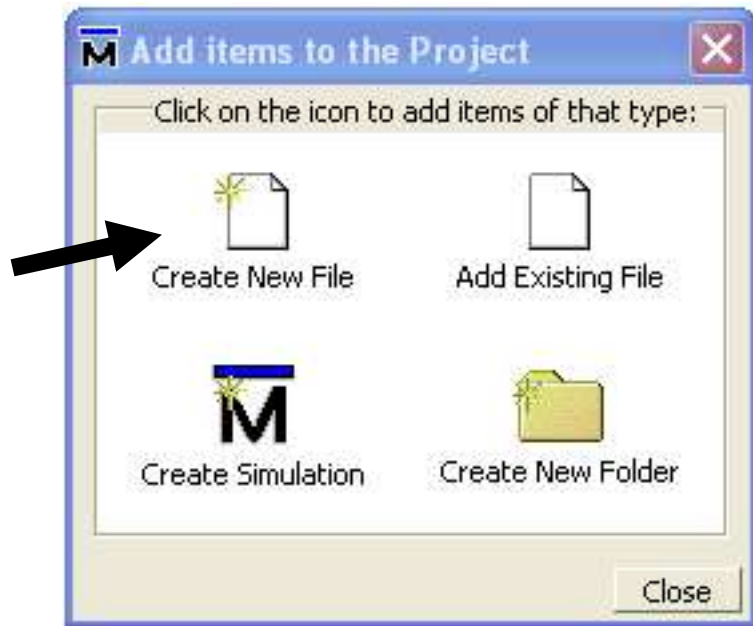
# How to Use ModelSim

- Create a new Project
  - Select: File -> New -> Project



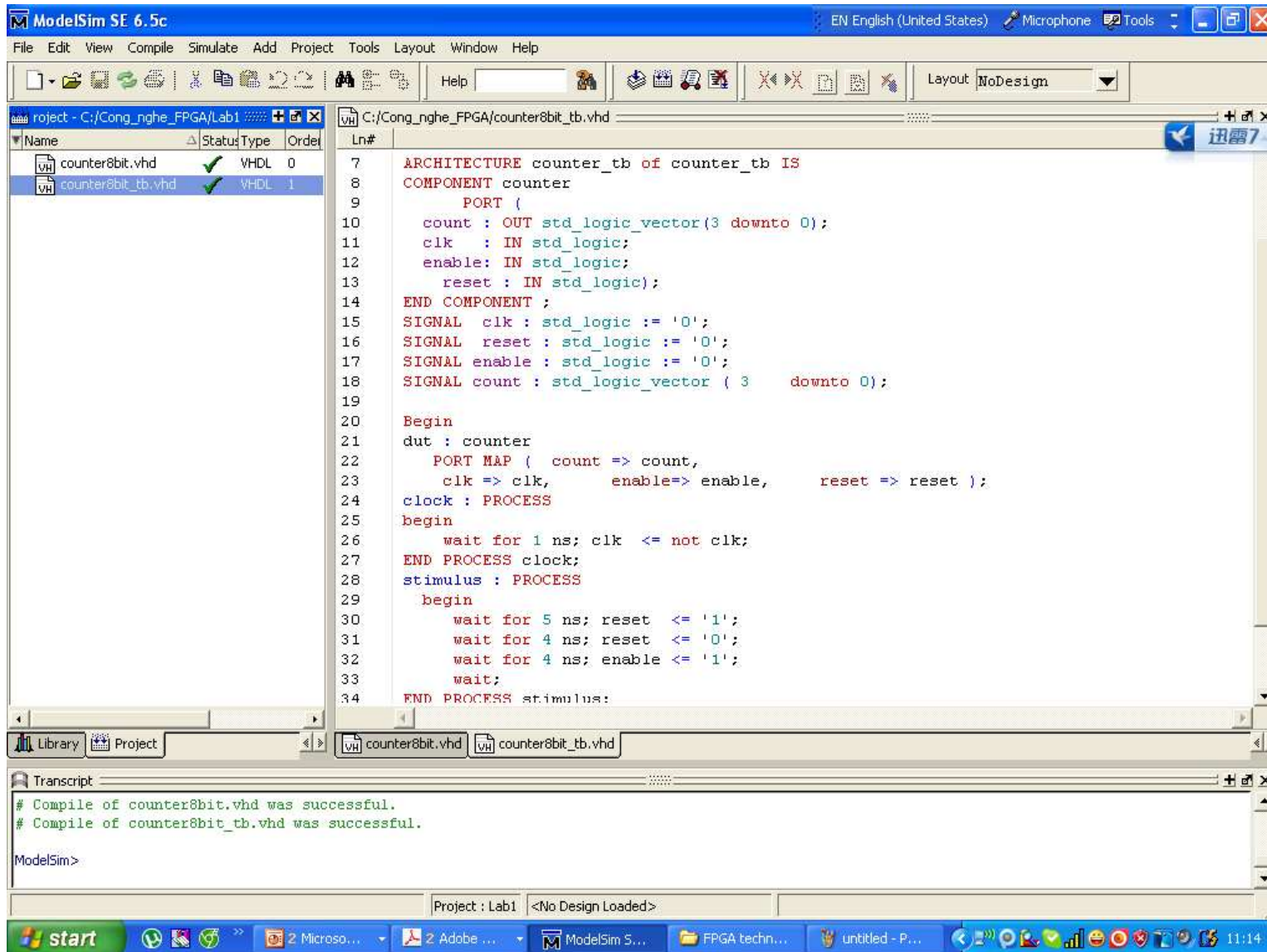


# How to Use ModelSim



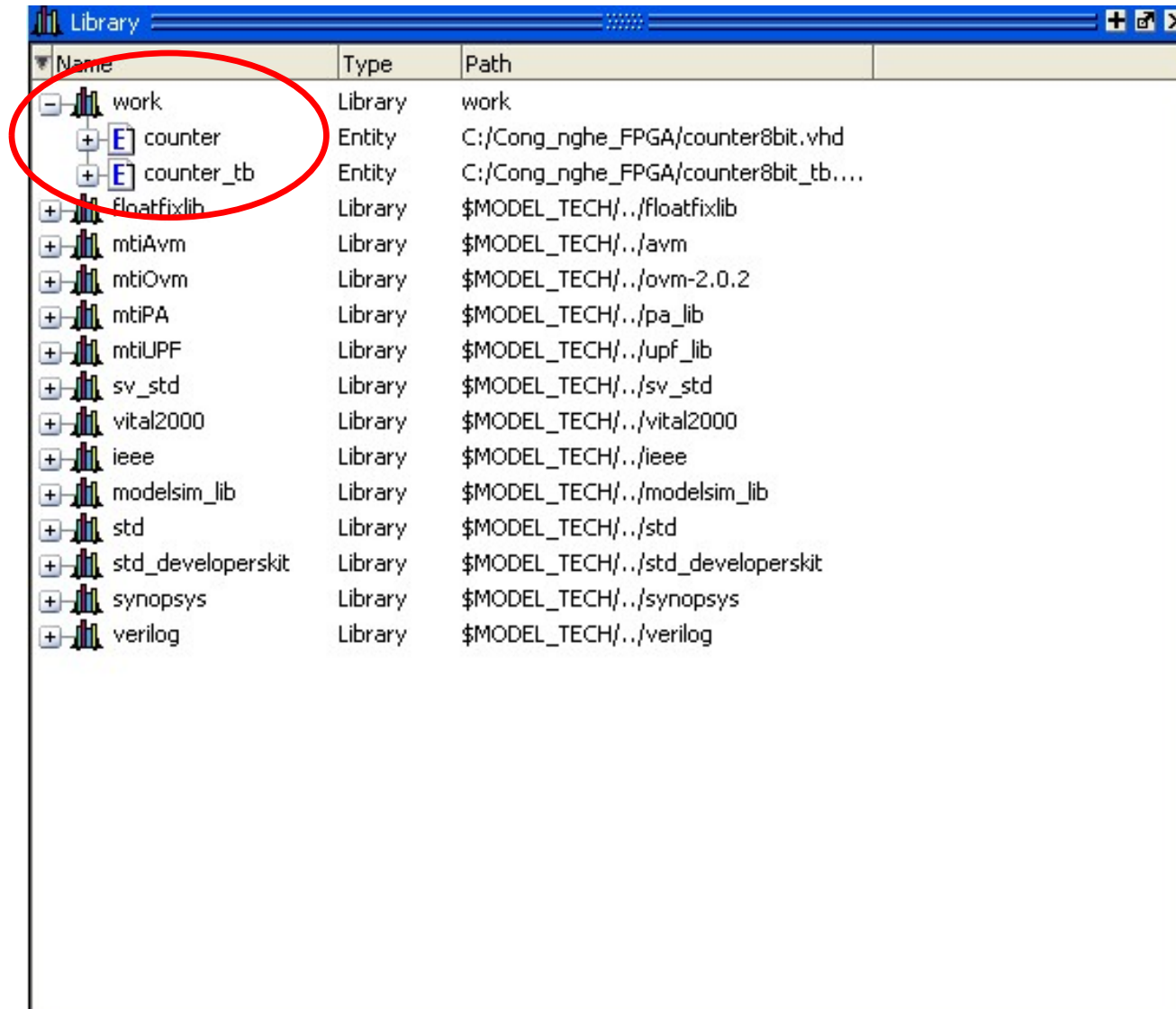
# How to Use ModelSim

## Design Entry and Compilation



# How to Use ModelSim

## Library Window



# How to Use ModelSim

## Optimize for Design Visibility

➤ Use the *vopt* command to optimize the design with full visibility into all design units.

➤ Enter the following command at the QuestaSim> prompt in the Transcript window:

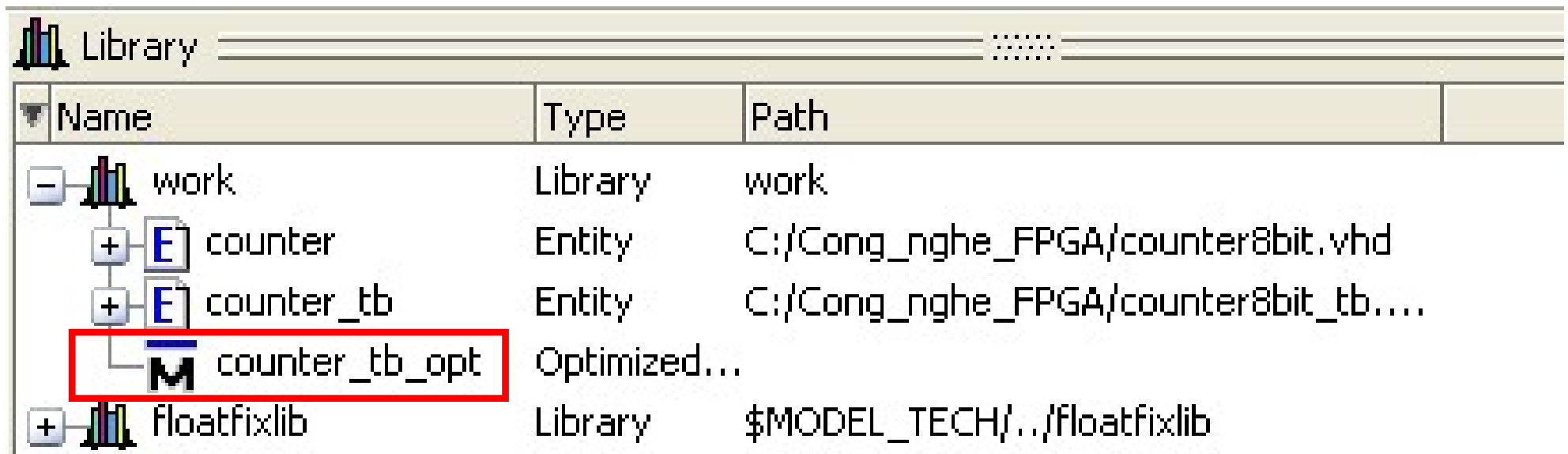
```
vopt +acc counter_tb -o counter_tb_opt
```

Where:

- The +acc switch provides visibility into the design for debugging purposes.
- The -o switch allows you designate the name of the optimized design file (testcounter\_opt).

# How to Use ModelSim

## Optimize for Design Visibility



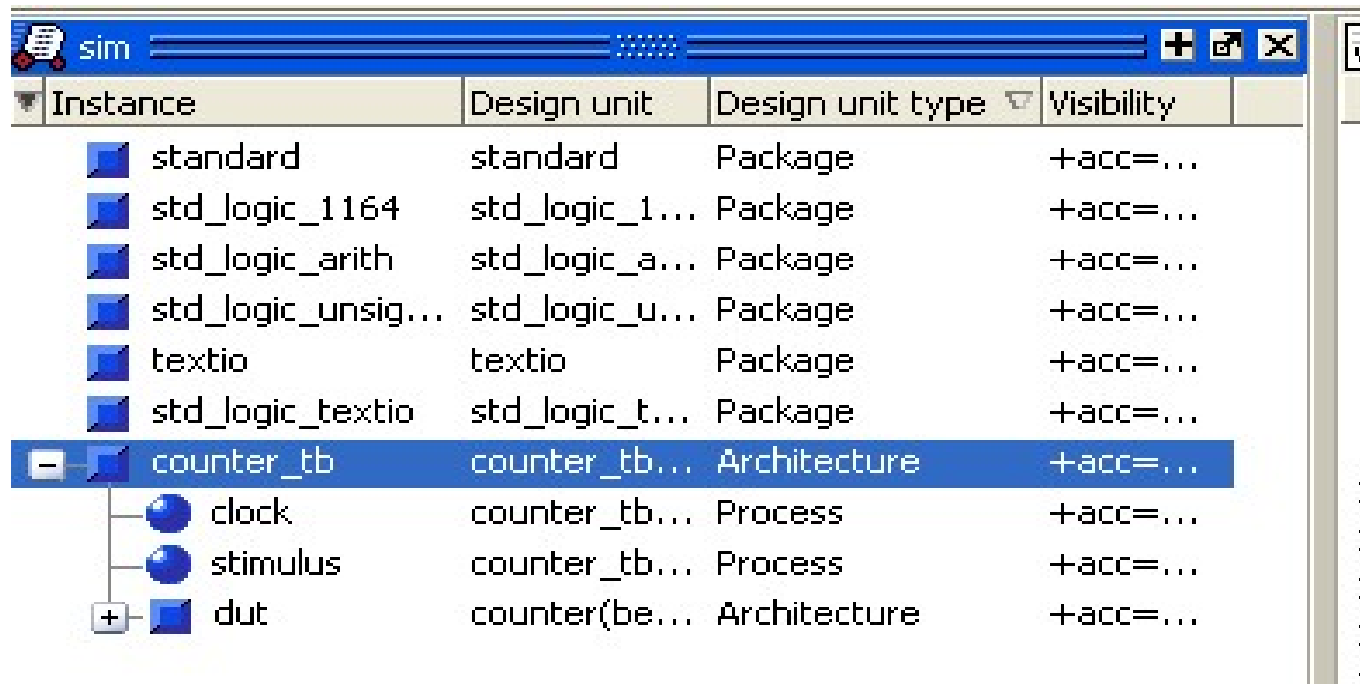
The screenshot shows the ModelSim Library window with a tree view on the left and a table on the right. The tree view shows a hierarchy starting with 'work', which contains 'counter' and 'counter\_tb'. 'counter\_tb' contains 'counter\_tb\_opt'. The table on the right lists the items in the tree with their names, types, and paths. The 'counter\_tb\_opt' entry is highlighted with a red box.

| Name           | Type         | Path                                 |
|----------------|--------------|--------------------------------------|
| work           | Library      | work                                 |
| counter        | Entity       | C:/Cong_nghe_FPGA/counter8bit.vhd    |
| counter_tb     | Entity       | C:/Cong_nghe_FPGA/counter8bit_tb.... |
| counter_tb_opt | Optimized... |                                      |
| floatfixlib    | Library      | \$MODEL_TECH/../../floatfixlib       |

# How to Use ModelSim

## Load the Design

1. Load the counter\_tb design unit.
  - a. Use the optimized design name to load the design with the *vsim* command:  
`vsim counter_tb_opt`



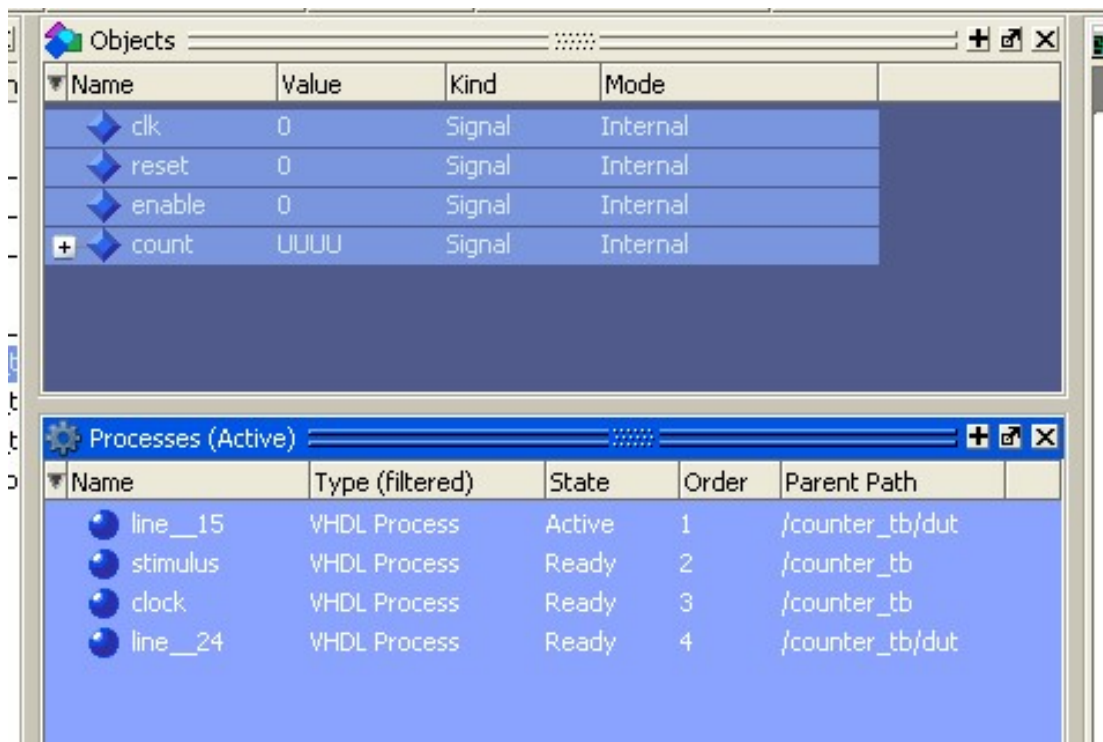
The screenshot shows the 'sim' window in ModelSim. The design hierarchy table is displayed with the following columns: Instance, Design unit, Design unit type, and Visibility. The 'counter\_tb' instance is selected, and its sub-components are expanded.

| Instance           | Design unit    | Design unit type | Visibility |
|--------------------|----------------|------------------|------------|
| standard           | standard       | Package          | +acc=...   |
| std_logic_1164     | std_logic_1... | Package          | +acc=...   |
| std_logic_arith    | std_logic_a... | Package          | +acc=...   |
| std_logic_unsig... | std_logic_u... | Package          | +acc=...   |
| textio             | textio         | Package          | +acc=...   |
| std_logic_textio   | std_logic_t... | Package          | +acc=...   |
| counter_tb         | counter_tb...  | Architecture     | +acc=...   |
| clock              | counter_tb...  | Process          | +acc=...   |
| stimulus           | counter_tb...  | Process          | +acc=...   |
| dut                | counter(be...  | Architecture     | +acc=...   |

# How to Use ModelSim

## Load the Design

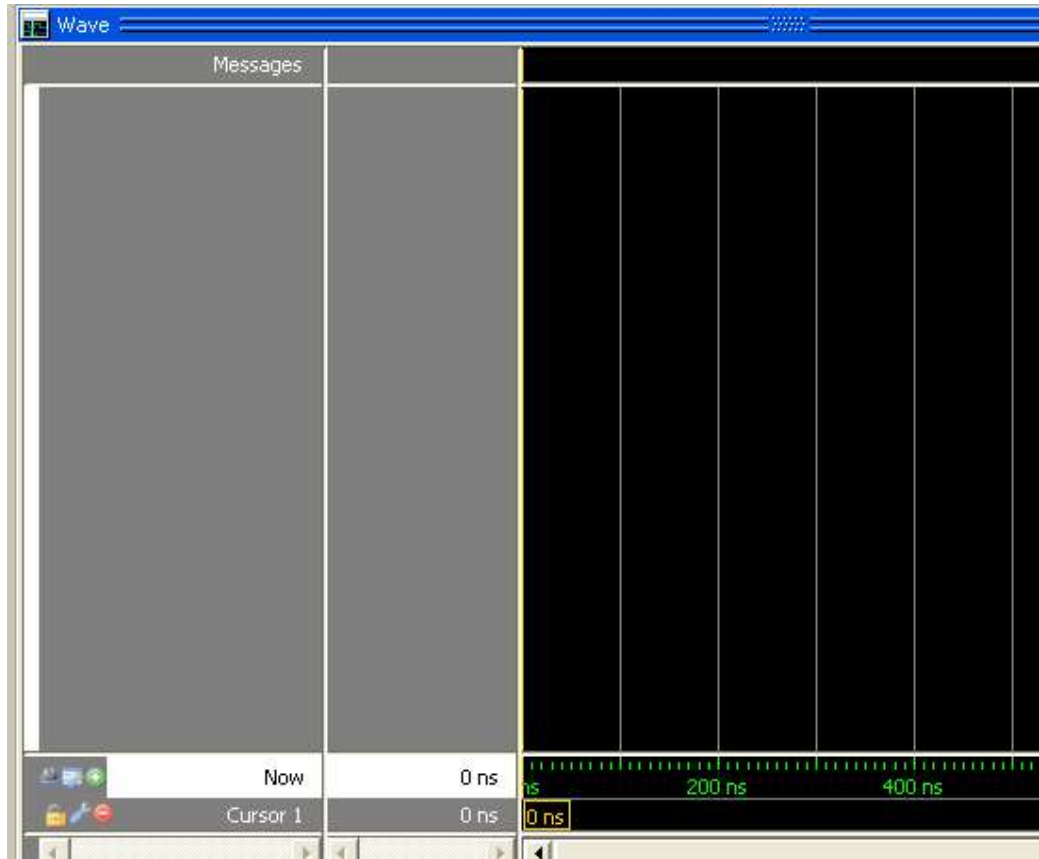
1. Load the counter\_tb design unit.
  - a. Use the optimized design name to load the design with the *vsim* command:  
`vsim counter_tb_opt`



# How to Use ModelSim

## Run the Simulation

1. Open the Wave window.
    - a. Enter **view wave** at the command line.
- You can also use the **View > Wave** menu selection to open a Wave window.

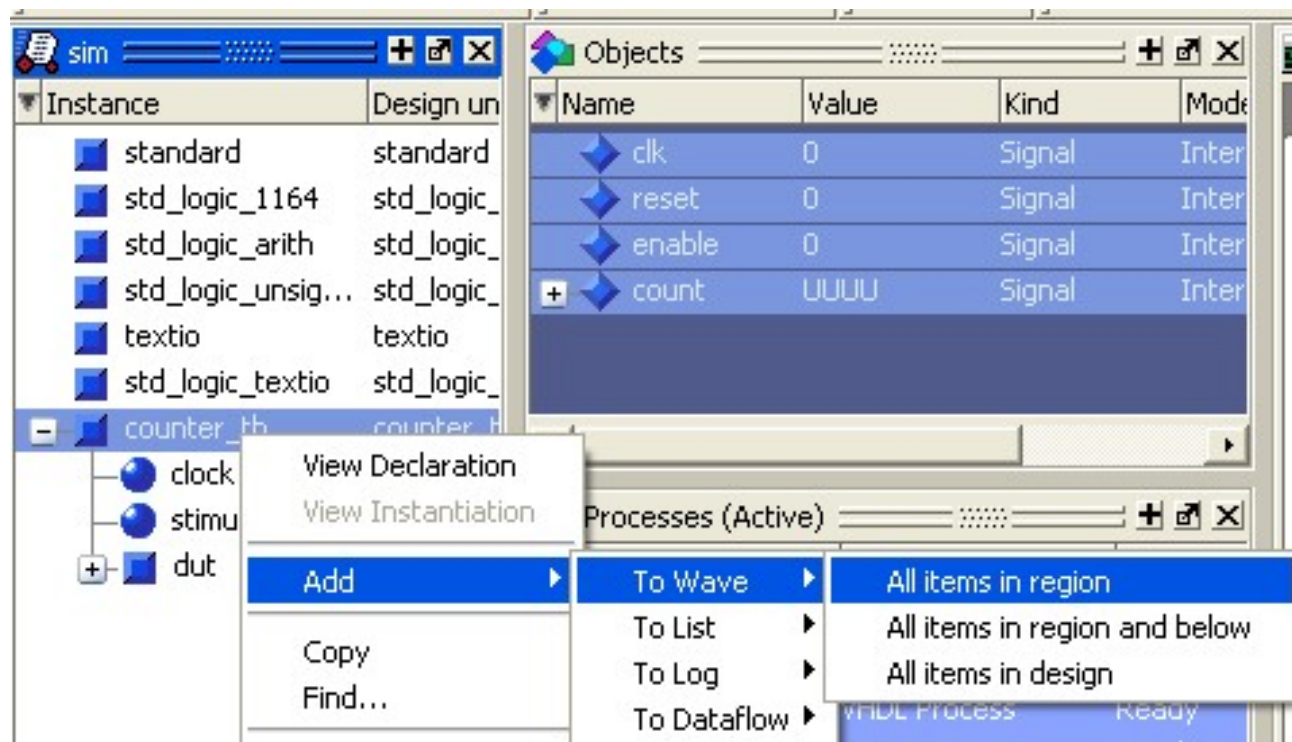




# How to Use ModelSim

## Run the Simulation

2. Add signals to the Wave window.
  - a. In the Structure (sim) window, right-click *counter\_tb* to open a popup context menu.
  - b. Select **Add > To Wave > All items in region**.All signals in the design are added to the Wave window.



# How to Use ModelSim

## Run the Simulation

3. Run the simulation.

a. Click the Run icon.



b. Enter run 500 at the VSIM> prompt in the Transcript window

