VietNam National University
University of Engineering and Technology

# THIẾT KẾ MẠCH TÍCH HỢP SỐ (DIGITAL IC DESIGN)

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# Lecture 1: Introduction to Microelectronics

# Objectives

**In this lecture you will be introduced to:**

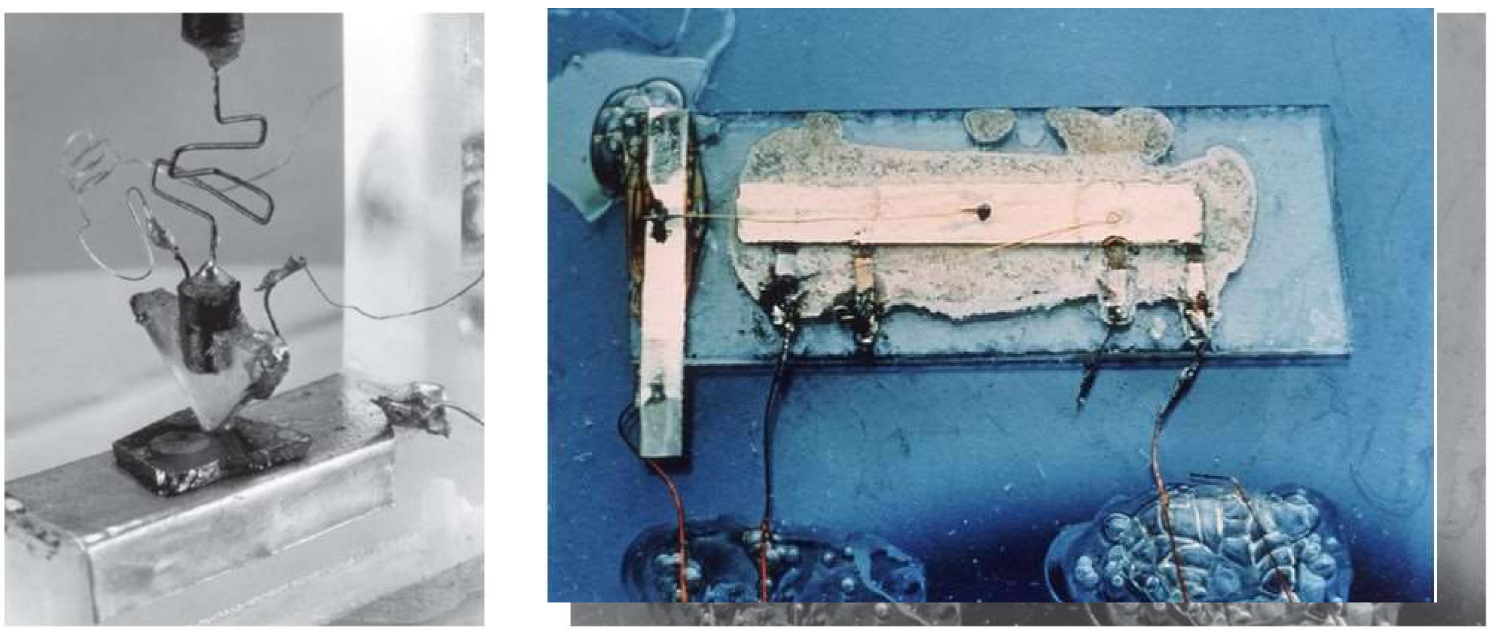
- The key terms and concepts behind digital integrated circuits
- IC Design Flow and Methodology

# Outline

- **Evolution of ICs**
- Applications of ICs
- What is a digital system
- Classification of digital ICs
- IC Design Flow and Methodology
- Summary

# What is IC?

- **Integrated circuits (IC or Chip):** set of electronic *circuits (including* many transistors interconnected toghether*)* on one small piece ("chip") of semiconductor material.



(a) (b)

(a) First transistor (1947, Bell Laboratories) and (b) the first integrated circuit Flip-Flop with two transistors (1958, Jack Kilby, Texas Instruments.)

# What is VLSI?

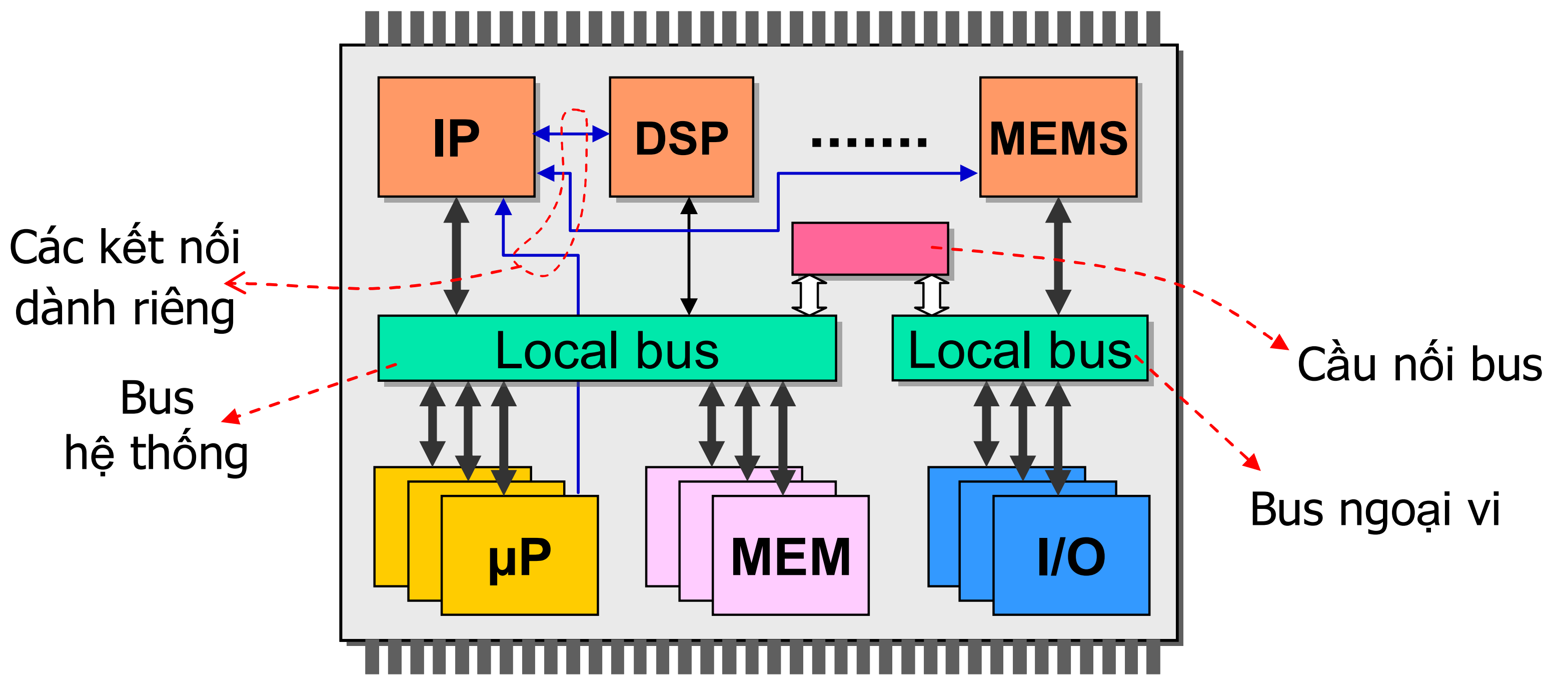
- **VLSI:** Very Large Scale Integration
  - Combining of many, many functional circuits on a single chip,
  - Being started with hundreds of thousands of transistors in the early 1980s, and continues beyond several billion transistors as of 2008.
  - For Example, in 2008:
    - ✓ Intel's Itanium microprocessor contained more than 2 billion transistors,
    - ✓ A 16 Gb Flash memory contained more than 4 billion transistors.

Annual growth rate of 53% over 50 years (1958-2008). No other technology in history has sustained such a high growth rate lasting for so long!

- ***ASIC:*** application-specific integrated circuit which could be a VLSI

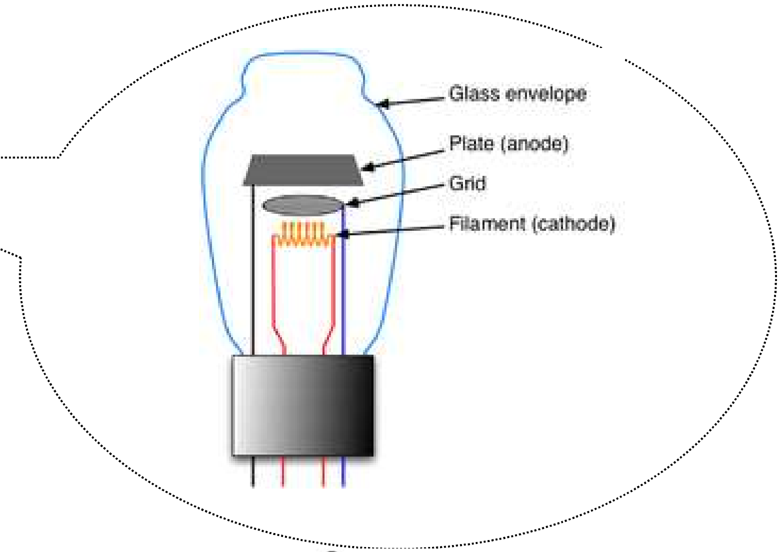
# What is SoC?

- **SoC:** System-on-Chip
  - Integrating of a complete computing system on a single chip of 1 inch$^2$ in size, started in the early 1990s;
  - Advantage: high-performance, low-power consumption, small area.

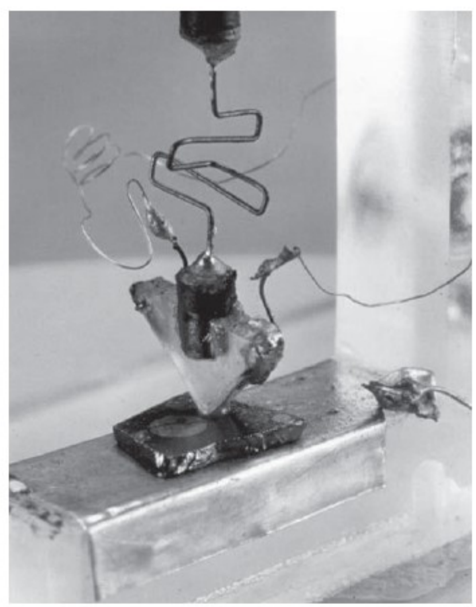


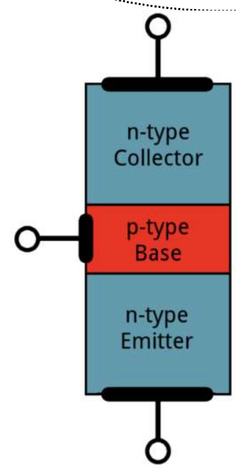
# Evolution of VLSI Systems

**The first half of the twentieth century:** Large, expensive, power-hungry, and unreliable **vacuum tubes**




**TRANSISTOR (1947):** is a resistor or semiconductor device which can amplify electrical signals as they are transferred through it from input to output terminals.






**Solid-state electronics: more reliable, less noisy, and more power-efficient**

# Evolution of VLSI Systems

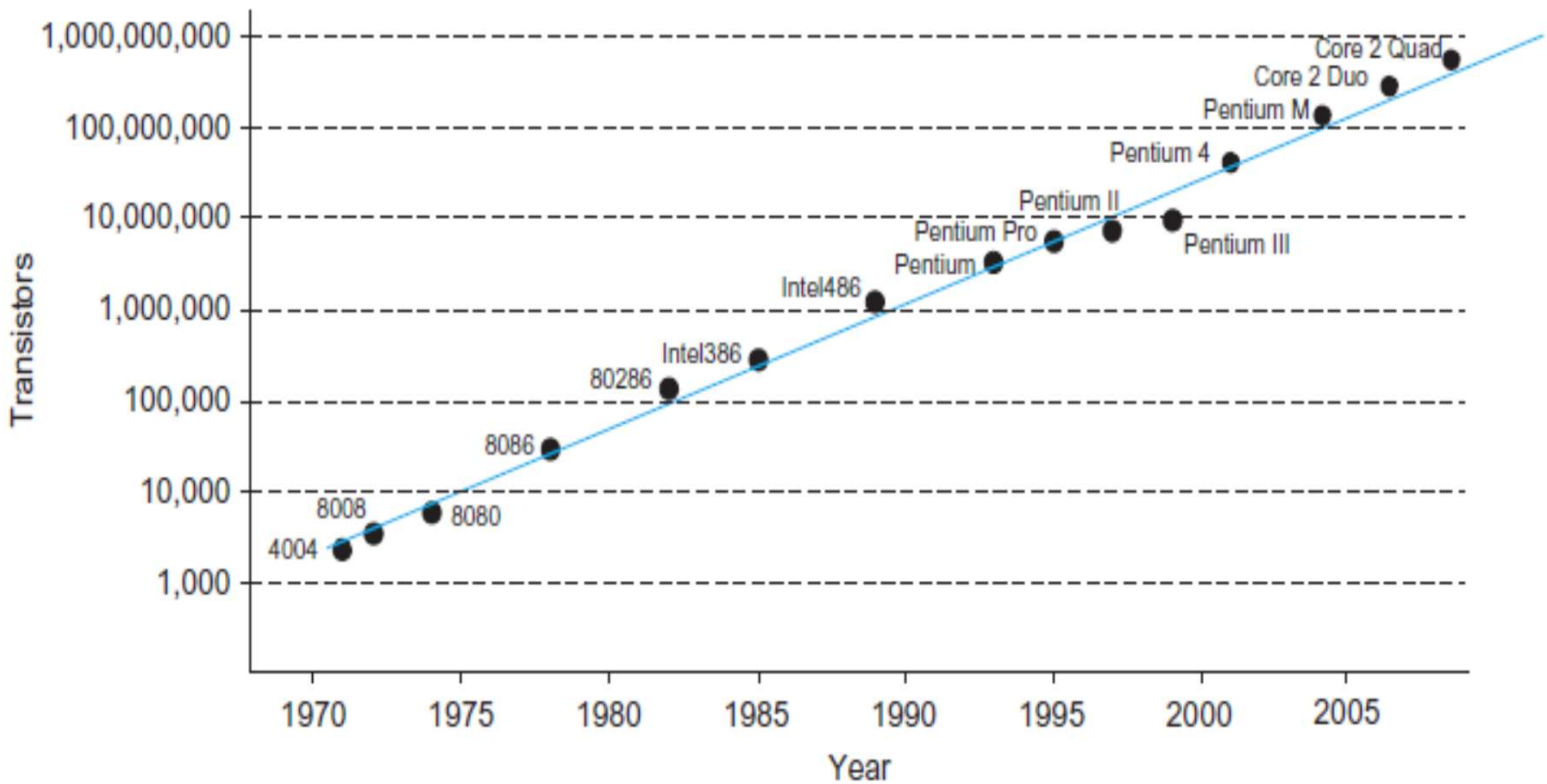
- **In 1947, Bipolar transistors:**
  - The quiescent power dissipated by these base currents limits the maximum number of transistors that can be integrated onto a single die.
- **By the 1960s, Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)**
  - Include nMOS and pMOS, using n-type and p-type silicon
  - *Almost zero control current* while idle.
  - Low cost because each transistor occupied less area and the fabrication process was simpler
  - Early commercial processes used only pMOS transistors suffered from poor performance and reliability

# Evolution of VLSI Systems

- **In 1963, the first CMOS (Complementary MOS) logic gates**
  - Composed of both nMOS and pMOS transistors
  - Consumed only nanowatts of power, six orders of magnitude less than their bipolar counterparts
- **Processes using nMOS transistors became common in the 1970s**
  - nMOS process was cheaper than CMOS
  - nMOS logic gates still consumed power while idle
- **In the 1980s, CMOS processes have essentially replaced nMOS and bipolar processes for nearly all digital logic applications**
  - Hundreds of thousands of transistors were integrated onto a single die

# Evolution of VLSI Systems

- **Moore's Law (by Gordon Moore since 1965)**
  - The transistor count on a chip will be doubling every 18 months




**Transistors in Intel microprocessors: the number of transistors has doubled every 26 months**

# Evolution of VLSI Systems

- **The level of integration of chips:** the number of logic gates or transistors in a single package

| Category | Year | Density (gates) |
|---|---|---|
| Single transistor | 1947 | 1 device |
| The first Logic gate | 1958 | 1 |
| Small scale integration (SSI) | 1964 | Up to 10 |
| Medium scale integration (MSI) | 1967 | 10-100 |
| Large scale integration (LSI) | 1972 | 100-1,000 |
| Very large scale integration (VLSI) | 1978 | 1,000-10,000 |
| Ultra large scale integration (ULSI) | 1989 | $\geq$ 10,000 |
| System Level Integration (SLI)/System-on-Chip (SOC) | Late 1990s | > 10 million |

# Evolution of VLSI Systems

- **Dennard's Scaling Law:**
  - As transistors shrink, they become **faster**, consume less power, and are cheaper to manufacture

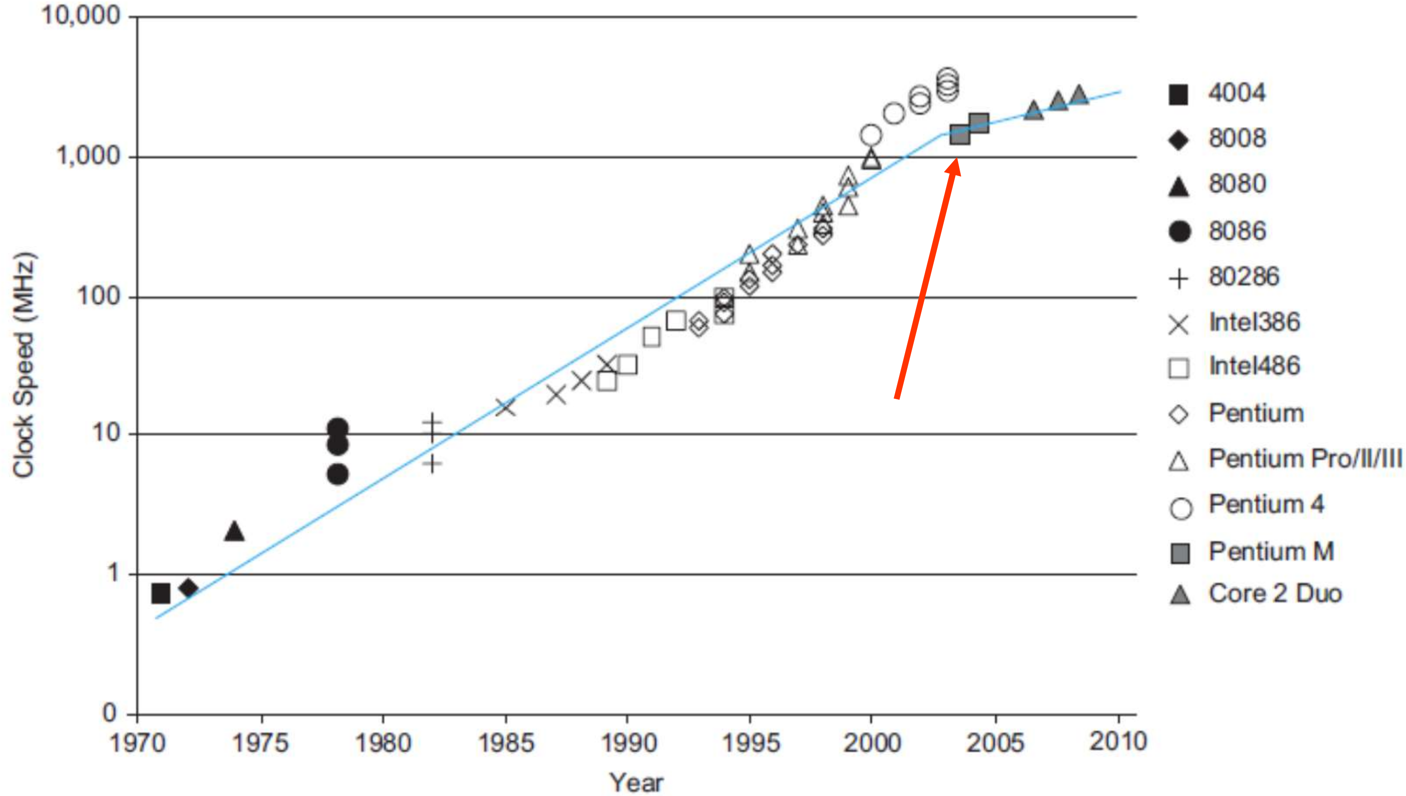
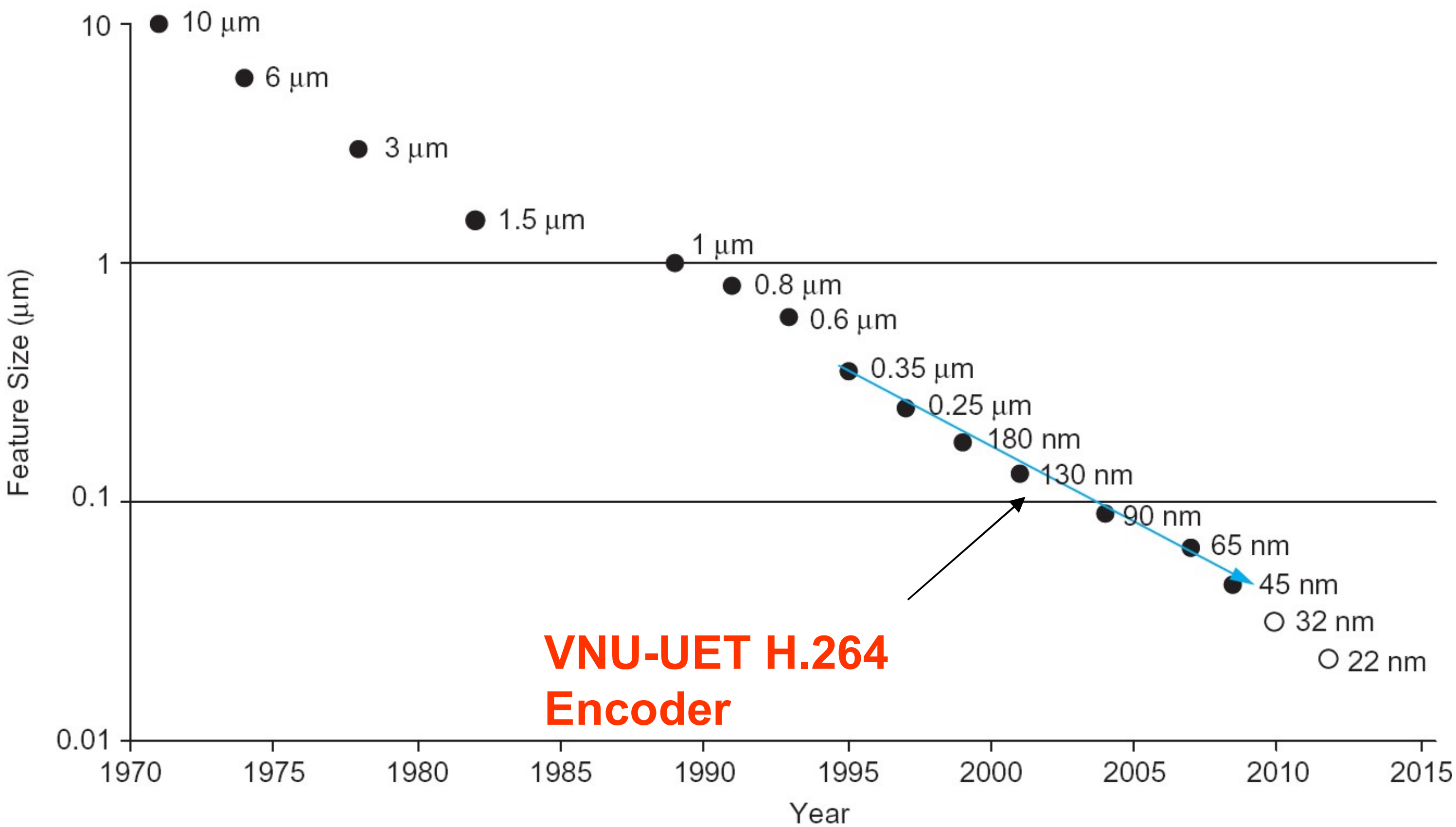



**Fig. 3 Clock frequencies of Intel microprocessors: clock frequencies have doubled roughly every 34 months**

# Evolution of VLSI Systems

- **Feature size of a CMOS manufacturing process:**
  - Refers to the minimum dimension of a transistor that can be reliably built.

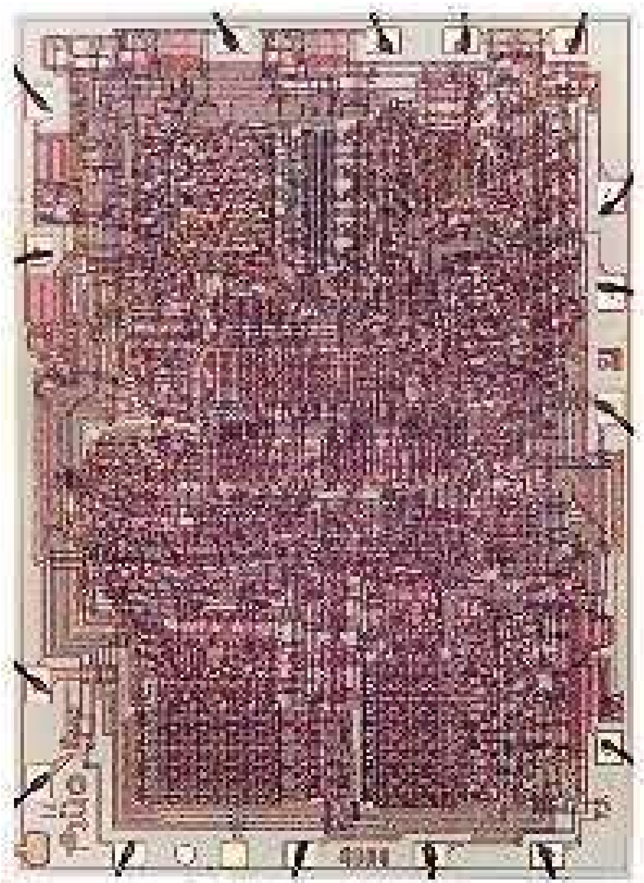



**Process generations and Future predictions from [SIA2007]**

(every 2-3 years with 30% smaller feature size)

- 10 µm – 1971
- 6 µm – 1974
- 3 µm – 1977
- 1.5 µm – 1981
- 1 µm – 1984
- 800 nm – 1987
- 600 nm – 1990
- 350 nm – 1994
- 250 nm – 1996
- 180 nm – 1999
- 130 nm – 2001
- 90 nm – 2003
- 65 nm – 2005
- 45 nm – 2007
- 32 nm – 2009
- 22 nm – 2012
- 14 nm – 2014
- 10 nm – 2016
- 7 nm – 2018
- 5 nm – 2019
- 3 nm – *~2021*

# Gallery - Early Processors



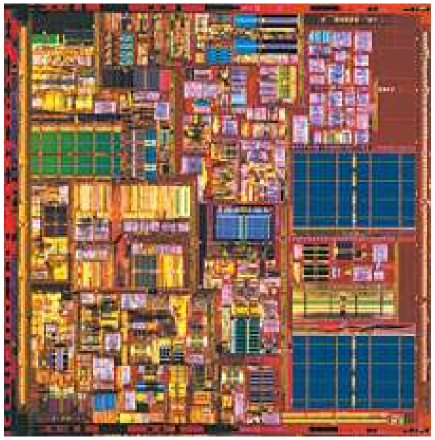
**Intel 4004 (1971)**
**First µP - 2300 xtors**
**L=10µm**

- Introduction date:
  **<u>November 15, 1971</u>**
- Clock speed: 108 KHz
- Number of transistors: 2,300
  (10 microns)
- Bus width: 4 bits
- Addressable memory: 640 bytes
- Typical use:
  calculator, first microcomputer chip, arithmetic manipulation

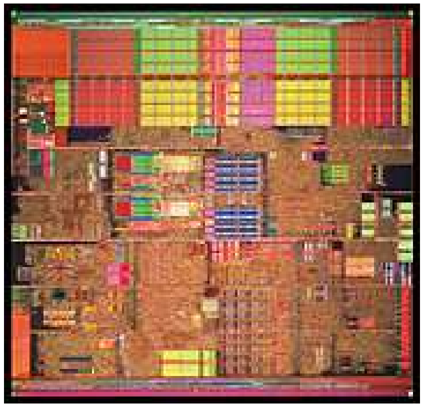
# Gallery - Current Processors

Process Shrinks →

**Pentium® 4**
**42M transistors / 1.3-1.8GHz**
**49-55W**
**L=180nm**



**Pentium® 4 "Northwood"**
**55M transistors / 2-2.5GHz**
**55W**
**L=130nm Area=131mm²**

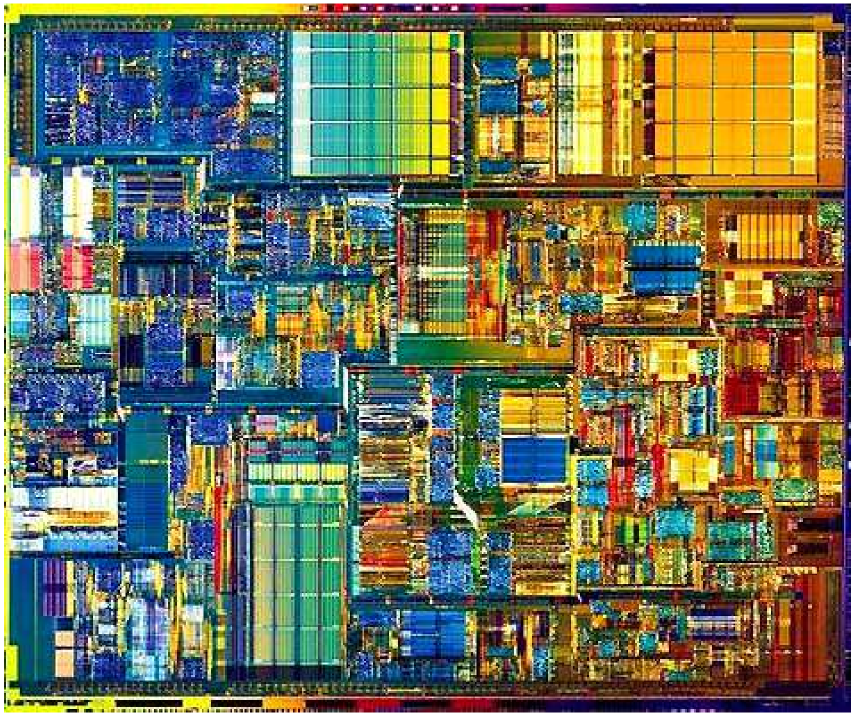


**Pentium® 4 "Prescott"**
**125M transistors / 2.8-3.4GHz**
**115W**
**L=90nm Area=112mm²**

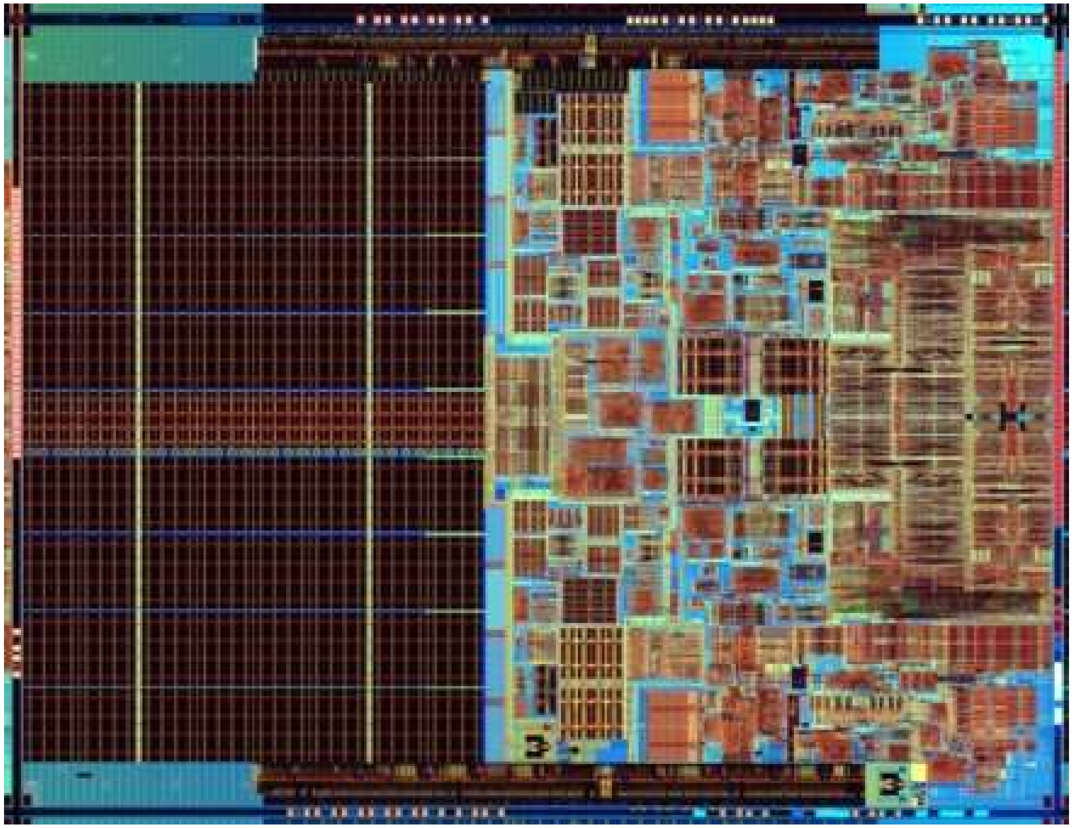
Image courtesy Intel Corporations

# Pentium 4

- 0.18-micron process technology
  **(2, 1.9, 1.8, 1.7, 1.6, 1.5, and 1.4 GHz)**
  - Introduction date: August 27, 2001 (2, 1.9 GHz); ...; November 20, 2000 (1.5, 1.4 GHz)
  - Level Two cache: 256 KB Advanced Transfer Cache (Integrated)
  - System Bus Speed: 400 MHz
  - SSE2 SIMD Extensions
  - Transistors: 42 Million
  - Typical Use: Desktops and entry-level workstations
- 0.13-micron process technology
  **(2.53, 2.2, 2 GHz)**
  - Introduction date: January 7, 2002
  - Level Two cache: 512 KB Advanced
  - Transistors: 55 Million



# Gallery – Multi-core Processors

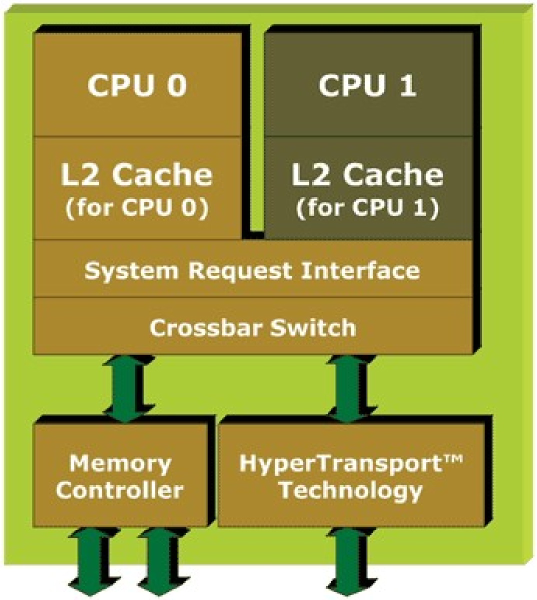


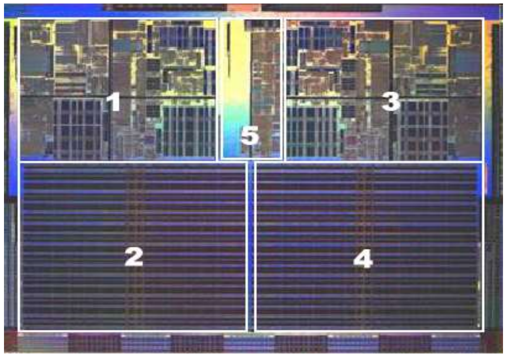
**Intel Core 2 Duo "Conroe"**
**291M transistors / 2.67GHz / 65W**
**L=65nm Area=143mm²**

# Gallery - Multi-core Processors

- Multi-core processors
  - Increase performance
  - Better Ratio of cost to performance
  - Low Power consumption

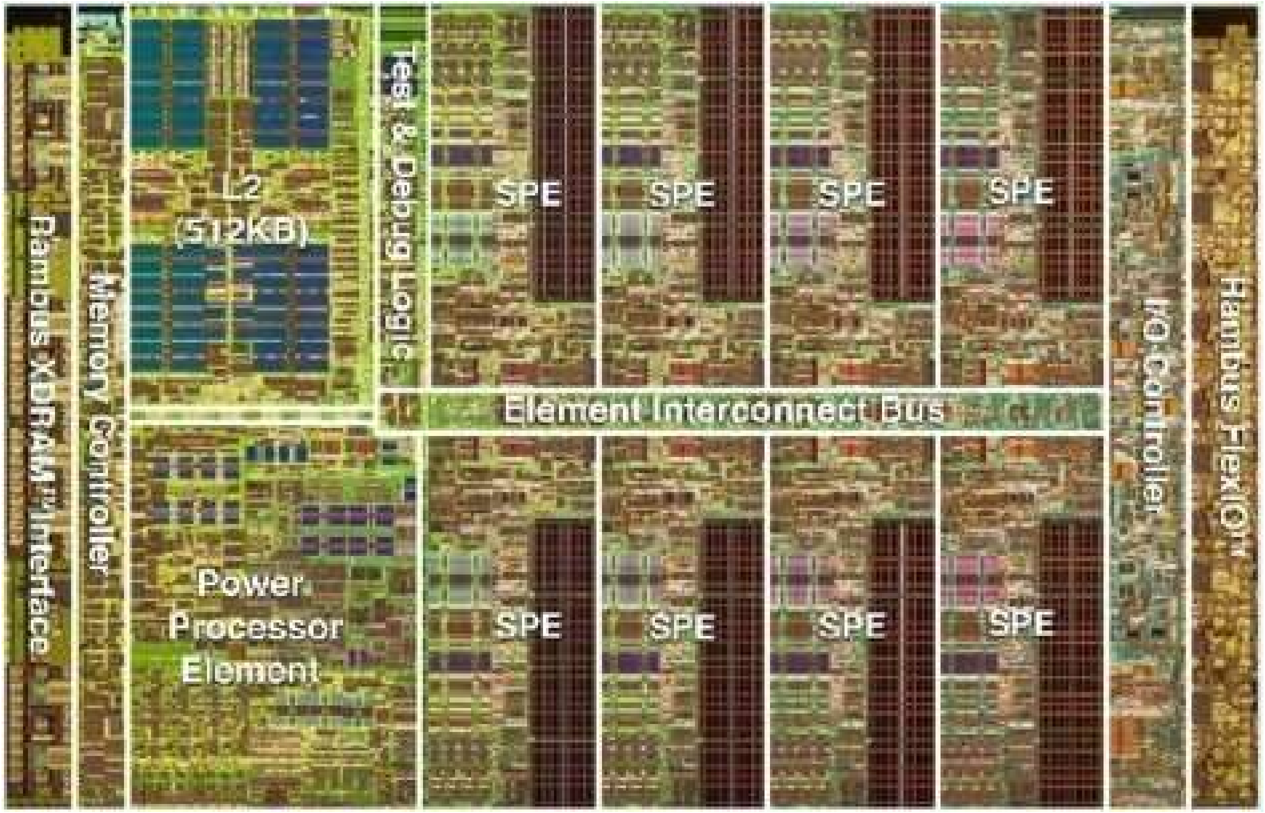
- Challenges
  - Complexity
  - Tasks management
  - On-chip communication
  - Chip temperature
  - etc.




**Athlon 64 X2 4800+ and 4400+**

# Gallery - Current Processors

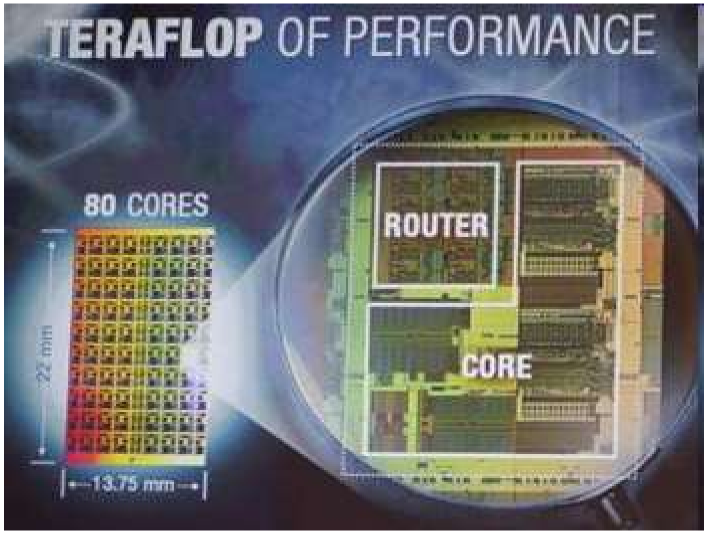



**IBM Cell Processor**
**234M transistors / 2GHz / ??W**
**L=90nm Area=221mm$^2$**

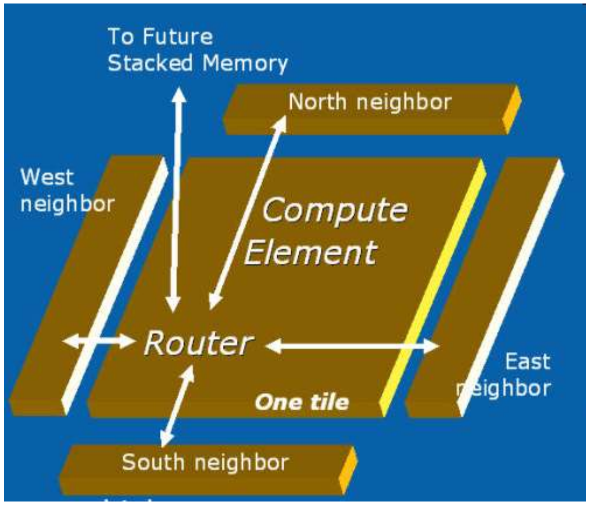
Image courtesy International Business Machines

# Gallery - Current Processors

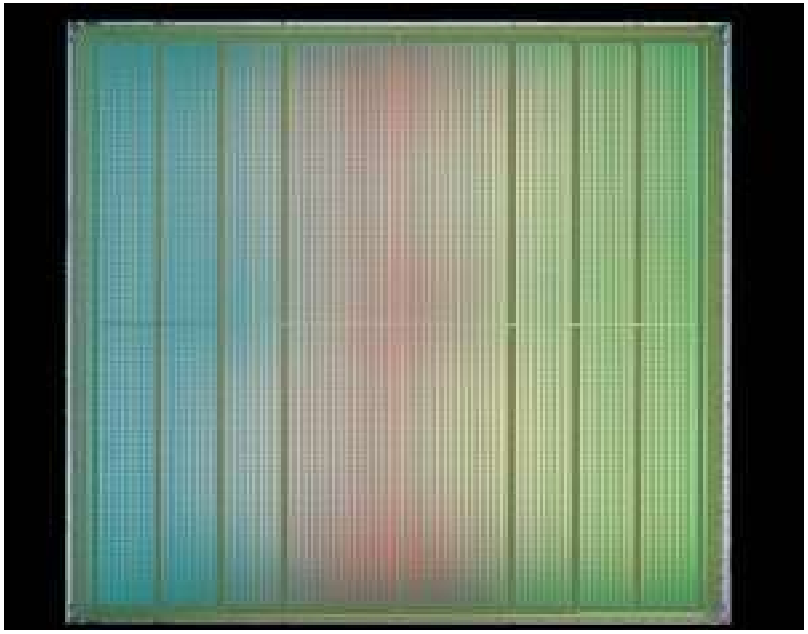
- Intel Polaris (80 cores)
  - Trillion operations/second
  - Area: $275mm^2$
  - Consumption: 62W
  - IEEE SOC Conference (2006)




- Teraflop ASCI Red at Sandia National Lab (1996)
  - 104 cabinets housing 10,000 Pentium Processors
  - spread out over 2500 square feet
  - It consumed a mere 500kw

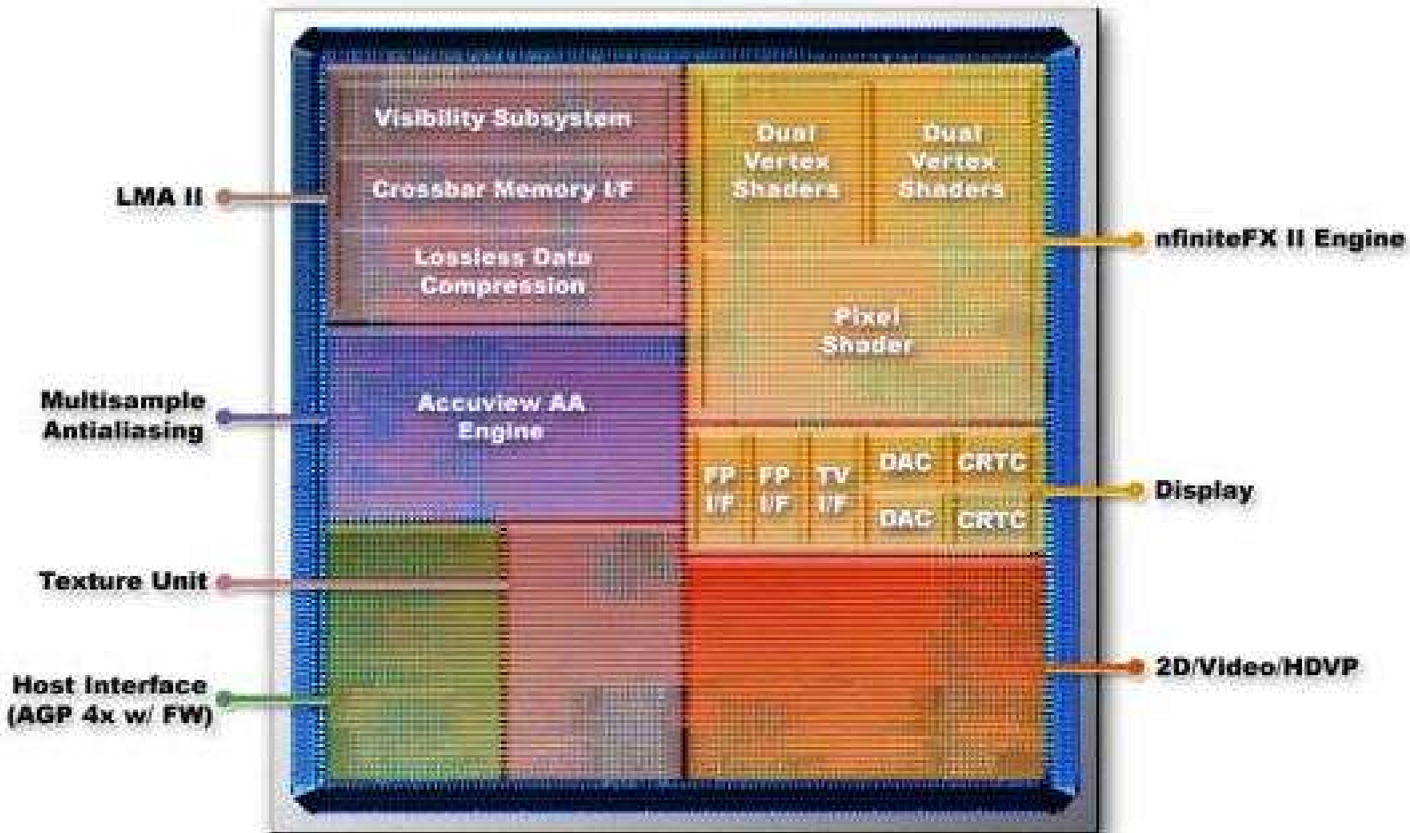


# Gallery - Current FPGA



**Xilinx Virtex FPGA**

# Gallery - Graphics Processor



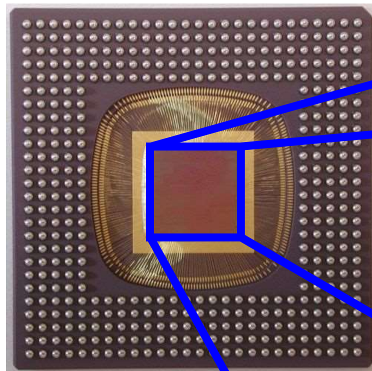

**nVidia GeForce4**

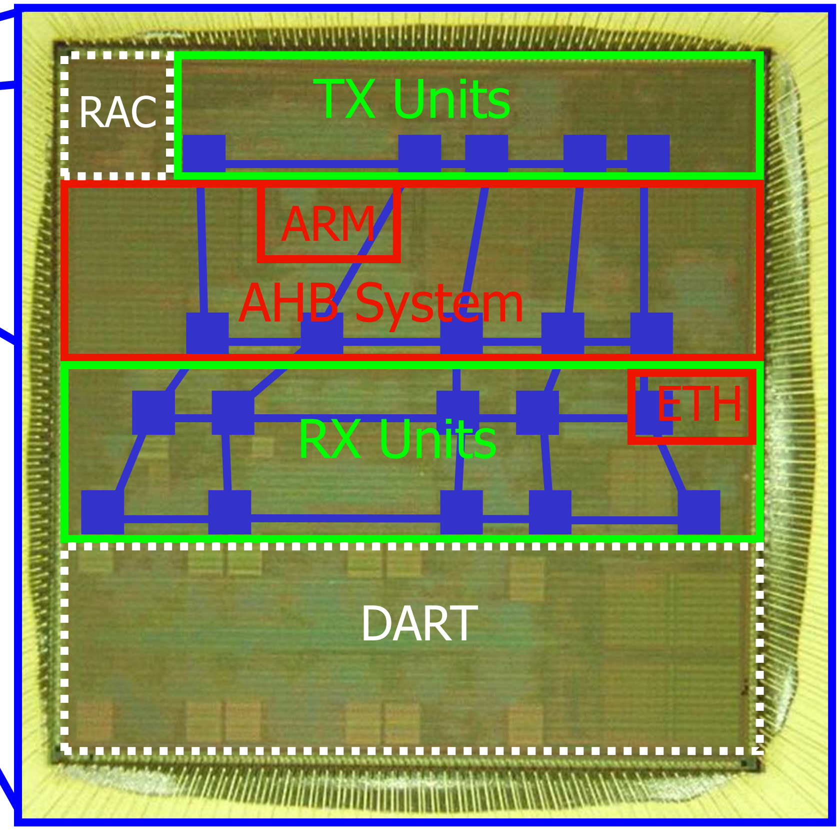
**57M transistors / 300MHz / ??W**

**L=0.15µm**

# FAUST chip

**F**lexible **A**rchitecture of a **U**nified **S**ystem for **T**elecoms





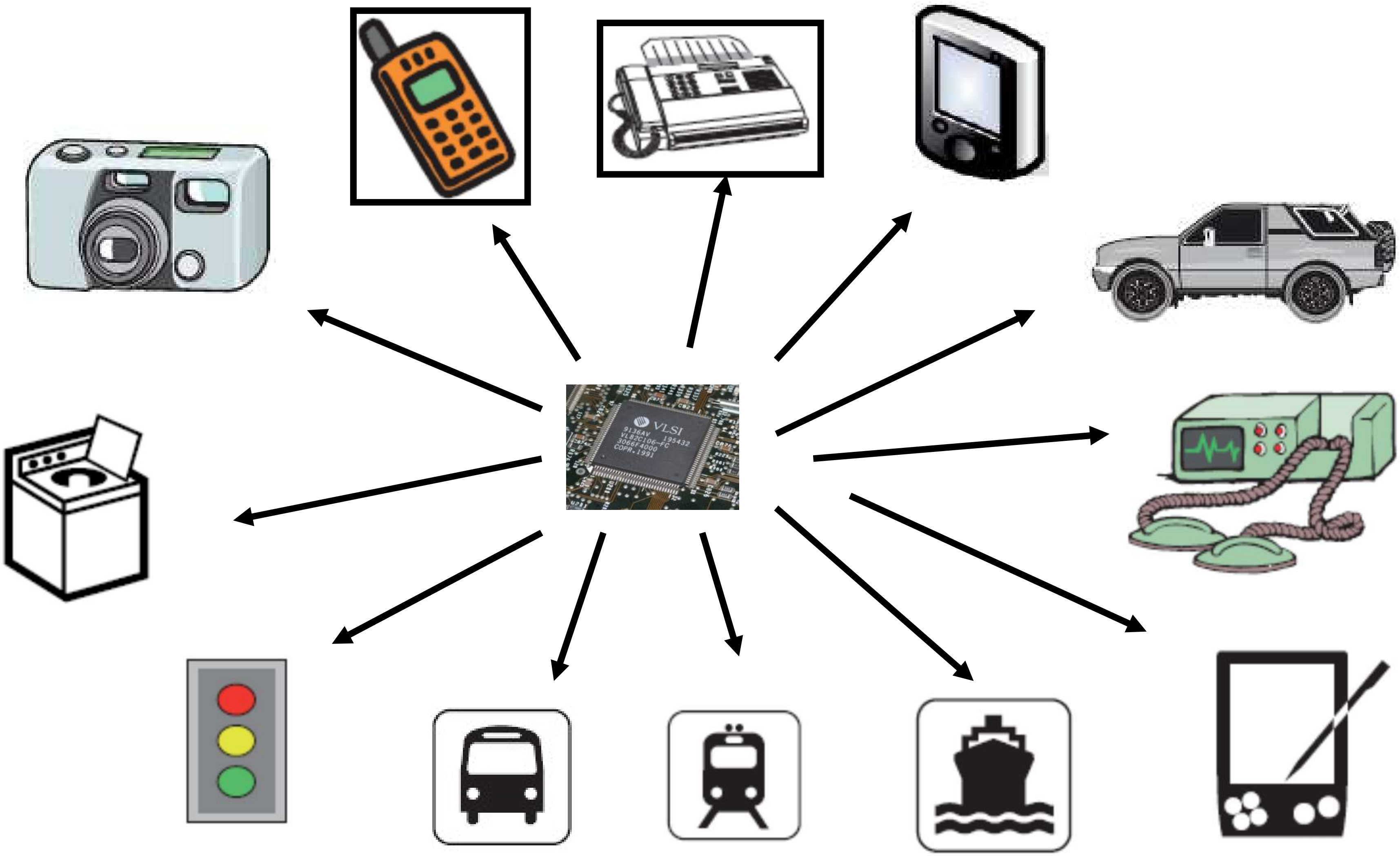

- Year: 2005
- 130 nm CMOS (STMicroelectronics)
- 20-node asynchronous NoC
- 23 NoC units
- **AHB subsystem including an** ARM946 core
- 24 clocks **(DFS to save power)**
- 8 M Gates **(including 81 RAM blocks)**
- Area**: core □ 70 mm2 -** chip □ 80 mm2
- 275 functional I/Os - **Package :** TBGA 420
- **Power supplies:** core □ 1.2 V **– I/Os □ 3.3 V**

D. Lattard, *et al*. – ISSCC'07

# Outline

- Evolution of ICs
- **Applications of ICs**
- What is a digital system
- Classification of Digital ICs
- IC Design Flow and Methodology
- Summary

# Applications of ICs



# Outline

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- **What is a digital system**
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# What is a digital system?

***"A digital system is one that accepts input digital information representing numbers, symbols, or physical quantities, processes this input information in some specific manner, and produces a digital output."***

# What is a digital system?

- Computer applications
  - The computer is required to process information related to physical quantities (such as pressure or temperature).

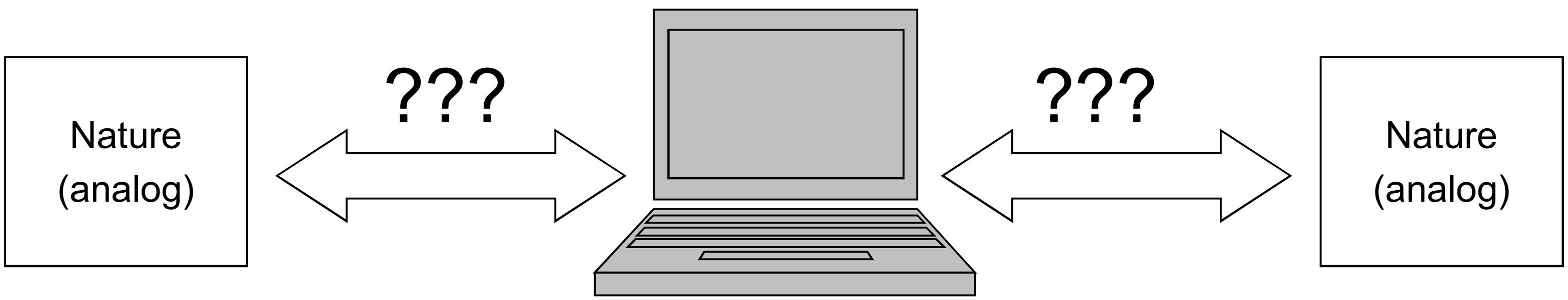
**<u>Computer</u>**

Discrete (*digital*) quantities

**<u>Nature</u>: physical quantities**

Continuous variables (*analog quantities)*

- Physical quantities & computer

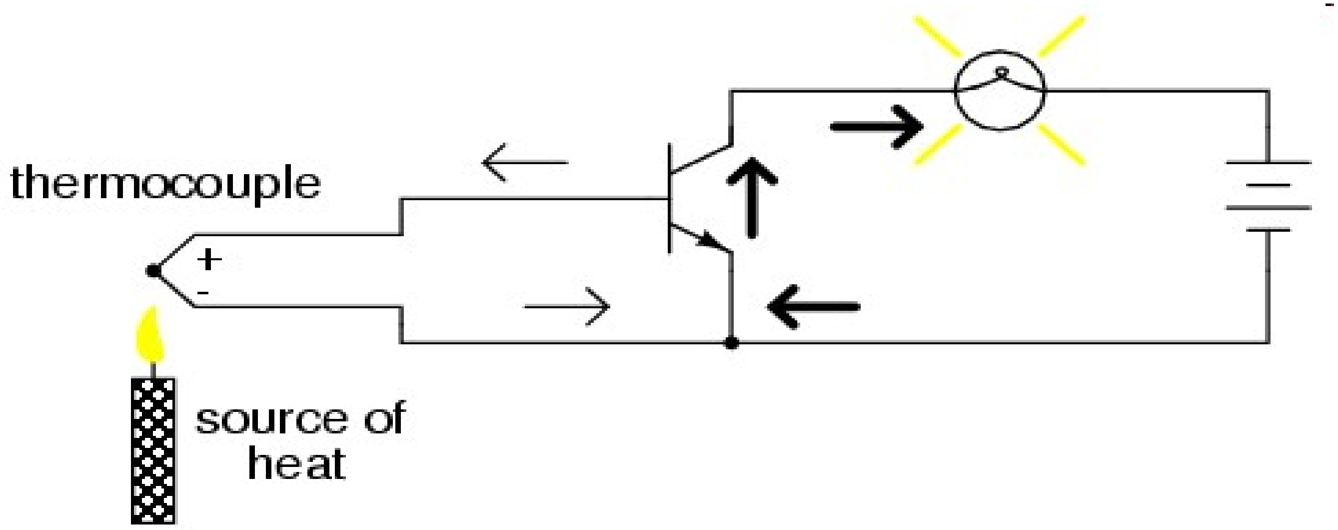



Computer (digital)

**Physical quantities must be converted to a digital form and vice versa !!!**

# What is a digital system?

- Thermocouple in an analog system



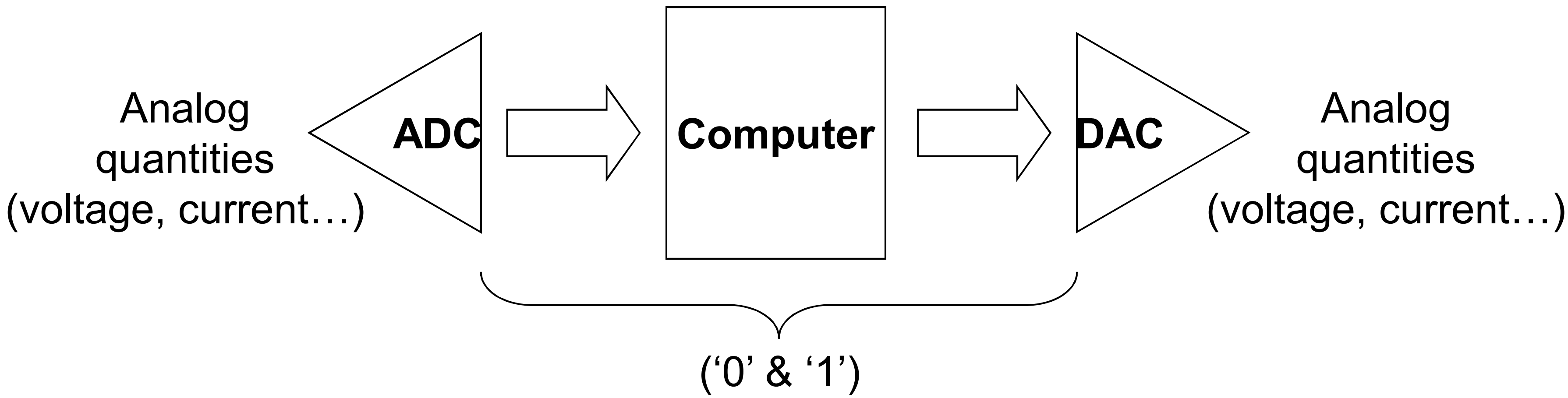

**How does this thermocouple be used in a digital system?**

# What is a digital system?

- Converting a physical quantity to a digital form
  - Physical quantity → voltage/current (by a *transducer*)

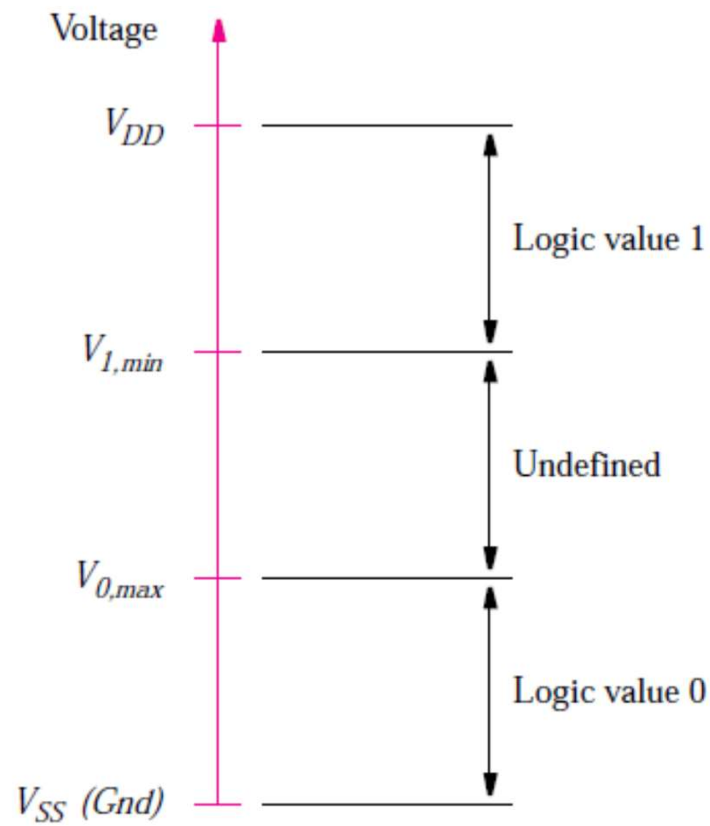
    *(coming energy in one form to going energy in another form)*
    - *Ex.: thermocouple* (temperature transducer)
    - Output voltage is proportional to the temperature

  - Voltage/Current → Digital form (by an *analog-to-digital converter*)



# What is a digital system?

- **How logic variables can be physically represented as signals in electronic circuits?**
  - *Binary variables*:
    - values 0 and 1
    - represented either as levels of voltage or current
  - Representation by voltage levels:
    - Positive logic system
    - Negative logic system




Representation of logic values by voltage levels.

# Why are digital systems so popular?

- **Flexibility**
  - Programmability of processor
- **Reliability**
  - ‘0’ and ‘1’ values is represented by a range of voltage, any minor change in voltage level due to noise or other external events will not cause a 0 to be misinterpreted as a 1, or vice versa.
- **Cost**
  - very low cost

# Outline

- Evolution of VLSI Systems
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# Classification of ICs

- **How large is that circuit?**
  - ✓ **Geometric chip size**
  - ✓ **Transistor count**
  - ✓ **Gate-equivalents**
    - ➢ 1 GE → 1 two-input nand → 4 MOSFETs in static CMOS logic

# Classification of ICs

- **How do functionality and target markets relate to each other?**
  - General-purpose IC Either very simple or of generic functionality

    Examples:
    - Simple: gates, flip-flops, counters, adders, etc.
    - Generic: RAMs, ROMs, microcontrollers, DSPs, etc.
  - Application-specific integrated circuit (ASIC) specified and designed with a particular purpose or processing algorithm
    - Application-specific standard product (ASSP): designed for a specific task and sold to various customers.

      Examples: graphics accelerators, cellular radio chip sets, smart card chips, etc.
    - User-specific integrated circuit (USIC): designed and produced for a single company.

      Examples: Apple A4 SoC introduced with the iPad in 2010; various audio processors for hearing aids.

      Exynos: ARM-based system-on-chips developed by Samsung

# Classification of ICs

- **A IC classification scheme**

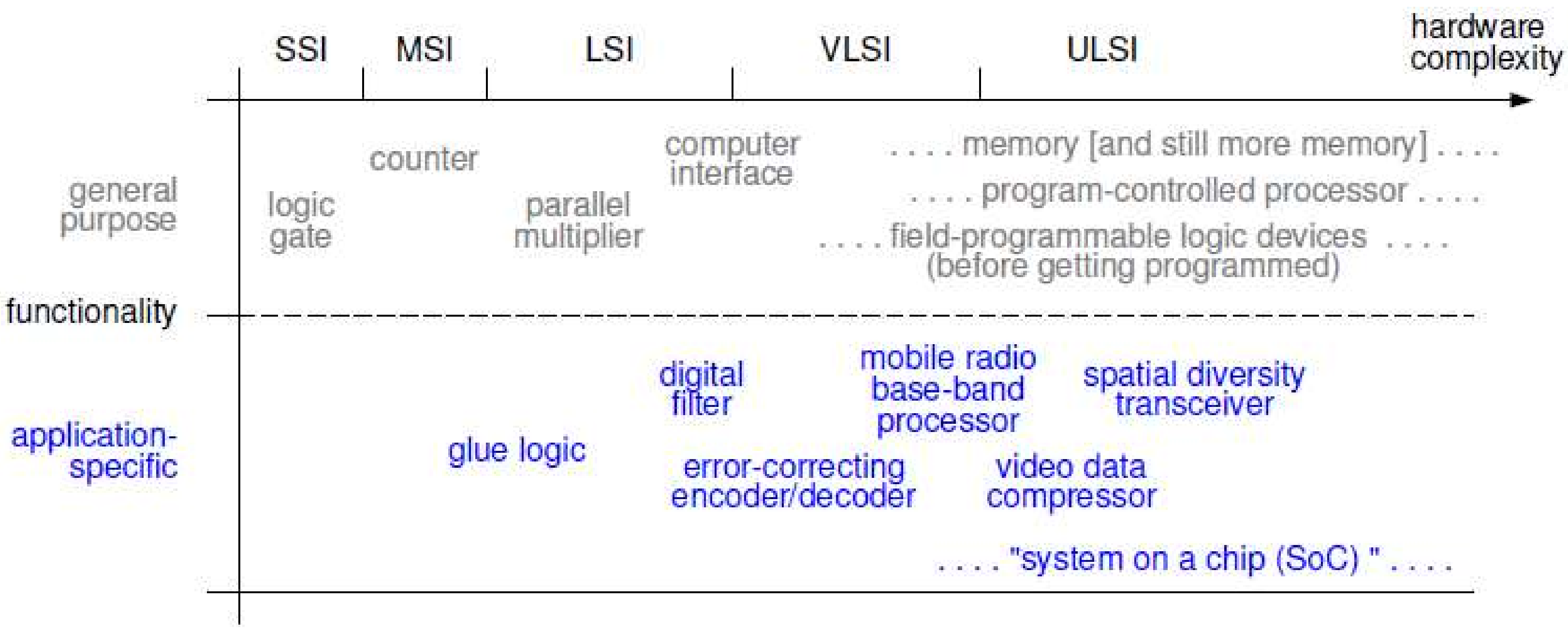



Figure: ICs classified as a function of functionality and hardware complexity.

# Classification of ICs

- **To what extent is a circuit manufactured according to user specifications**

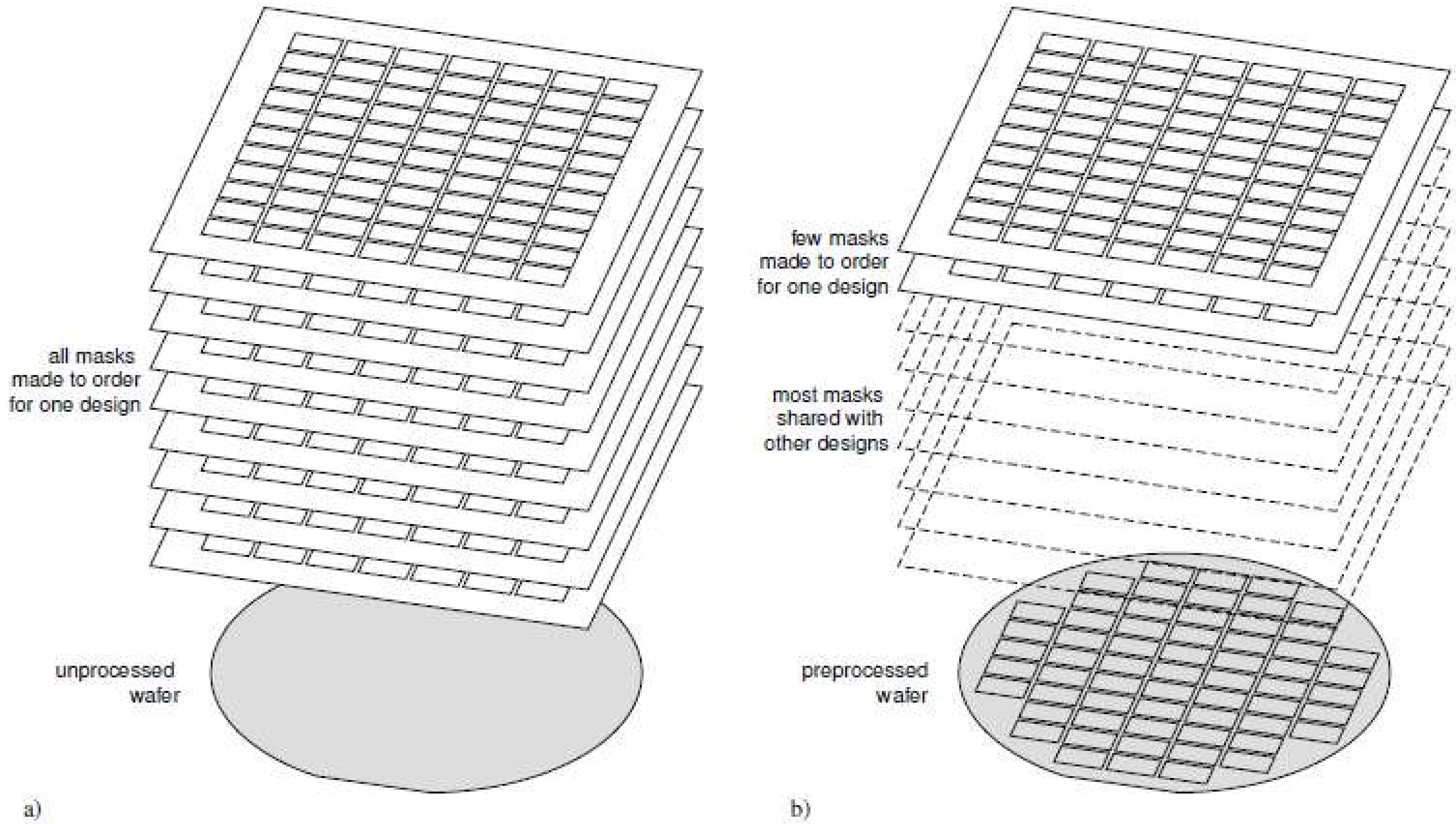



Figure: Full-custom (a) and semi-custom (b) masks sets compared.

# Classification of ICs

- **Semi-custom fabrication I**

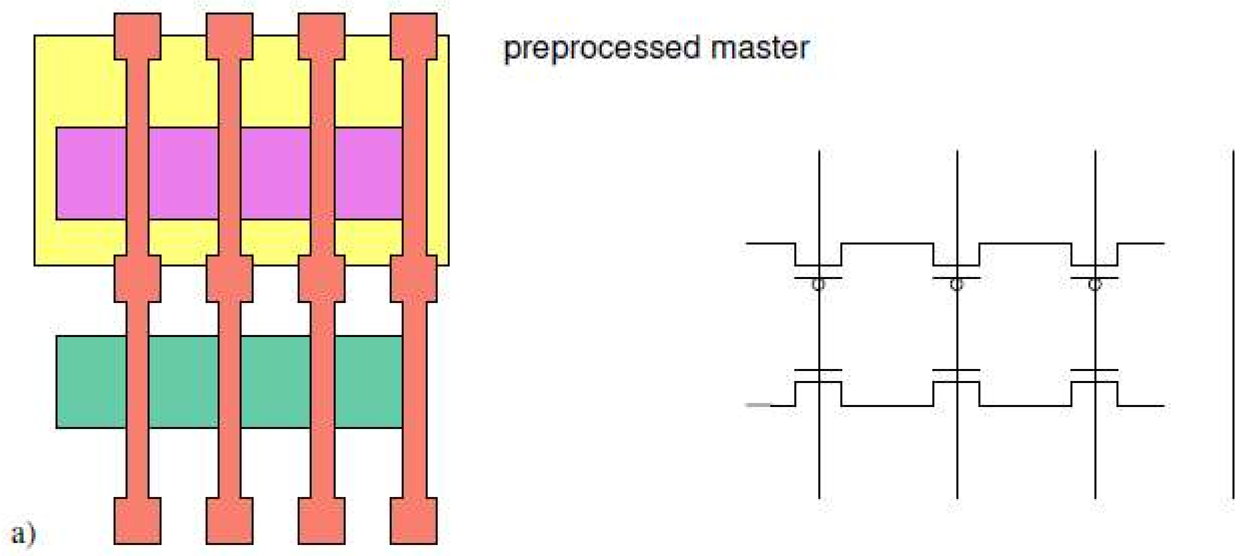



Figure: Gate array site with six prefabricated MOS transistors.

# Classification of ICs

- **Semi-custom fabrication II**

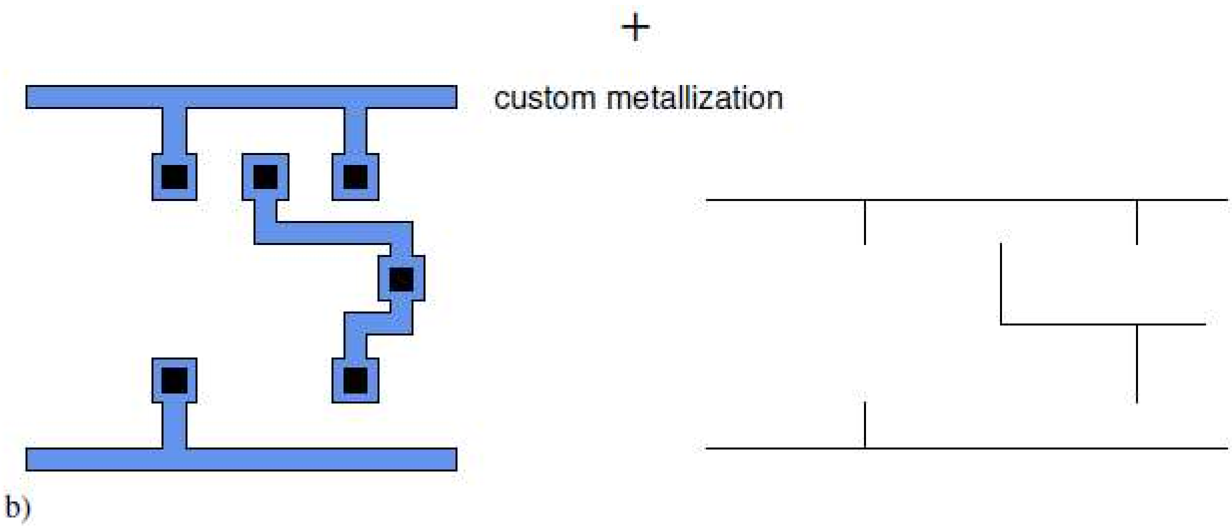



Figure: Custom-designed contact and metal masks.

# Classification of ICs

- **Semi-custom fabrication III**

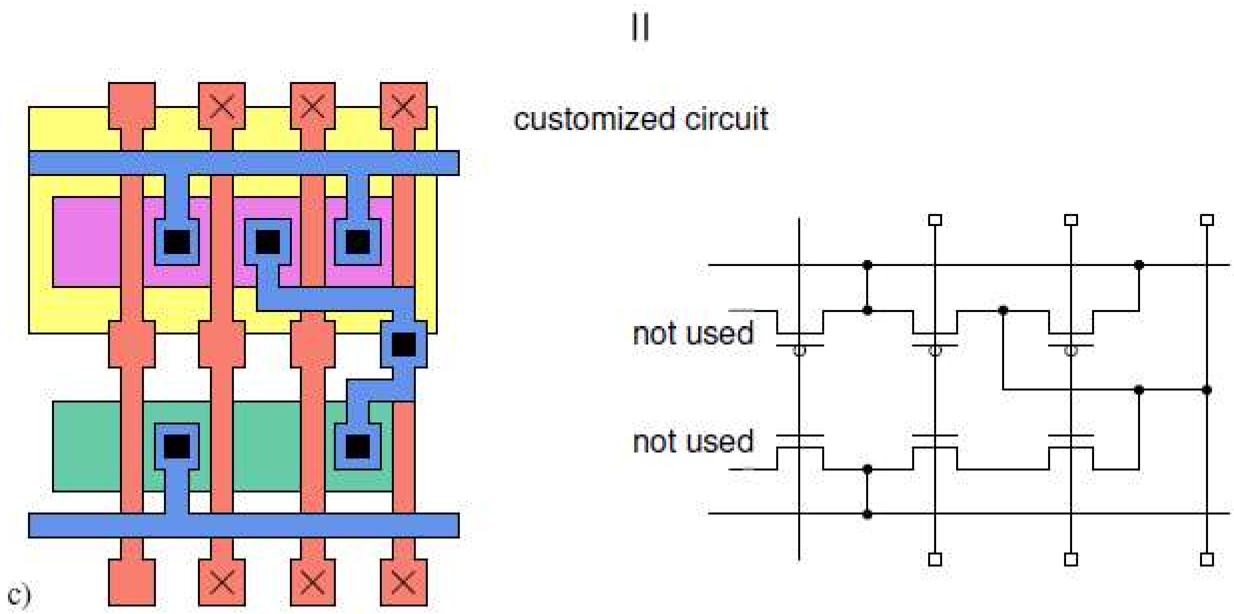



Figure: Site customized into a 2-input NAND gate.

# Classification of ICs

- **Field-programmable logic (FPL)**
  - ✓ Pre-manufactured subcircuits get configured into the target circuit via purely electrical means such as programmable links and look up tables borrowed from memory
  - ✓ The term “programmable" is a misnomer as there is no program, no instruction sequence to execute.
  - ✓ Compared to mask-programmed ICs:
    + Easy and extremely fast to modify.
    + I/O subcircuits, clock and power distribution, embedded memories, testability, etc. come at no extra effort shut in the component.
    – Large overhead in terms of area, delay and energy.

**Observation**

FPL devices can be thought of as “soft hardware”.

# Classification of ICs

- **To what extent is a circuit manufactured according to user specifications**

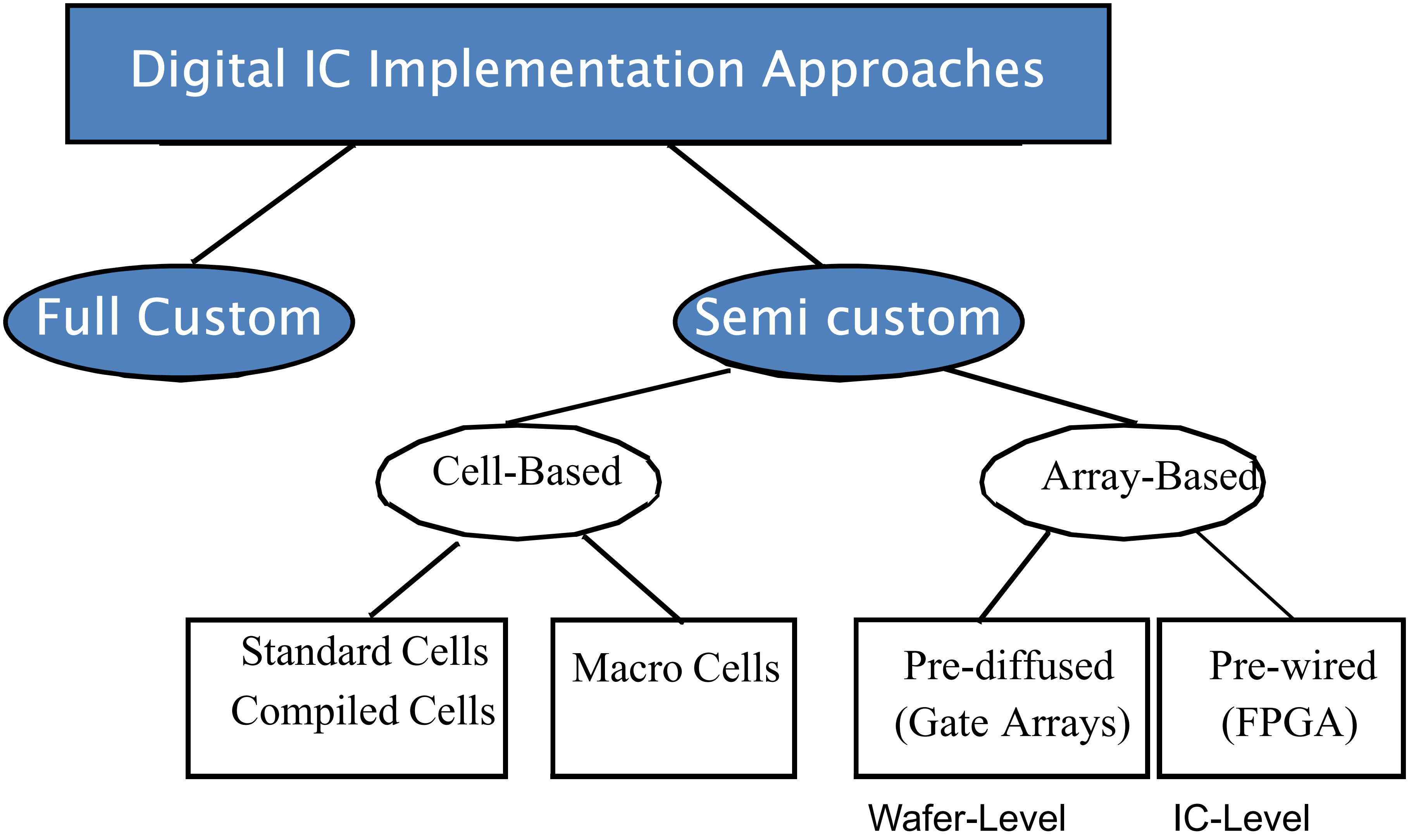
**Full-custom IC** All fabrication layers, full set of photomasks.

**Semi-custom IC** (gate array, sea-of-gates, structured ASIC)
A few metal layers only, subset of photomasks.

**Field-programmable logic** (SPLD, CPLD, FPGA)
Customization occurs electrically, no masks involved.

**Standard part** Catalog part with no customization whatsoever
aka commercial off-the-shelf (COTS) component.

# IC Fabrication/Implementation



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# Design Methodology

- **What?**
  - **A procedure for designing a system by breaking the process into manageable steps.**
- **Why?**
  - **Understanding your methodology helps you ensure you didn’t skip anything.**
  - **Computer-aided design (CAD) tools can be used to:**
    - help automate methodology steps;
    - keep track of the methodology itself.
  - **A design methodology makes it much easier for members of a design team to communicate**

# Levels of Abstraction

High Level

**Specification**
(what the chip does, inputs/outputs)

**Algorithm**
(data and/or signal processing requirements )

**Architecture**
major blocks, connections

**Register-Transfer**
Combinational logic, FSMs, Registers

**Logic**
gates, flip-flops, latches, connections

**Circuit**
transistors, parasitics, connections

**Layout**
mask layers, polygons

Low Level

**Idea is not changing**

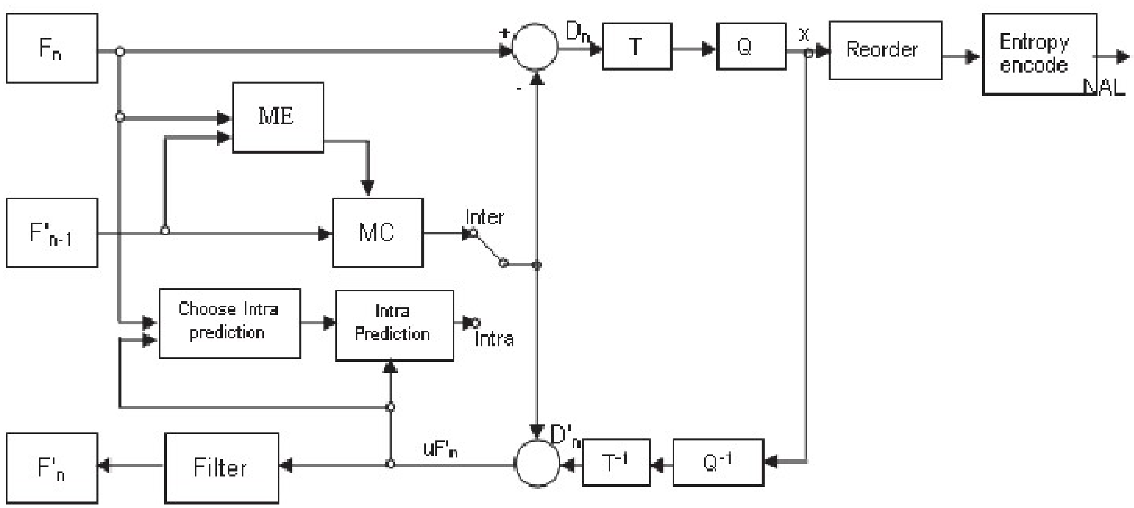
# Levels of Abstraction

- **Specification:** What the IC does, inputs/outputs interface?
  - Goals and constraints of the design.
    For example, H.264 encoder, baseline profile, @CIF30fps
  - Functionality (what will the design do):
  - Performance features like speed and power
  - Fabrication Technology constraints like feature size and area (physical dimensions)
  - Design techniques: parrallel or pipeline; ASIP or ASIC

# Levels of Abstraction

- ***Algorithm proposal:***
  - Defining a series of computations used to meet **data and/or signal processing requirements**
  - Find acceptable compromises between computational complexity and accuracy
  - Decide on number representation schemes, effects of finite word-length computation
  - Quantify the minimum required computational resources (in terms of memory, word widths, arithmetic and logic operations, and their frequencies of occurrence).

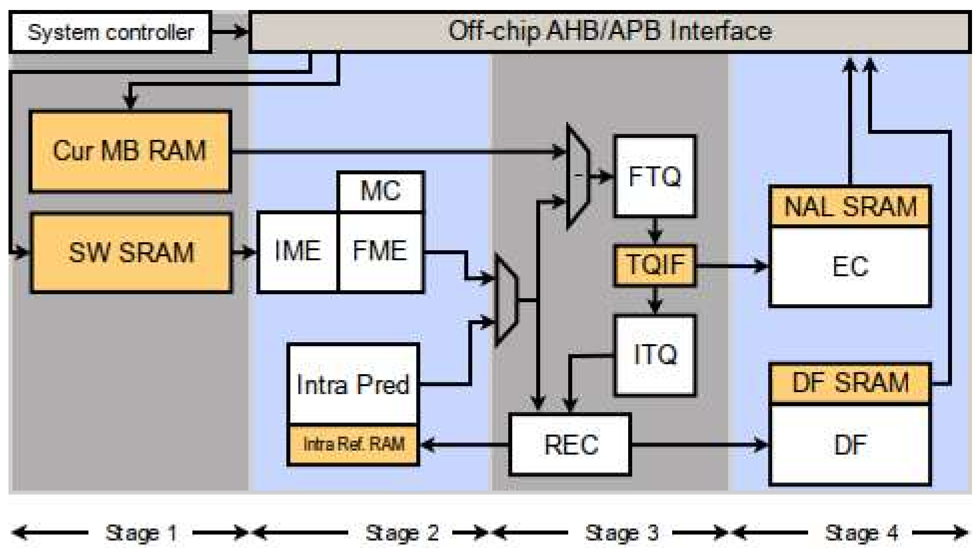
H.264 encoder CDFG
(Control Data Flow Graph)



# Levels of Abstraction

- **System-level Architecture:**
  - Decide what **major functional blocks, connections** used for the design, e.g. dedicated IP, Processor; pipelining stages, parallelism etc …
  - A complex system is broken down into several sub systems.
    - The functionality of these subsystems should match the specifications.
    - The relationship between different sub-systems and with the top level system is also defined

H.264 encoder architecture



# Levels of Abstraction

- **RTL (Register-transfer level) Design:**
  - A design abstraction which models a synchronous digital circuit in terms of the flow of digital signals (data) between hardware registers, and the logical operations performed on those signals by combinational logic
  - Implementing:
    - Finite state machines, Combinatorial and Sequential Logic is expressed usually in Hardware Description Language (e,g. Verilog or VHDL)/Schematics
  - Functional/Logical Verification is performed at this stage to ensure the RTL designed matches the idea.

# Levels of Abstraction

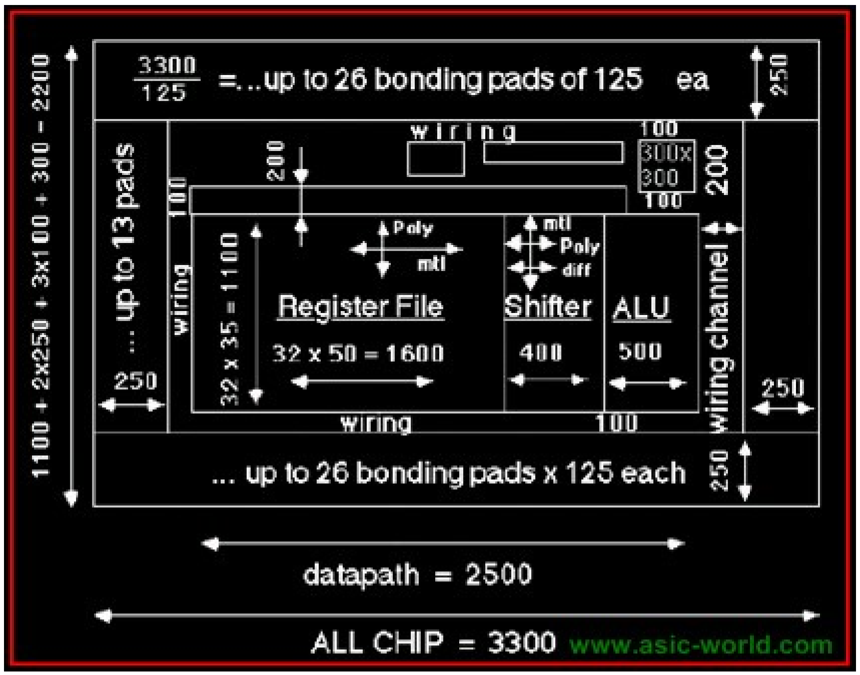
- **Logic design:**
  - Describes how functional units are constructed by only logic functions (NAND, NOR, NOT, …) latches, flip-flop, and connections.
  - For example: various logic design for a 32-bit adder in the x86 integer unit include:
    - ripple carry,
    - Or carry look ahead,
    - Or carry select.

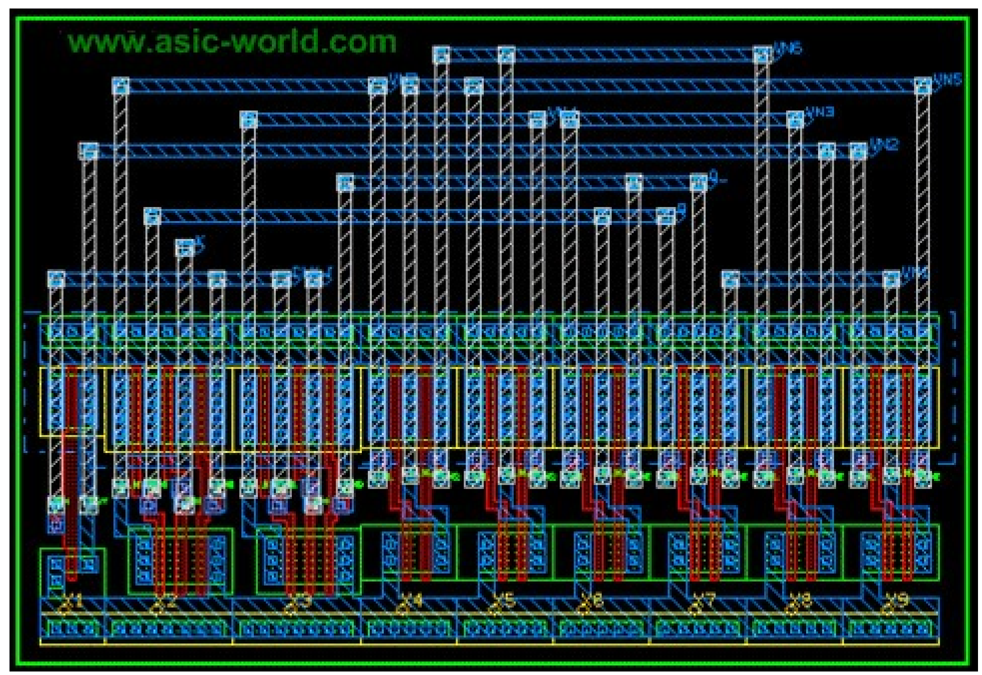
# Levels of Abstraction

- **Circuit design:**
  - Describes how transistors are used to implement the logic circuits.
  - For example, a carry look-ahead adder can use static CMOS circuits, or pass transistors.
  - The circuits can be tailored to emphasize high performance or low power.

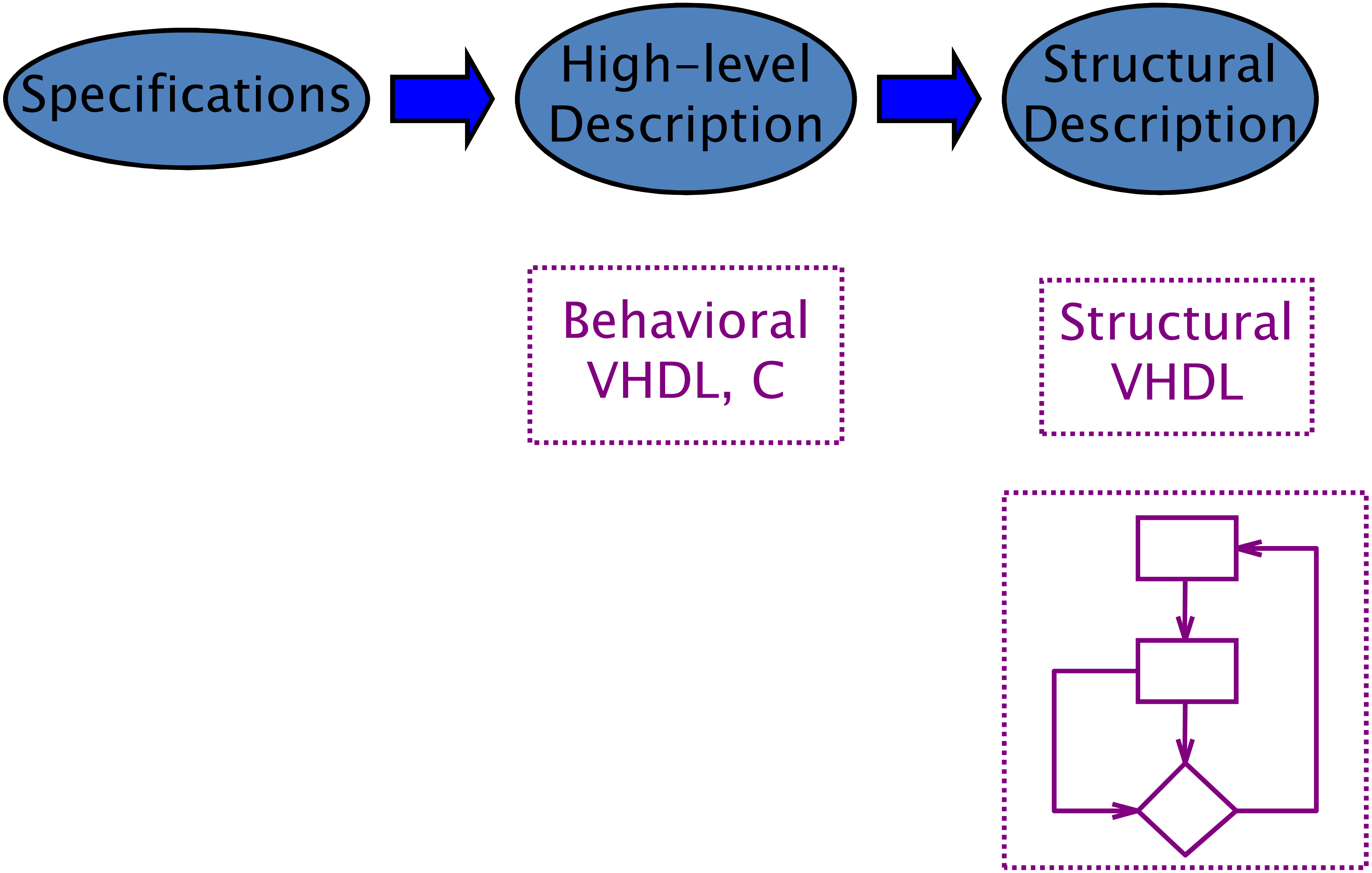
# Levels of Abstraction

- **Physical design:**
  - Describes the layout of the chip with cell libraries.

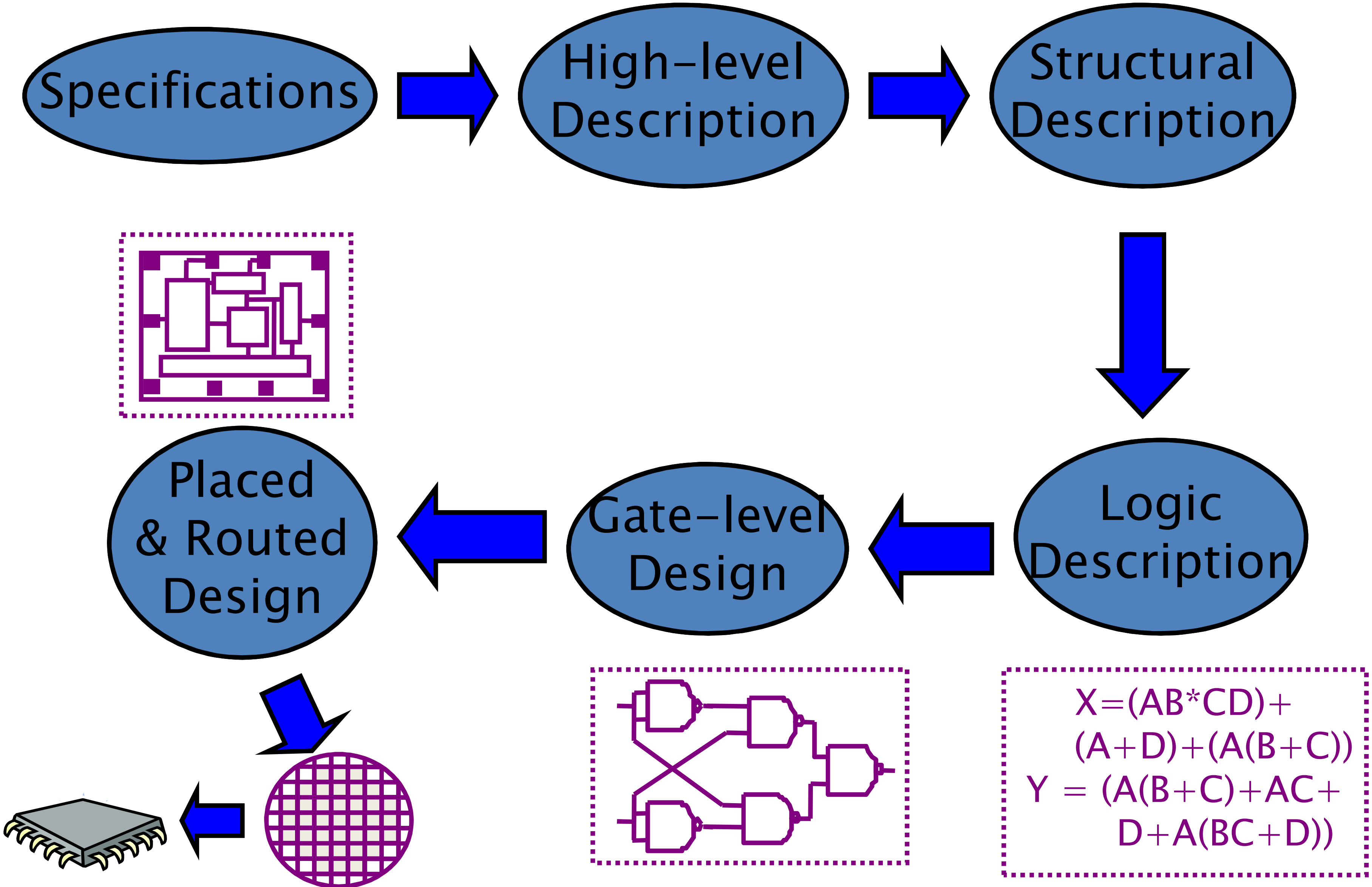


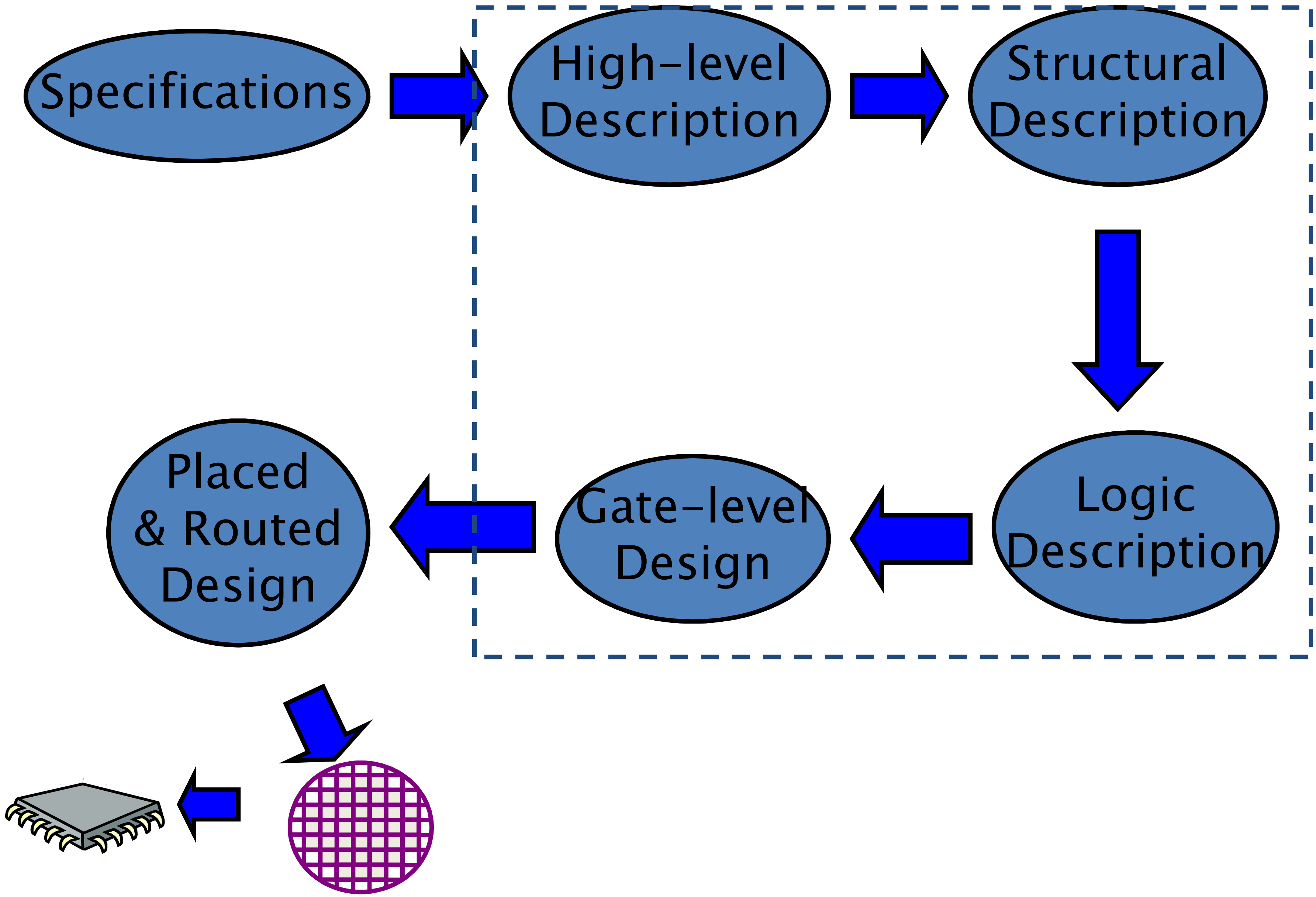
# Levels of Abstraction in IC Design Flow



# Levels of Abstraction in IC Design Flow



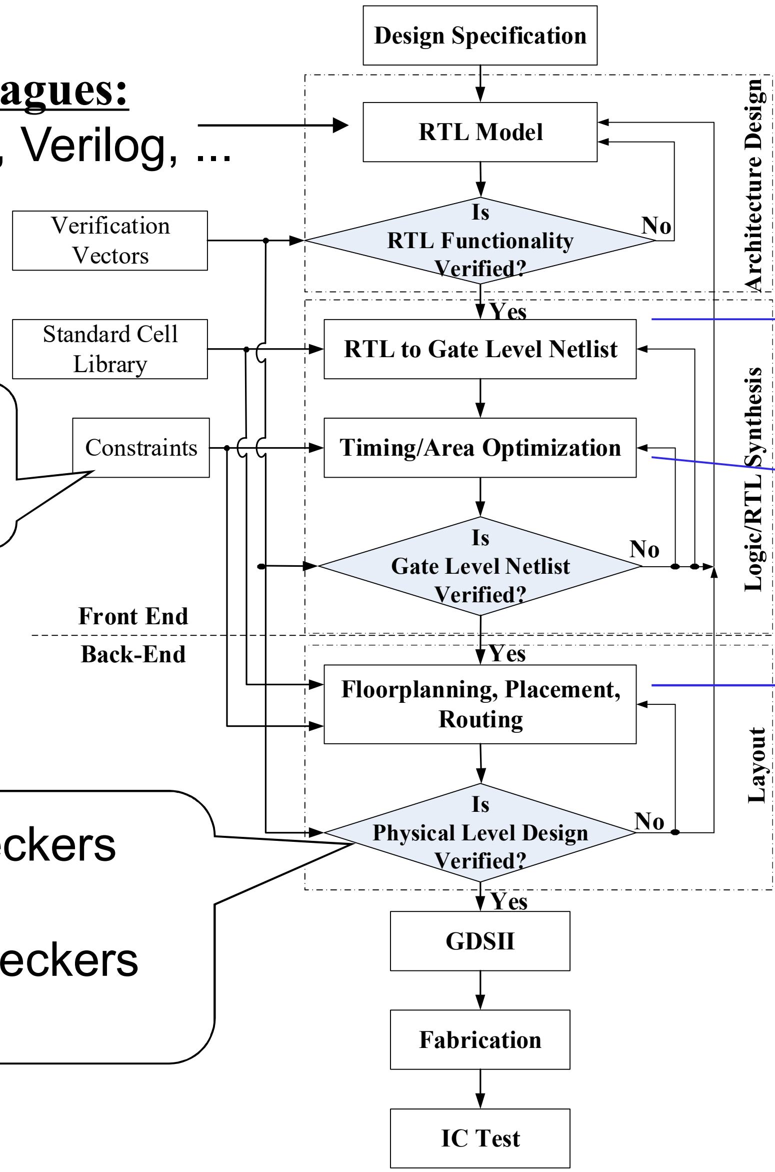
# Levels of Abstraction in IC Design Flow



# IC Design Flow

**Languages:**
VHDL, Verilog, …

Timing, Area, Power, etc.




Design rule checkers (DRC),
Electrical rule checkers (ERC)

**Tools:**
Design Compiler (Synopsys),
RTL Compiler (Cadence)

**Tools:**
Primetime (Synopsys)

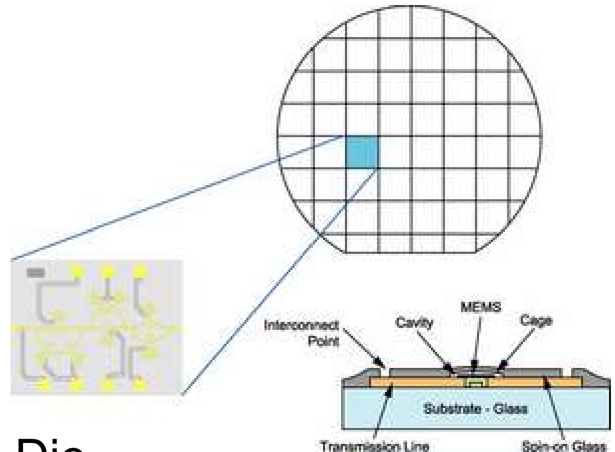
**Tools:**
IC Compiler (Synopsys),
Encouter (Cadence),

# IC Design Flow

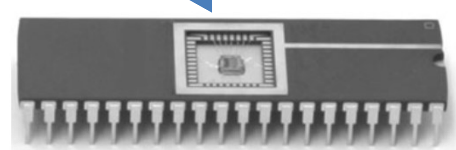
## Fabrication

GDSII

Wafer

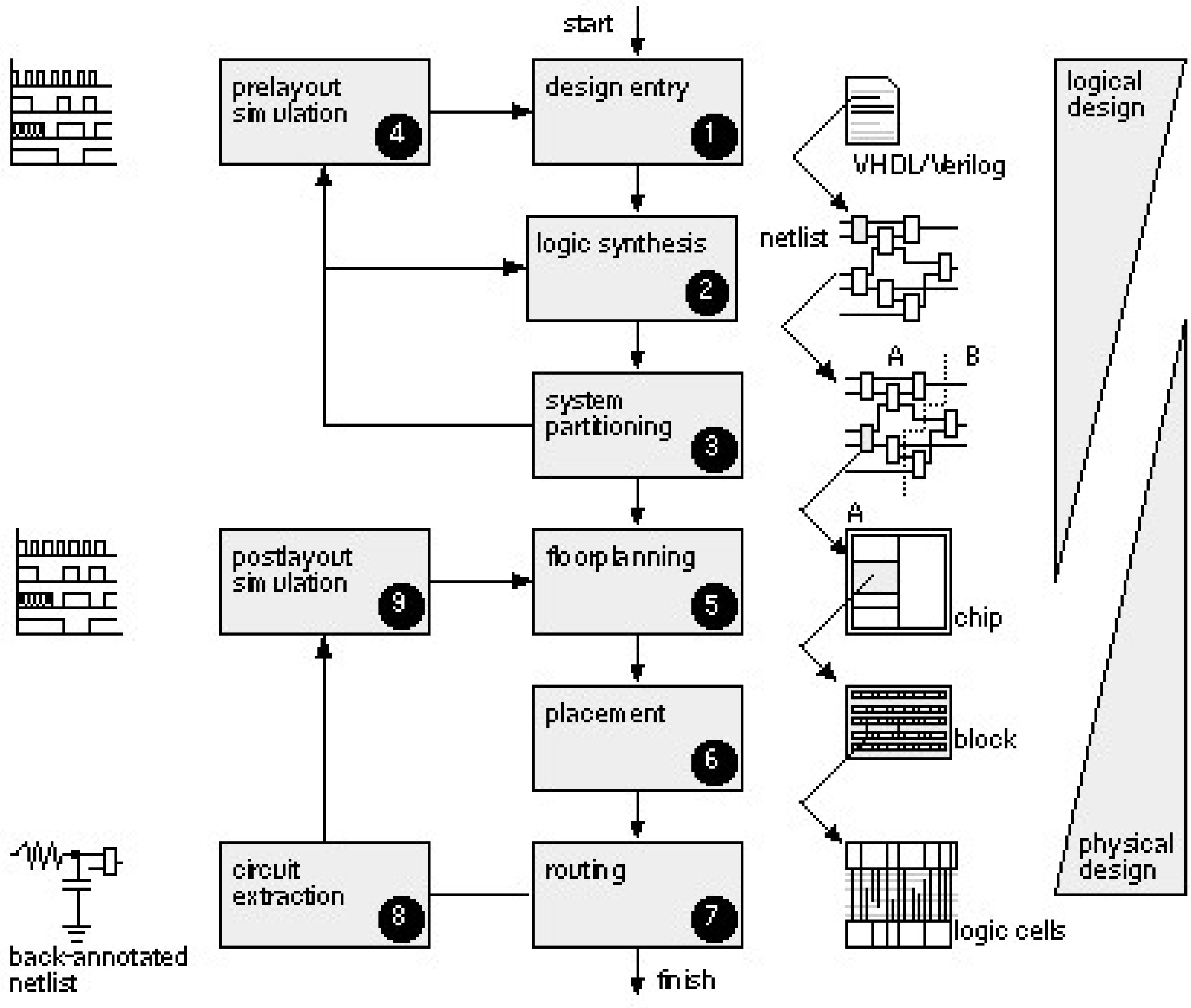



Die



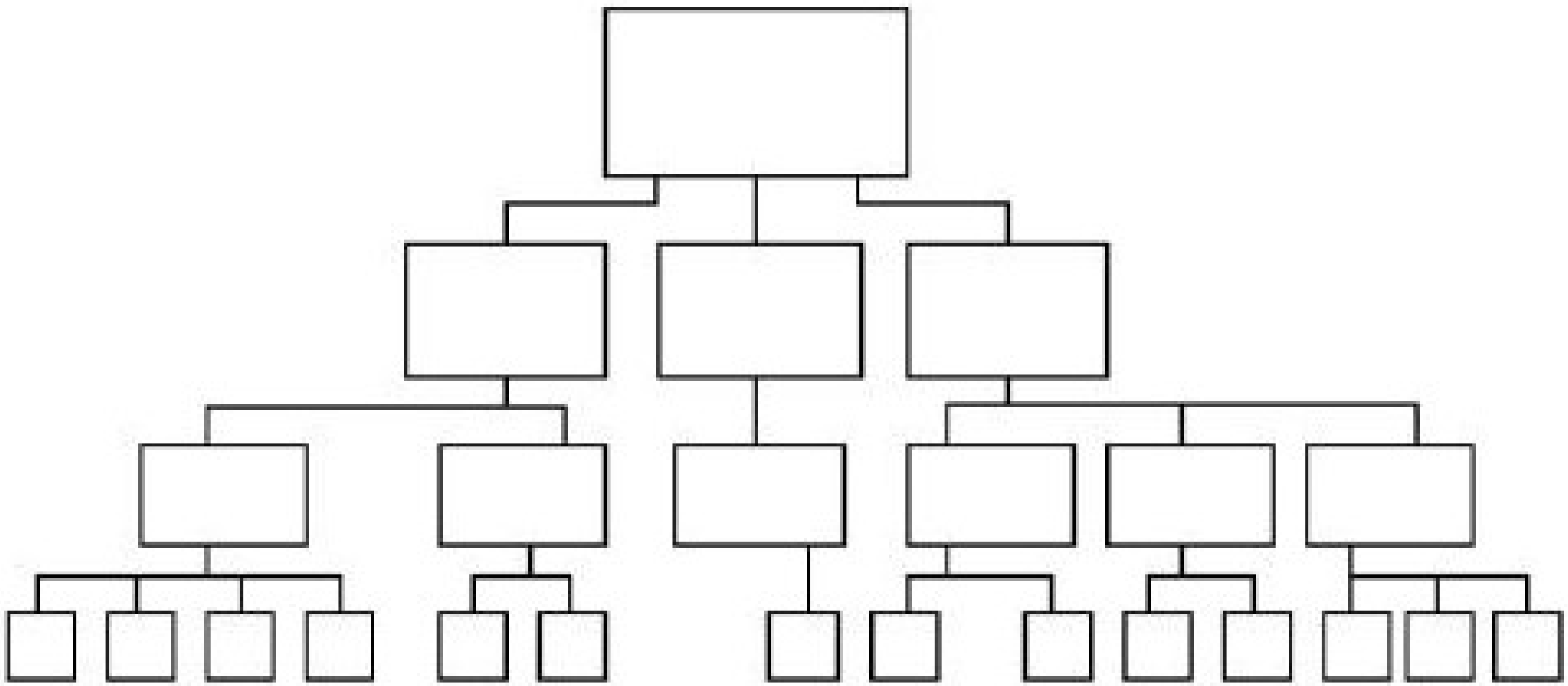
IC Package

# VLSI/ASIC design flow



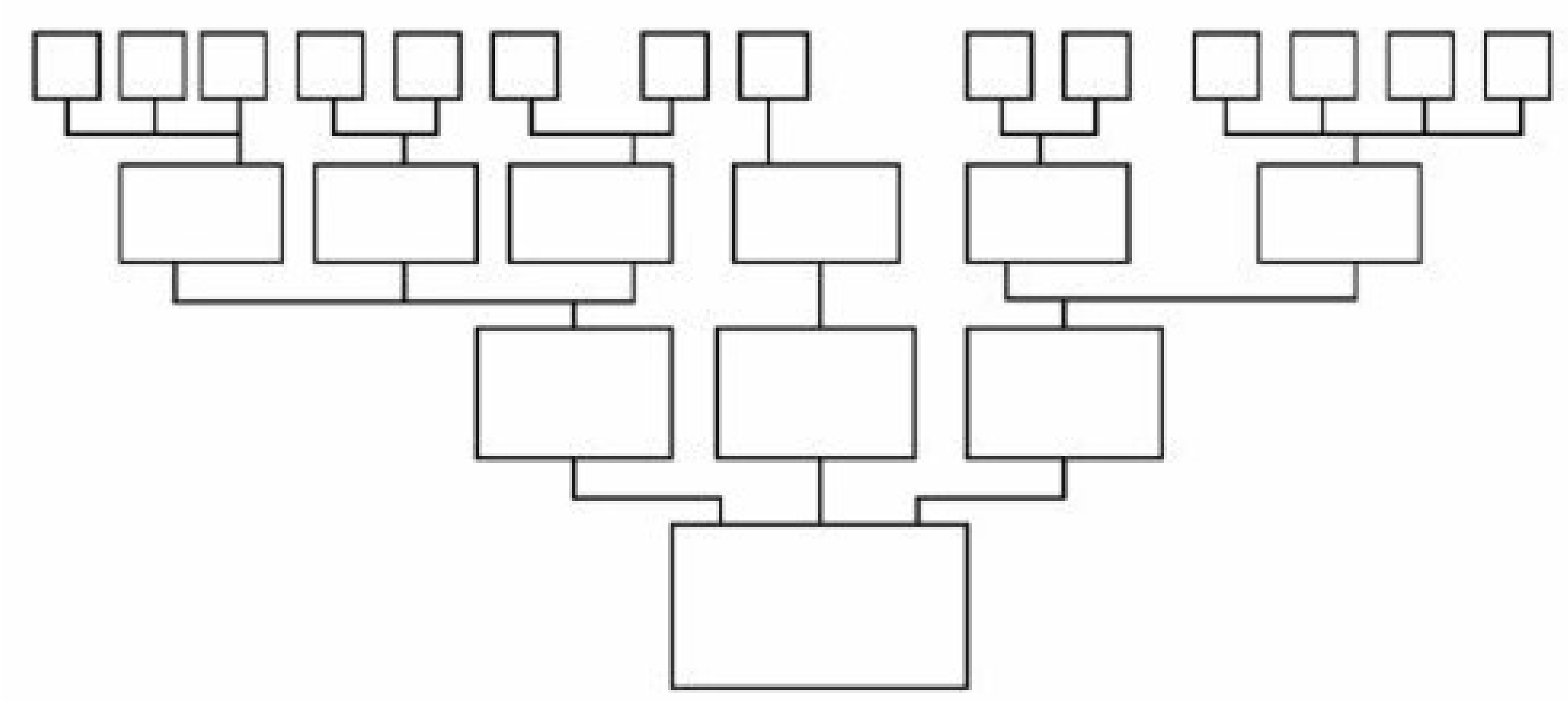
# Implementation Methods

- Top-Down Design Method
  - High level functions are defined first
  - Lower level implementation details are filled in later



# Implementation Methods

- Bottom-Up Design Method
  - Low level functions are defined and finished first
  - High level implementation are completed in later



# Implementation Methods

| Designer | Tasks | Tools |
| --- | --- | --- |
| Architect Designer | Define Overall Chip<br>C++/SystemC Model<br>Initial Floorplan | Text Editor<br>C Compiler |
| Logic Designer | RTL Model<br>Behavioral Simulation<br>Logic Simulation<br>Synthesis<br>Datapath schematics | RTL Simulator<br>Synthesis Tools<br>Timing Analyzer<br>Power Estimator |
| Circuit Designer | Cell Libraries<br>Circuit Schematics<br>Circuit Simulation<br>Megacell Blocks | Schematic Editor<br>Circuit Simulator<br>Router |
| Physical Designer | Layout and Floorplan<br>Place and Route<br>Parasitics Extraction<br>DRC/LVS/ERC | Place/Route Tools<br>Physical Design and Evaluation Tools |

# VLSI Design Tradeoffs

- **Non-Recurring Engineering (NRE) Costs**
  - Design Costs
  - Mask “Tooling” costs
- **Unit Cost - related to chip size**
  - Amount of logic
  - Current technology
- **Performance**
  - Clock speed
  - Implementation
- **Power consumption**
  - Power supply voltage
  - Clock speed
- **Time to Market**

# Outline

- Evolution of ICs
- Applications of ICs
- What is a digital system
- Classification of ICs
- IC Design Flow and Methodology
- **Summary**

# Summary

- Concepts and applications of ICs
- IC Design Flow and Methodology
  - Abstraction Levels
  - IC Design flow
  - Implementation Method