VietNam National University
University of Engineering and Technology

CMOS TECHNOLOGY FOR VLSI IMPLEMENTATION

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Laboratory for Smart Integrated Systems

Objectives

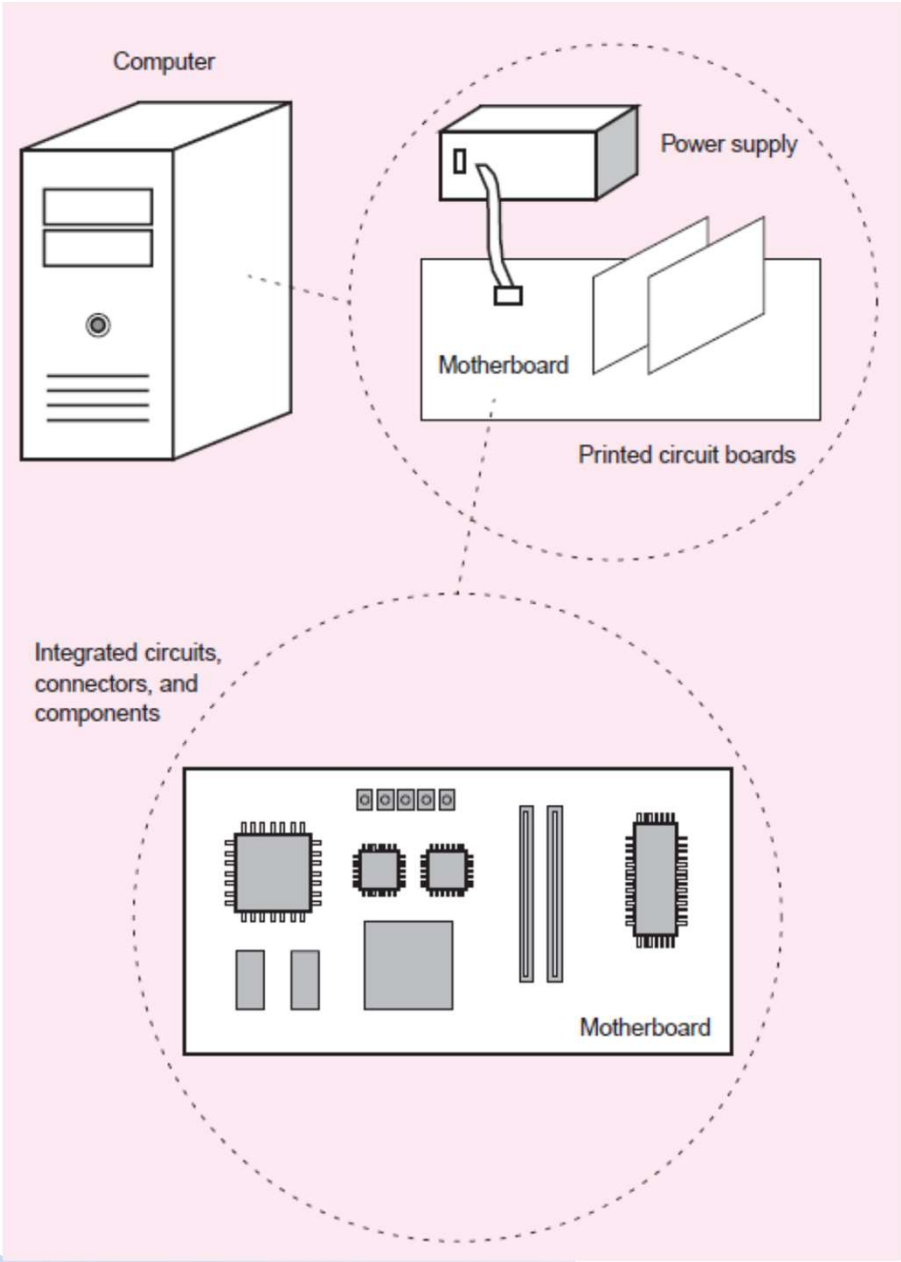
- **In this lecture you will be introduced to:**
  - How transistors operate and form simple switches
  - CMOS logic gates
  - Basic characteristics of electronic circuits
  - CMOS Fabrication

Outline

- **MOS Transistors**
- NMOS vs. CMOS Logic Circuits
- MOS Logic Circuits
- CMOS Fabrication and Layout
- Summary

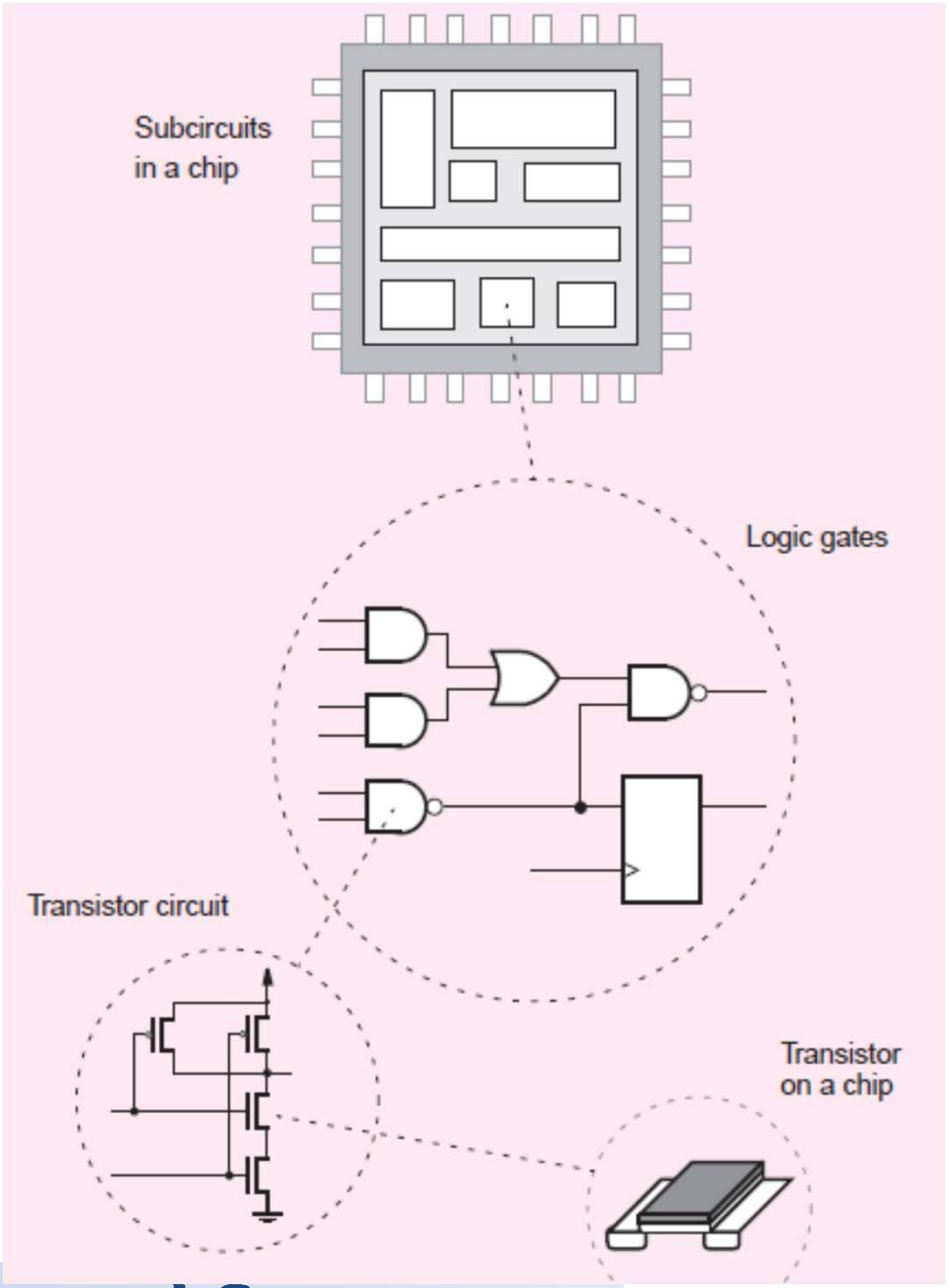
Review: Digital System Example

- **Structure of Computer**
  - Motherboard
  - Power Supply
  - Slots & daughter boards
  - ICs (Integrated Circuits)



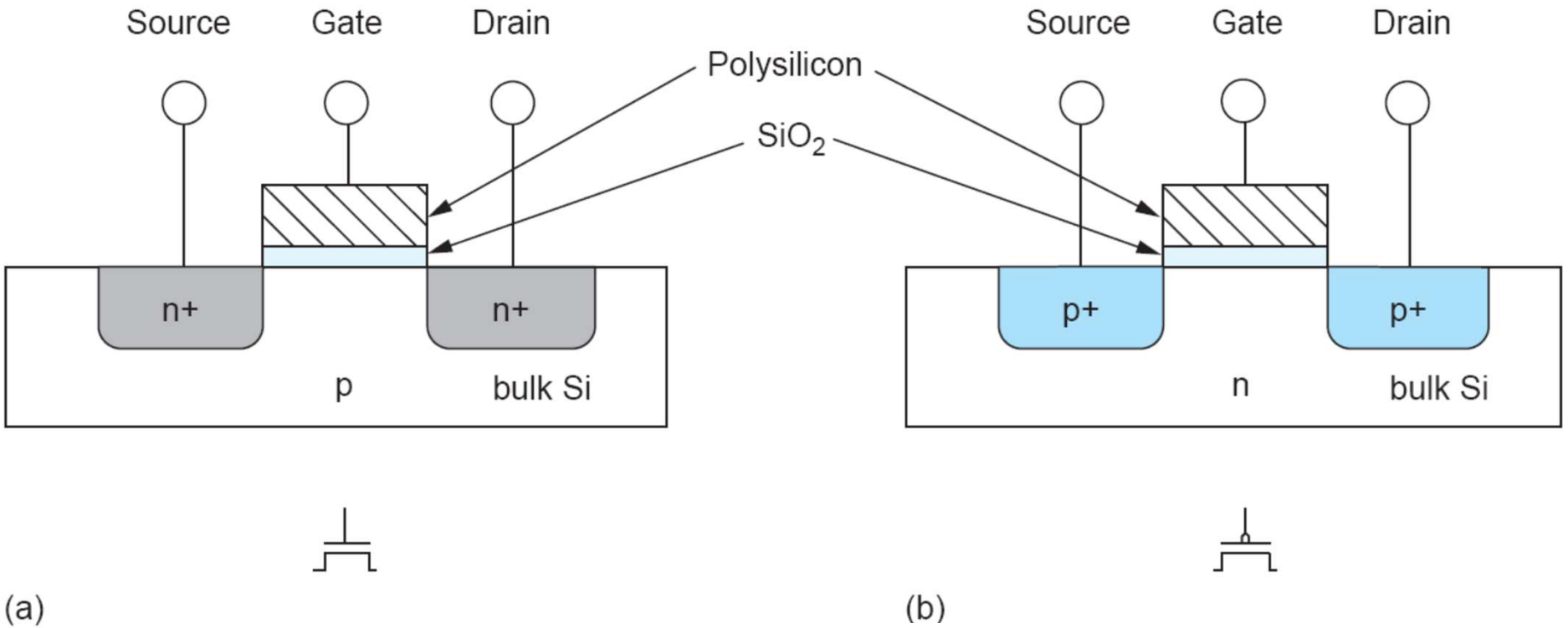
Review: Digital System Example

- Structure of a IC
  - Include several Sub-circuits
    - arithmetic operations, store data, or control the flow of data
  - Logic circuit comprises a network of connected *logic gates*
    - logic gate performs a very simple function
    - Logic gates are built with transistors
    - Transistors are implemented by fabricating various layers of material on a silicon chip



MOS TRANSISTOR

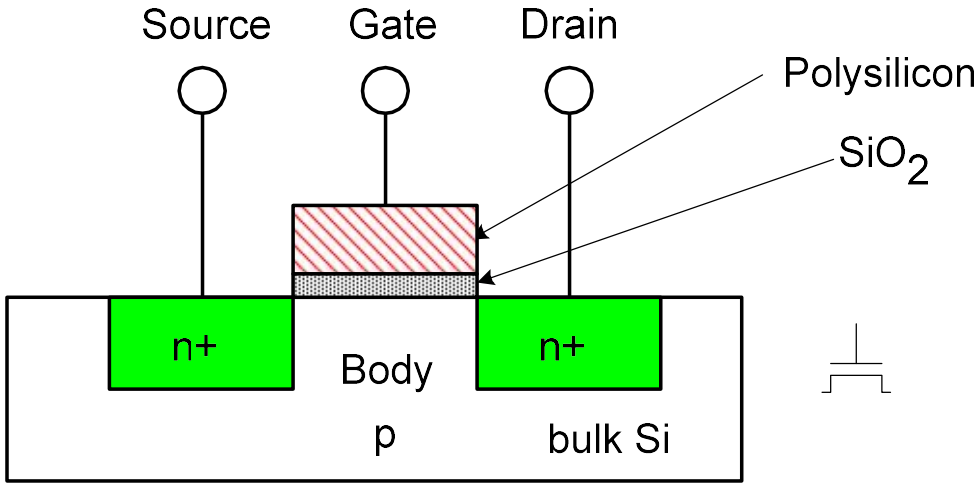
- **A Metal-Oxide-Semiconductor (*MOS*) structure**
  - superimposing several layers of conducting and insulating materials
  - chemical processing steps: oxidation of the silicon, selective introduction of dopants, and deposition and etching of metal wires and contacts



nMOS transistor (a) and pMOS transistor (b)

nMOS TRANSISTOR

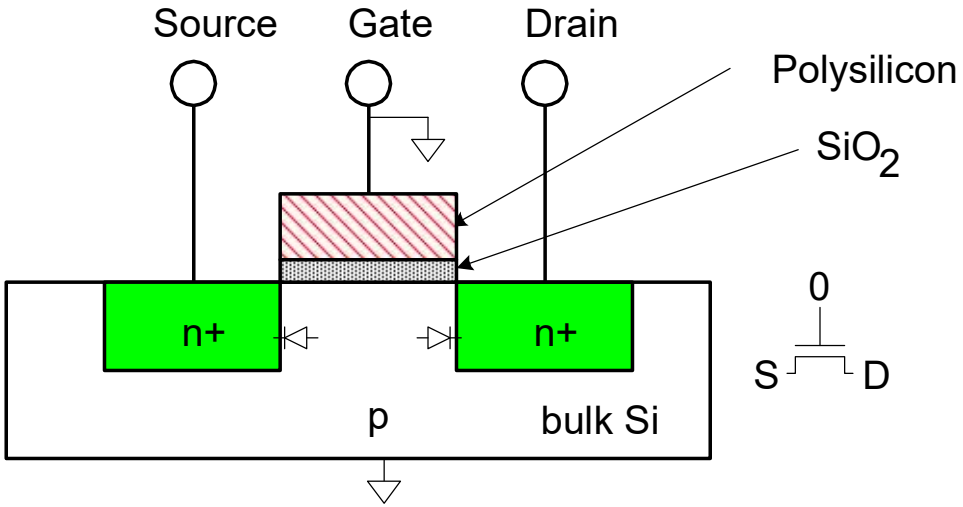
- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - SiO_2 (oxide) is a very good insulator
  - Called metal – oxide – semiconductor (MOS) capacitor
  - Even though gate is no longer made of metal*



* Metal gates are returning today!

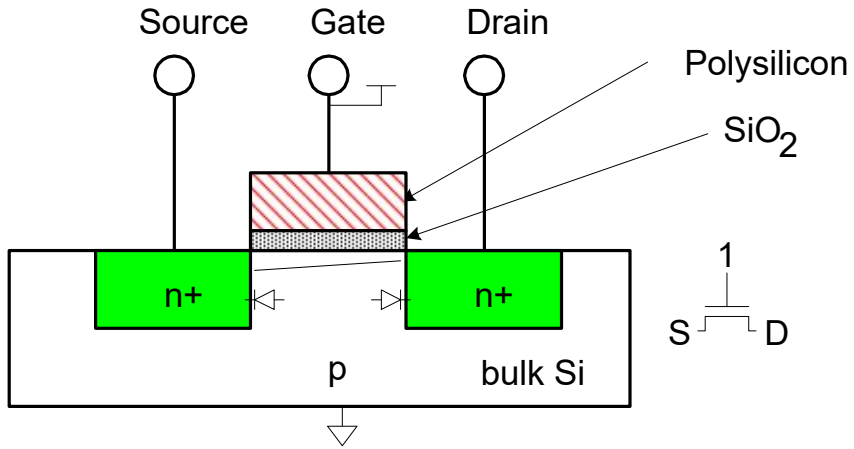
nMOS TRANSISTOR

- Body is usually tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



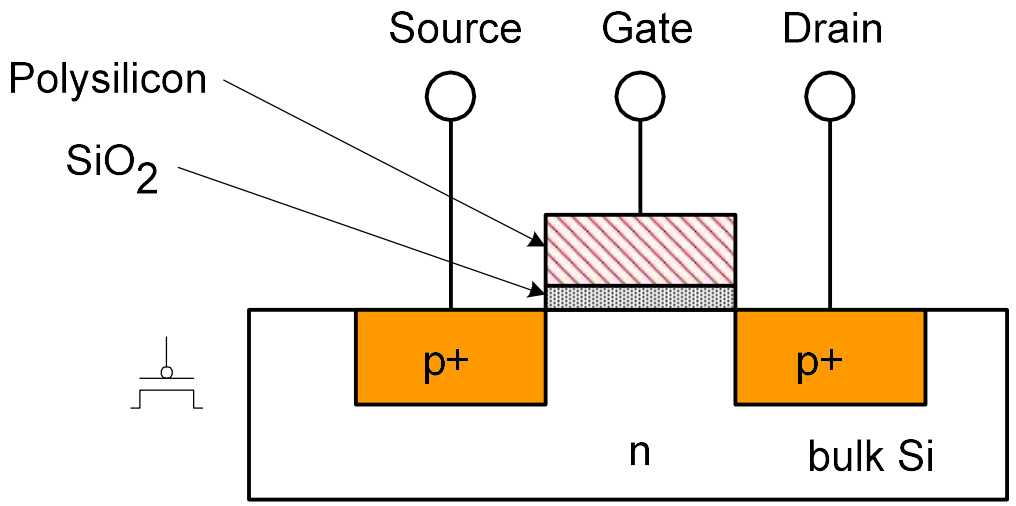
nMOS TRANSISTOR

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



pMOS TRANSISTOR

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior

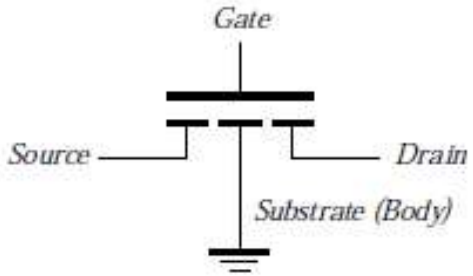


Power Supply Voltage

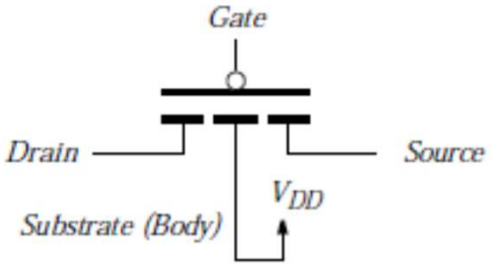
- GND = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, …

MOS TRANSISTOR

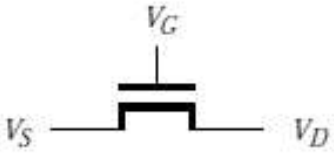
- **Transistor symbols and Switch-level models**



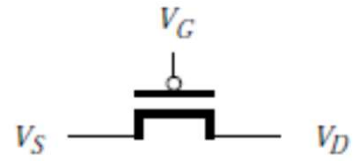
(b) NMOS transistor



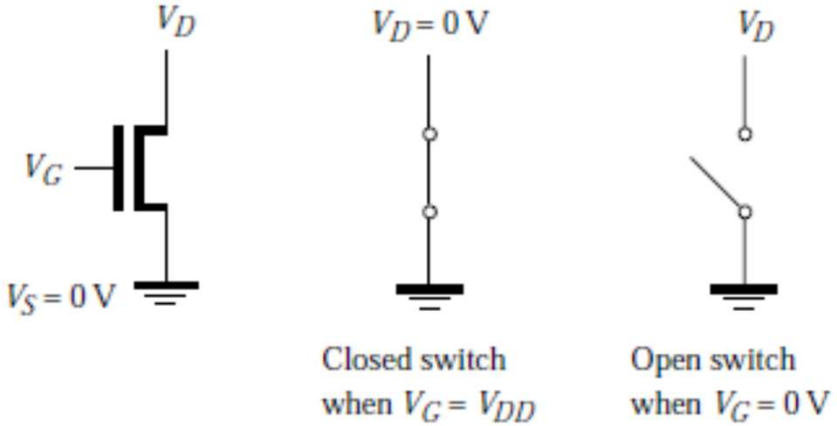
(b) PMOS transistor

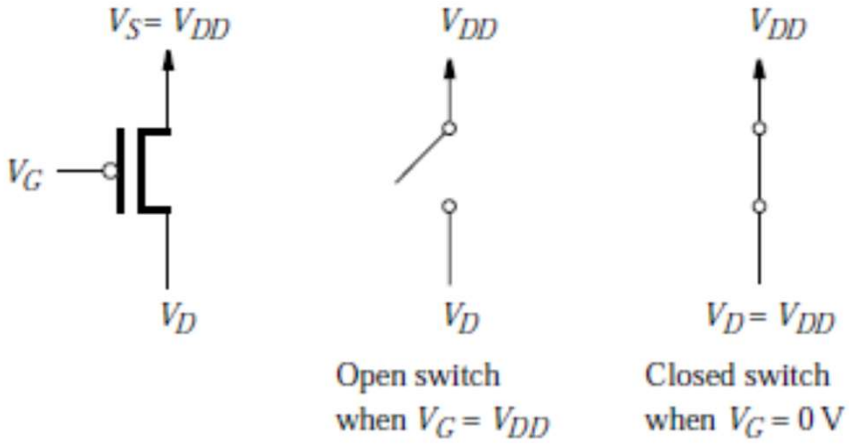


(c) Simplified symbol for an NMOS transistor



(c) Simplified symbol for an PMOS transistor



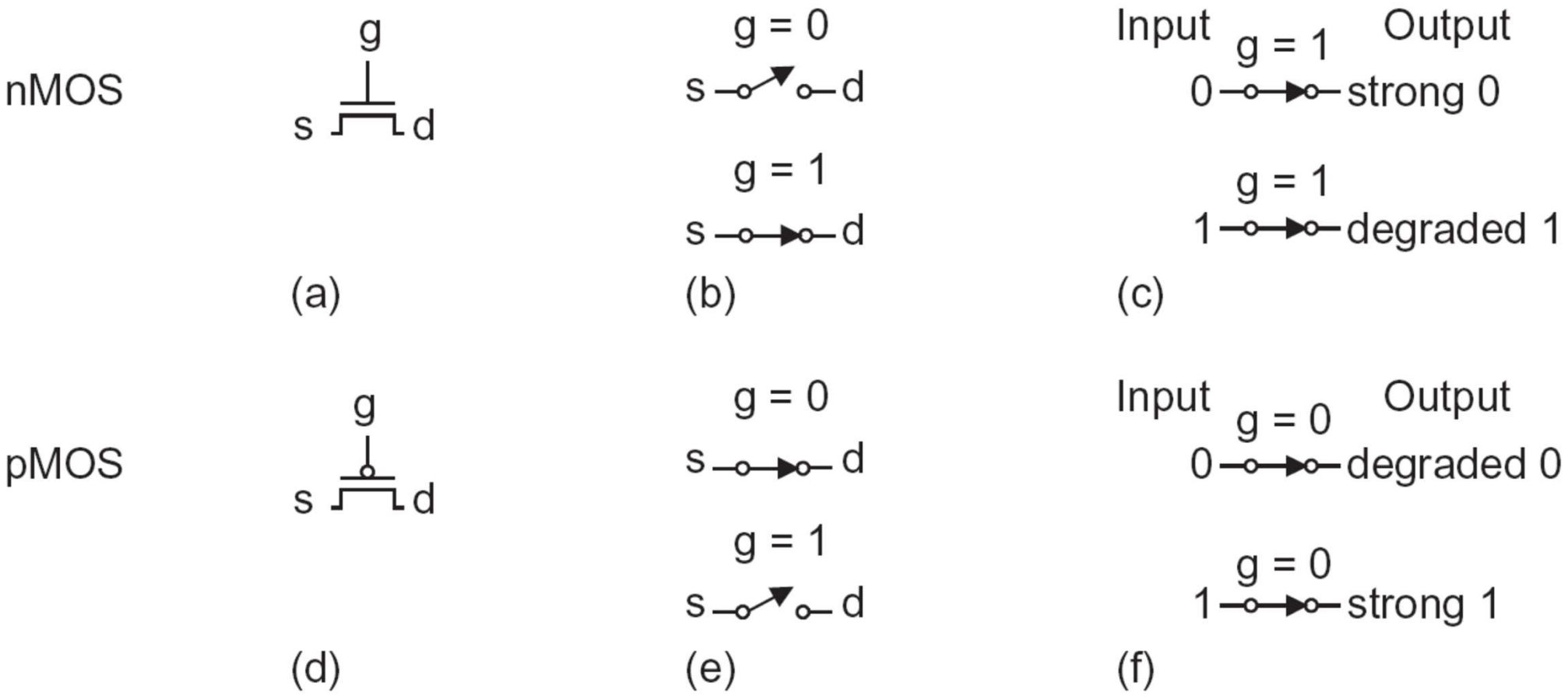


nMOS Transistor

pMOS Transistor

MOS TRANSISTOR

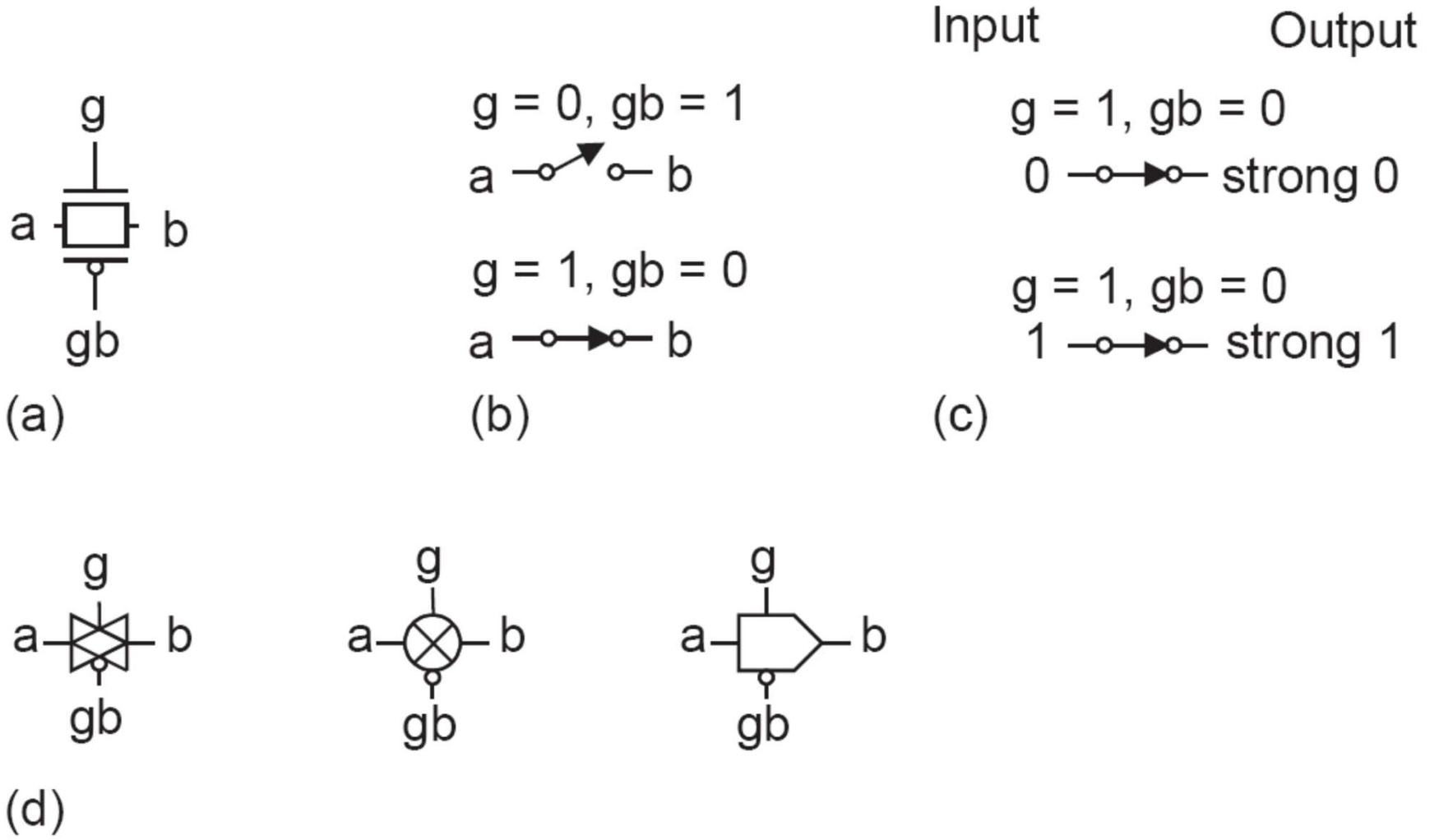
- **Pass transistor**



Pass transistor strong and degraded outputs

MOS TRANSISTOR

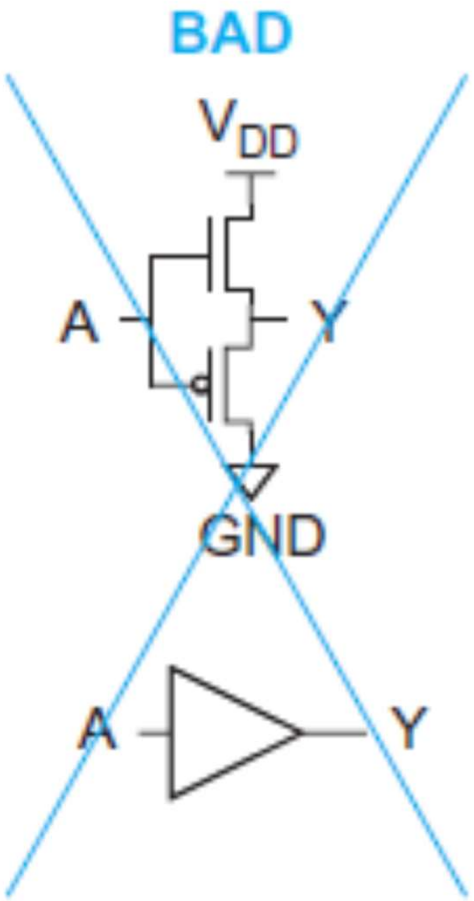
- **Transmission gate**



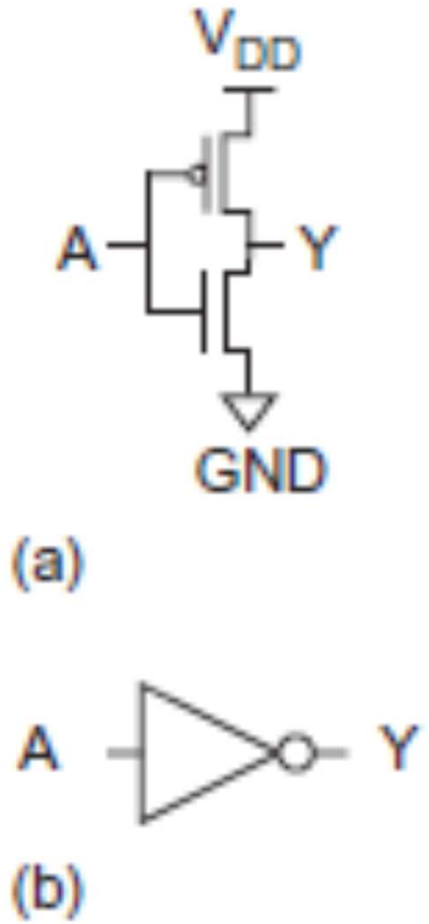
Transmission gate

MOS TRANSISTOR

- **Inverting gate:** *fully restored*



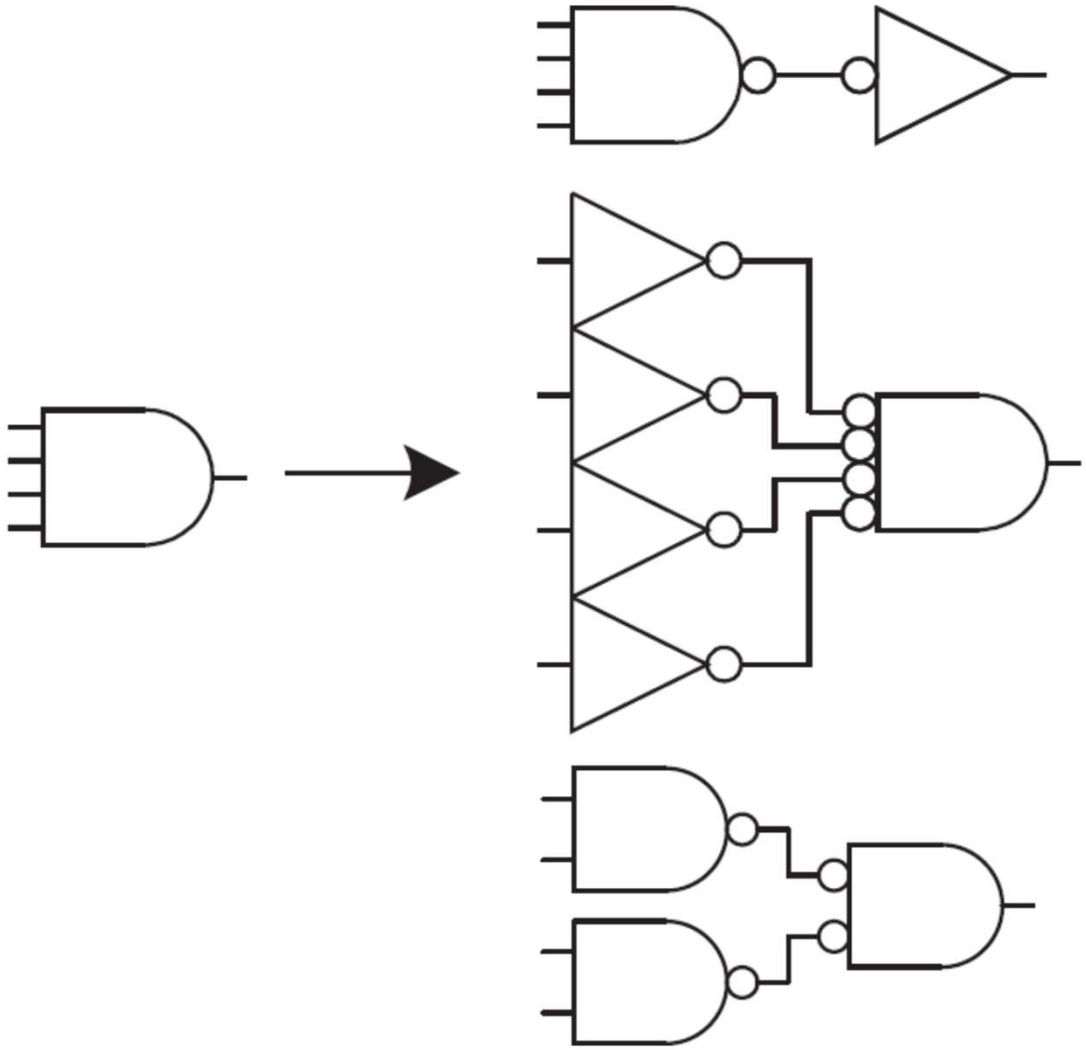
Bad non-inverting buffer



Inverter schematic (a) and symbol (b)

MOS TRANSISTOR

- **Solution for building non-inverting gates**



Various implementations of a CMOS 4-input AND gate

Outline

- MOS Transistors
- **NMOS vs. CMOS Logic Circuits**
- MOS Logic Circuits
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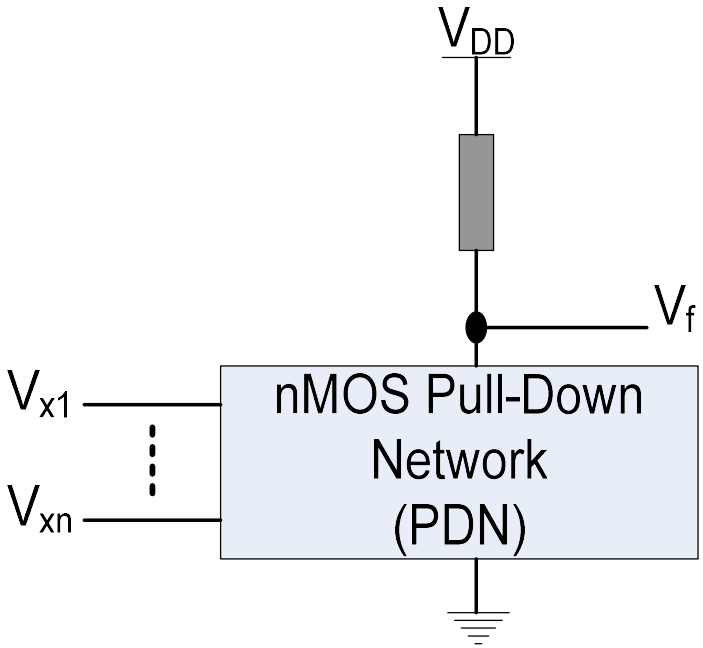
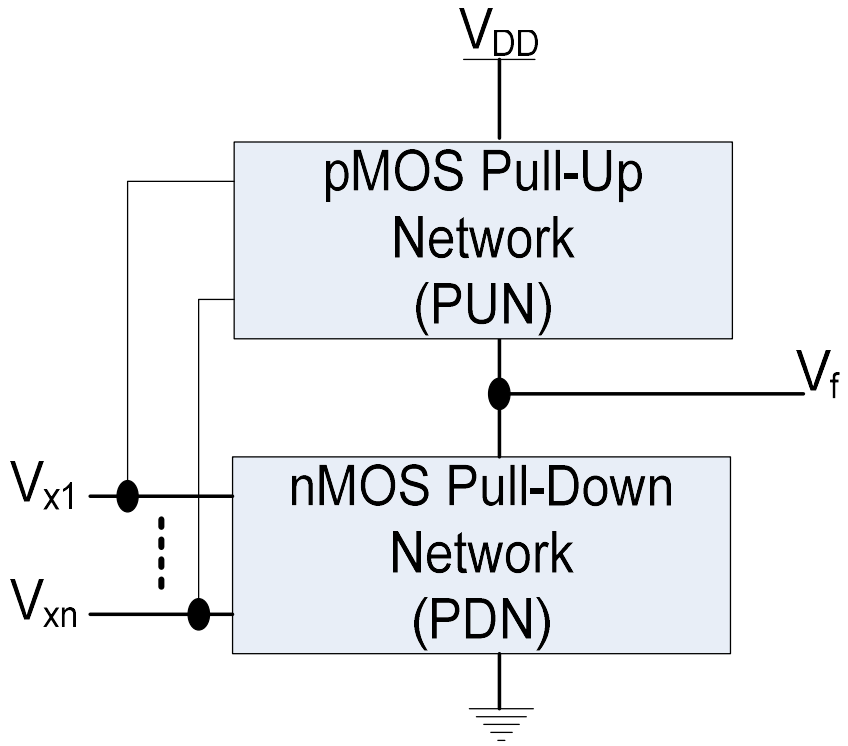
NMOS vs. CMOS LOGIC CIRCUITS

- **Pull-down Network** (PDN): composed of **NMOS transistors** in series (or parallel)
- **Pull-up Network** (PUN): composed of **PMOS transistors** in parallel (or series)
- PDN and PUN networks are complements of each other, have equal numbers of transistors:
  - either the PDN pulls V_f down to Gnd or the PUN pulls V_f up to VDD



Structure of a NMOS circuit



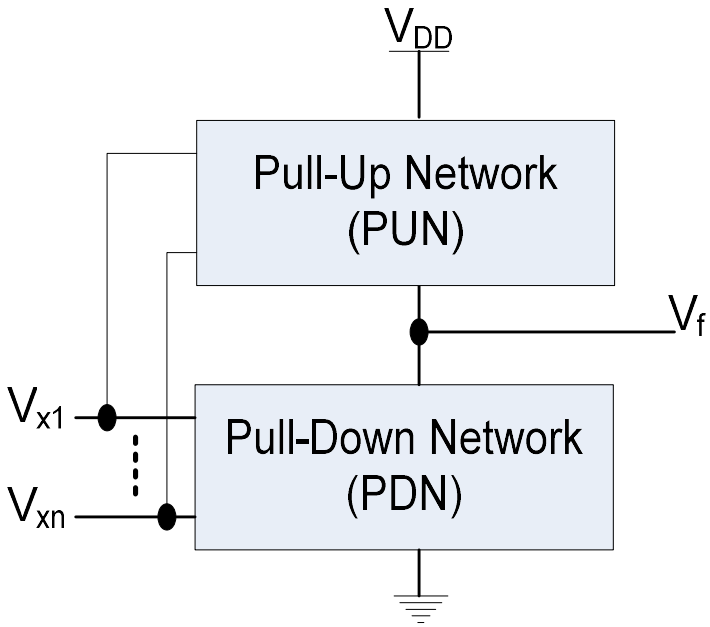
Structure of a CMOS circuit

Outputs of CMOS LOGIC CIRCUITS

- ***High impedance* or *floating* Z output:** when both pull-up and pull-down are OFF
  - Importance in multiplexers, memory elements, and tristate bus drivers
- ***Contention* (or *Crowbarred*) X level**: when both pull-up and pull-down are simultaneously turned ON
  - indeterminate output level
  - dissipates static power
  - is usually an unwanted condition

Output states of CMOS gates

	Pull-up OFF	Pull-up ON
Pull-down OFF	**Z**	**1**
Pull-down ON	**0**	**Contention (X)**



Structure of a CMOS circuit

Outline

- MOS Transistors
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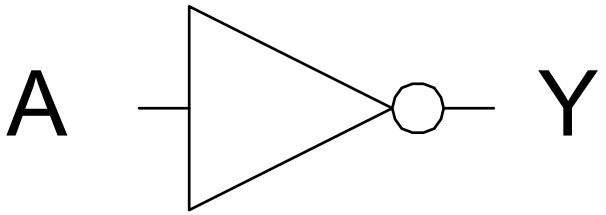
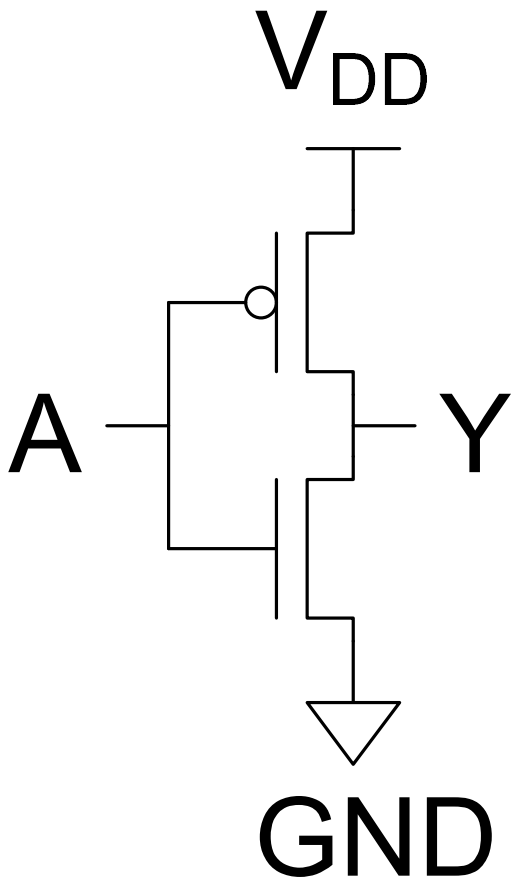
CMOS LOGIC CIRCUITS

- **Inverter:** $Y = \overline{A}$

Inverter truth table

A	Y



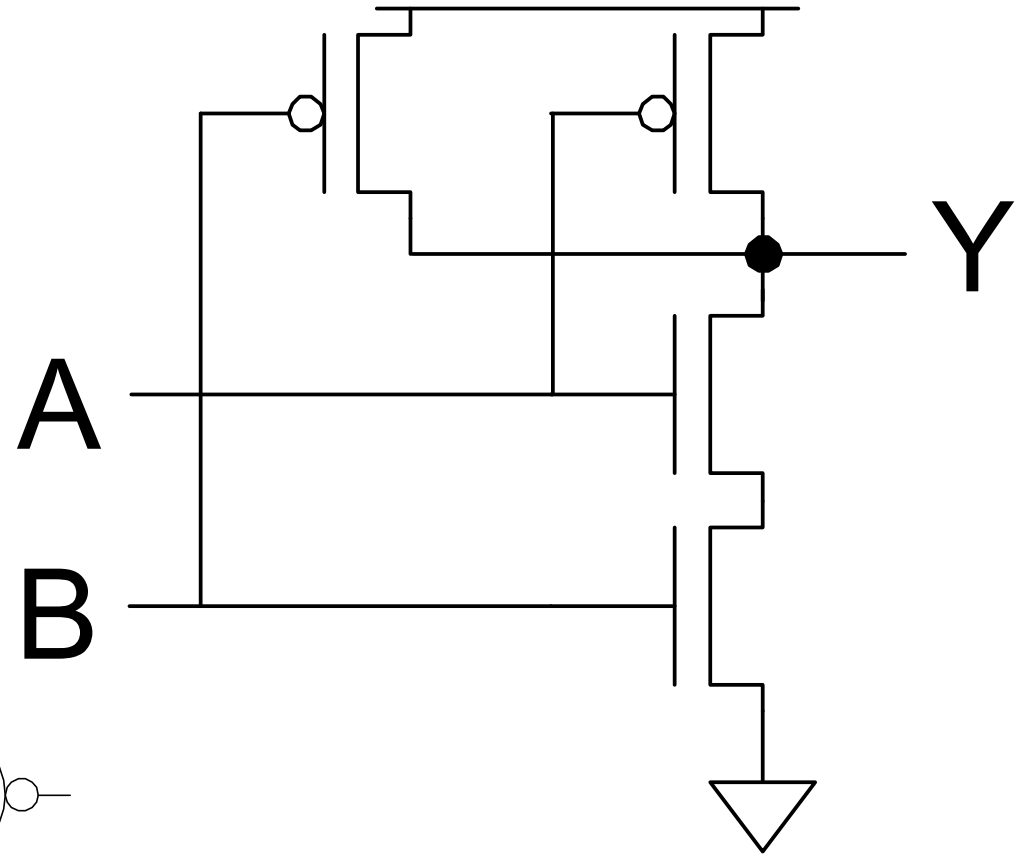


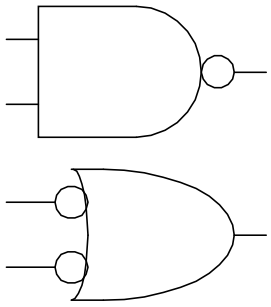
Symbol (a) and (b) Inverter schematic

MOS LOGIC CIRCUITS

- **2-input NAND Gate:** $Y = \overline{A \cdot B}$

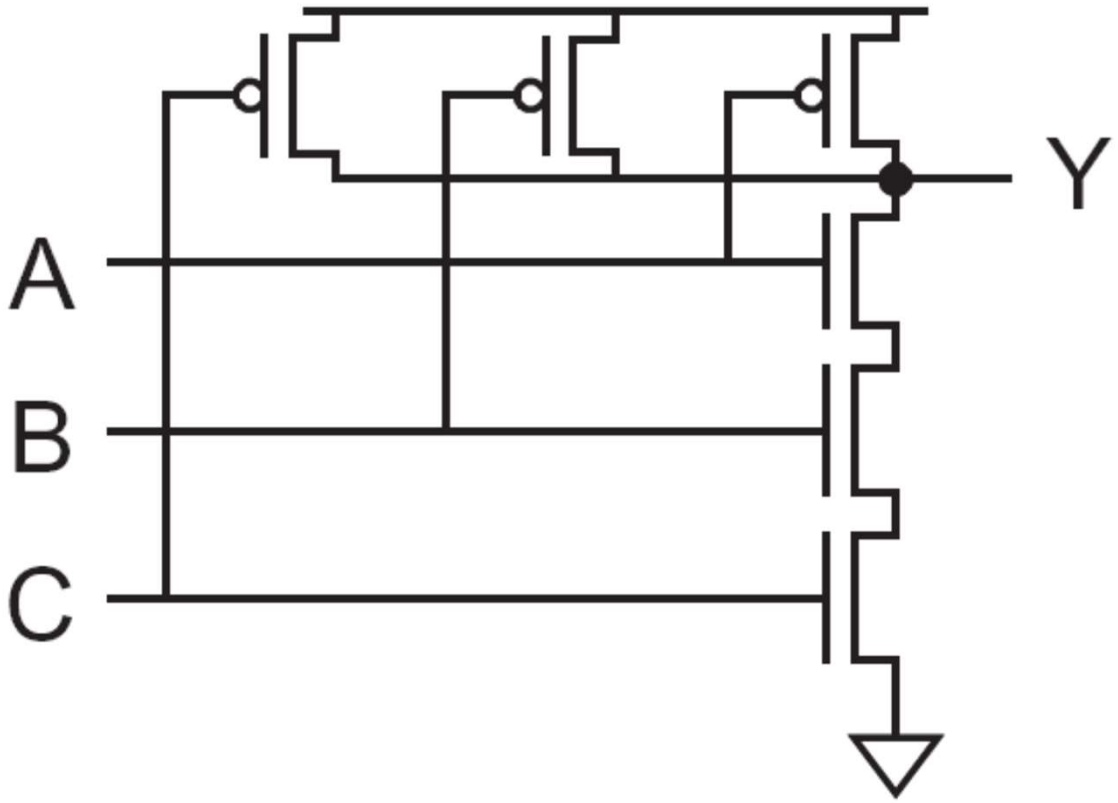
A	B	Y
0	0	
0	1	
1	0	
1	1	





MOS LOGIC CIRCUITS

- **k-input NAND Gate:**
  - k series nMOS transistors
  - k parallel pMOS transistor:



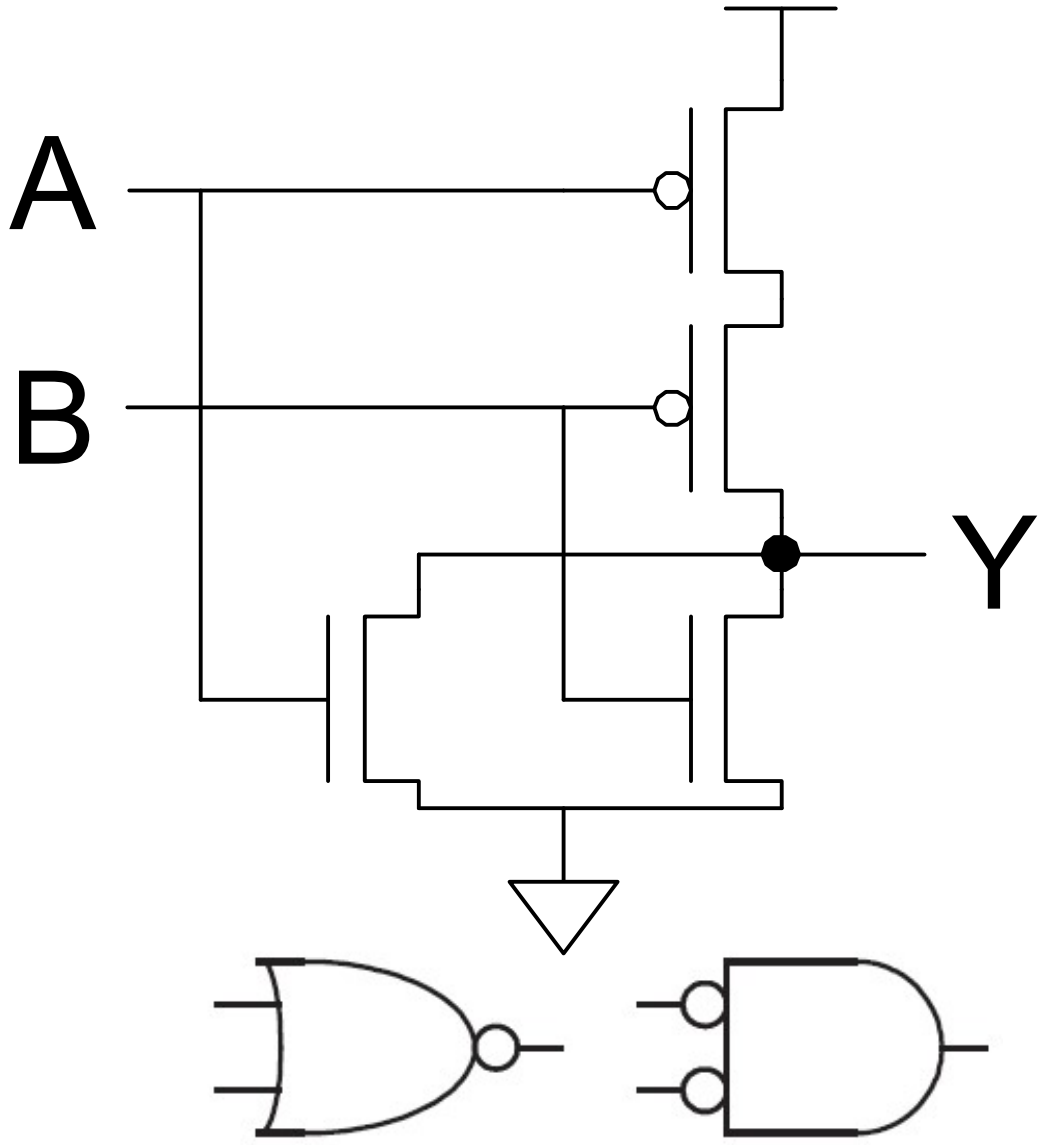
3-input NAND gate schematic

MOS LOGIC CIRCUITS

- **2-iput NOR Gate**:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$$Y = \overline{A + B}$$



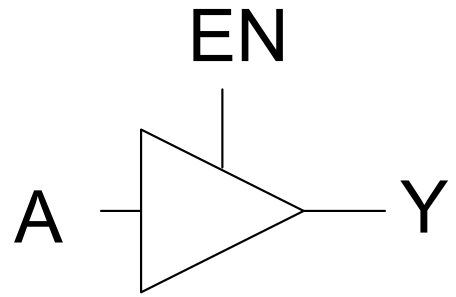
QUIZ

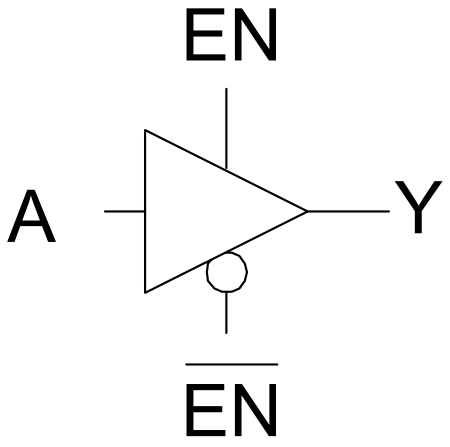
Sketch a k-input CMOS NOR gate?

MOS LOGIC CIRCUITS

- **Tristate Buffer**:
  - *Tristate buffer* produces Z when not enabled

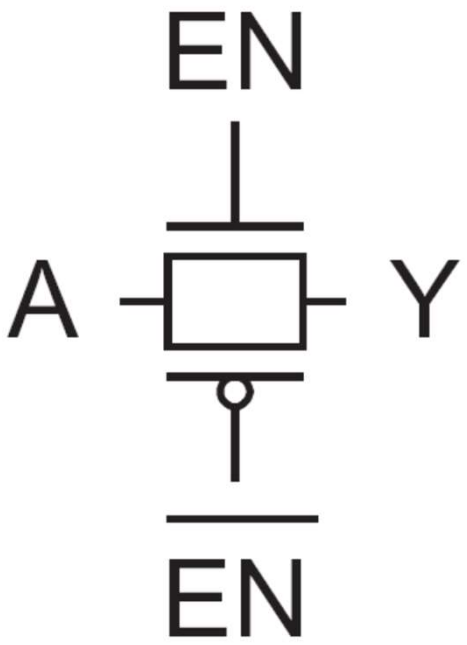
EN	A	Y
0	0	
0	1	
1	0	
1	1	





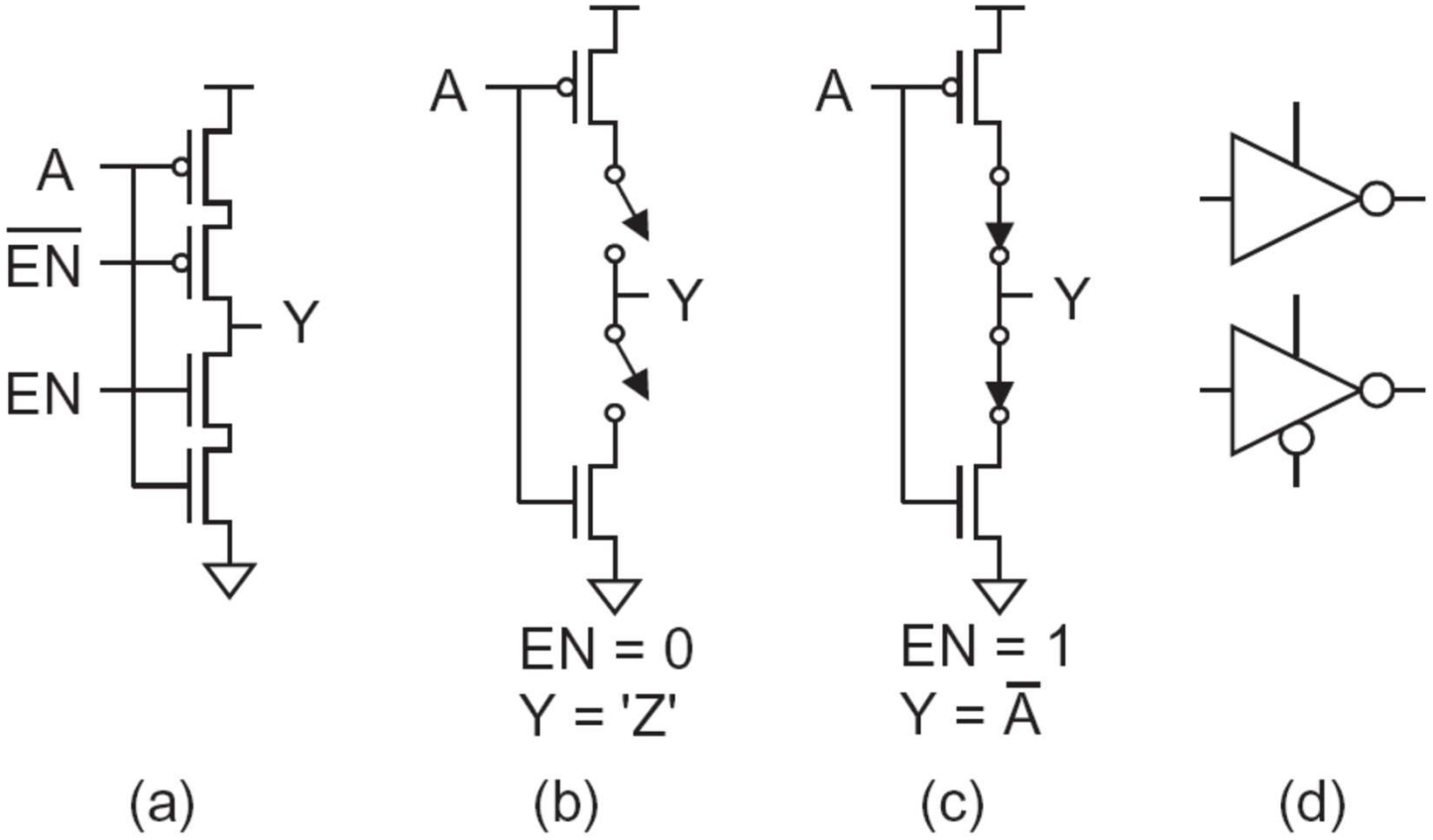
MOS LOGIC CIRCUITS

- **Tristate Buffer**:
  - Transmission Gate acts as tristate buffer
  - Advantage: Only two transistors
  - Drawback: **Nonstoring** - output level is not driven from V_{DD} or GND
    - Noise on A is passed on to Y



MOS LOGIC CIRCUITS

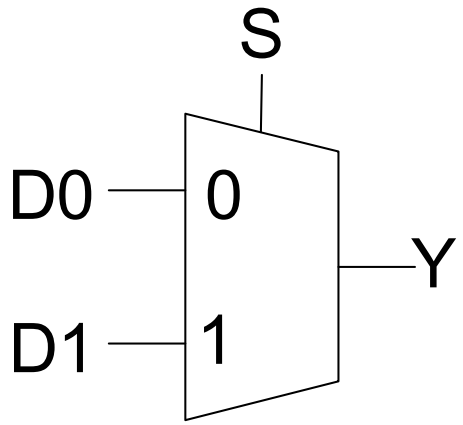
- **Tristate Inverter**:
  - *Application*: To allow multiple units to drive a common bus
  - *Drawback*: Delay between different EN signals switching can cause contention



MOS LOGIC CIRCUITS

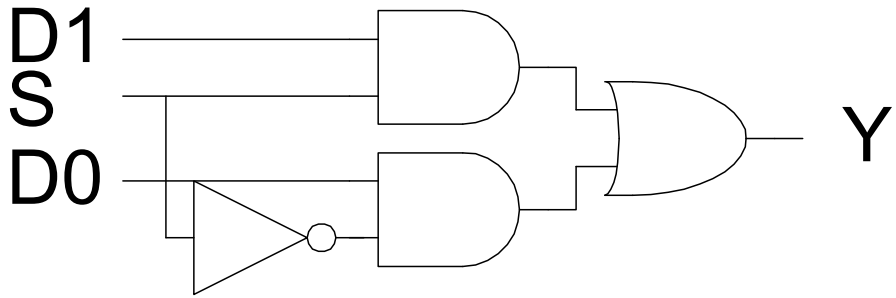
- **Multiplexer:**
  - 2:1 multiplexer chooses between two inputs

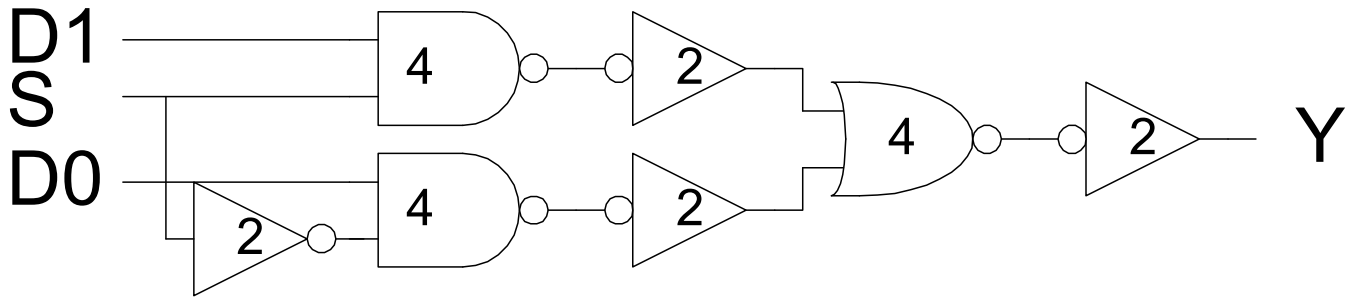
S	D1	D0	Y
0	X	0	
0	X	1	
1	0	X	
1	1	X	



MOS LOGIC CIRCUITS

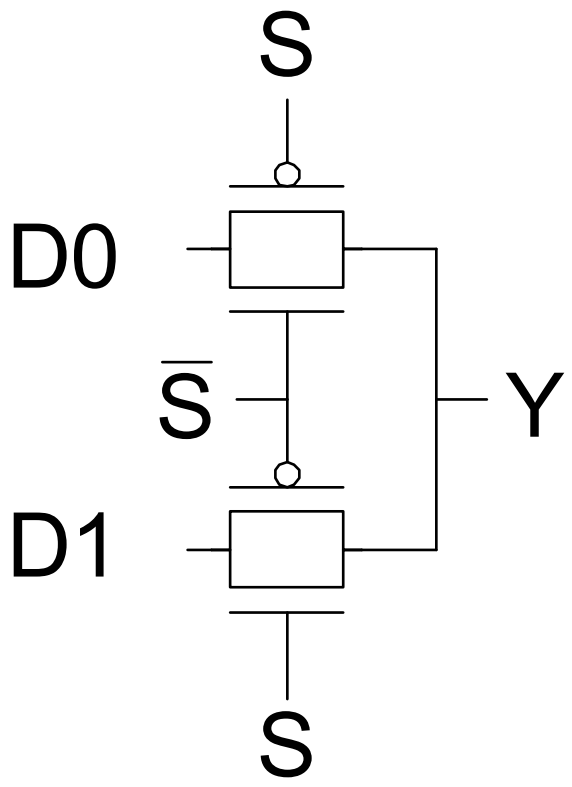
- **Multiplexer:**
  - $Y = SD_1 + \overline{S}D_0$ (too many transistors)
  - How many transistors are needed?





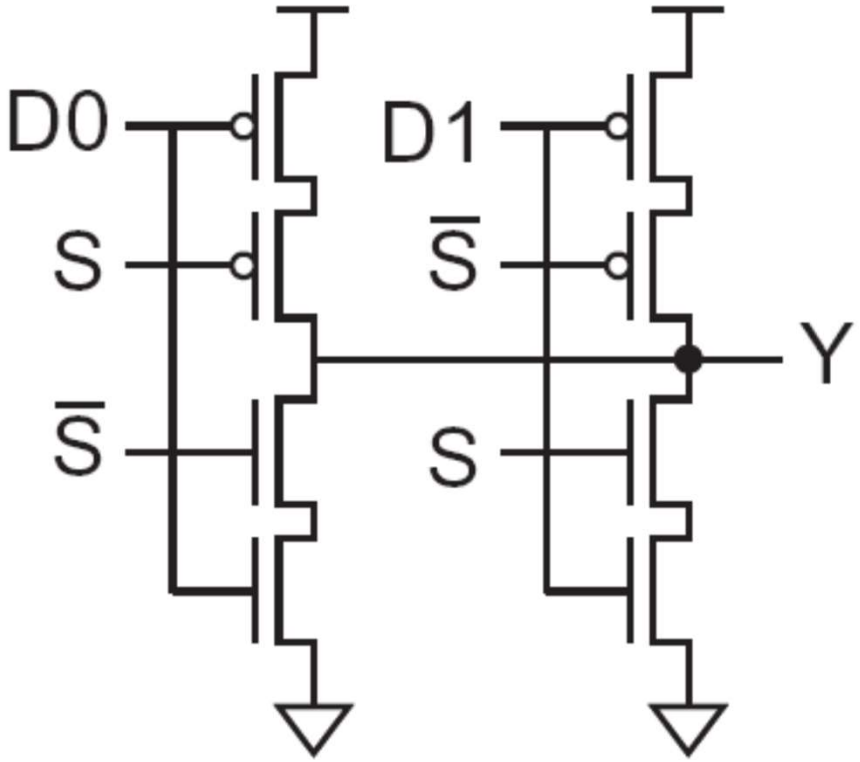
MOS LOGIC CIRCUITS

- **Multiplexer:**
  - Non-storing MUX uses two transmission gates
    - Only 4 transistors

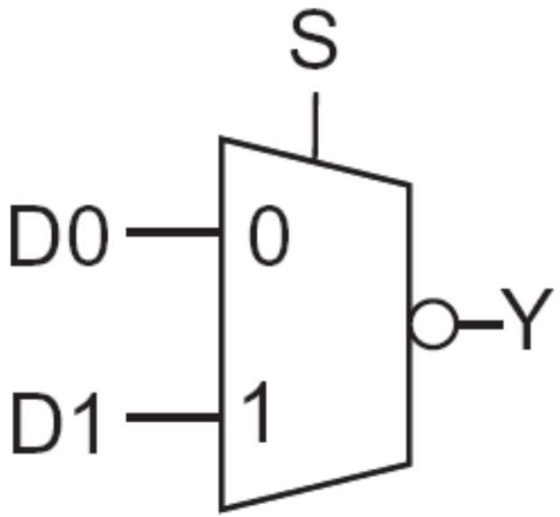


MOS LOGIC CIRCUITS

- **Inverting Multiplexer**:
  - Use a pair of tristate inverters



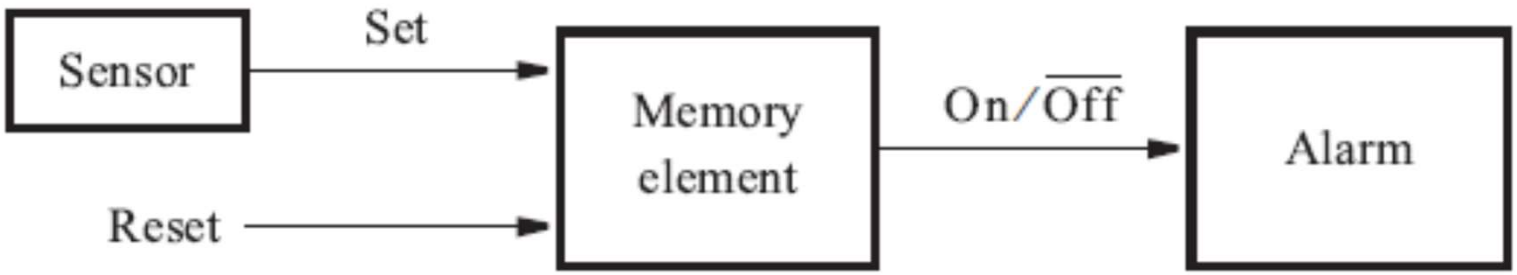
(b)



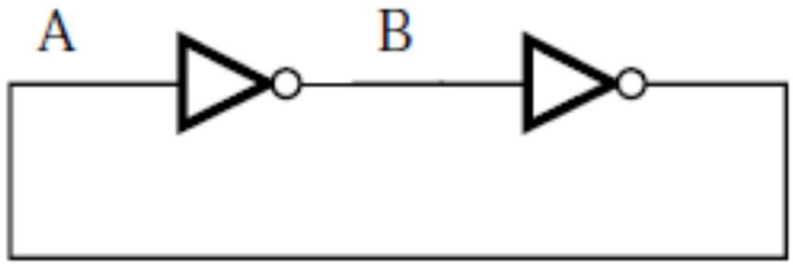
(c)

MOS LOGIC CIRCUITS

- **Sequential Circuits:** have memory, their outputs depend on both current and previous inputs.
  - Examples: latches and flip-flops



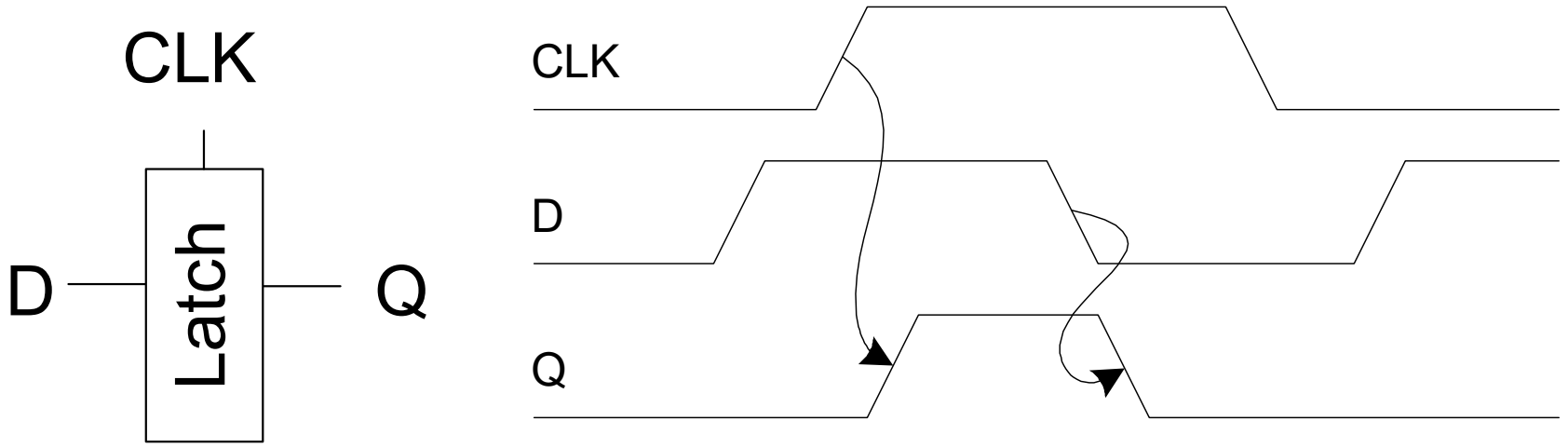
Control of an alarm system



A simple memory element

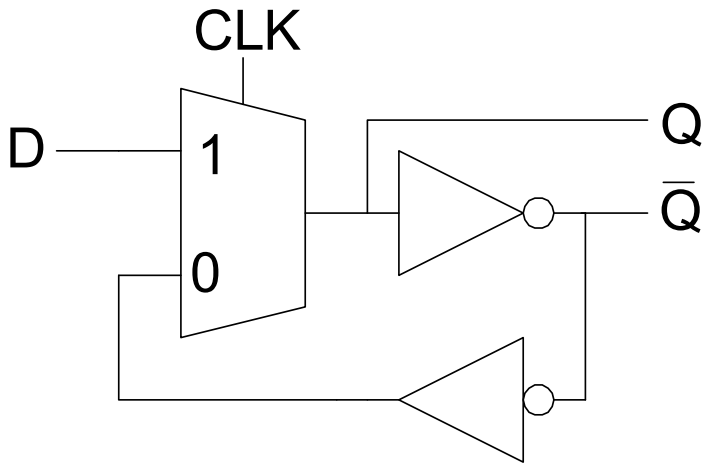
MOS LOGIC CIRCUITS

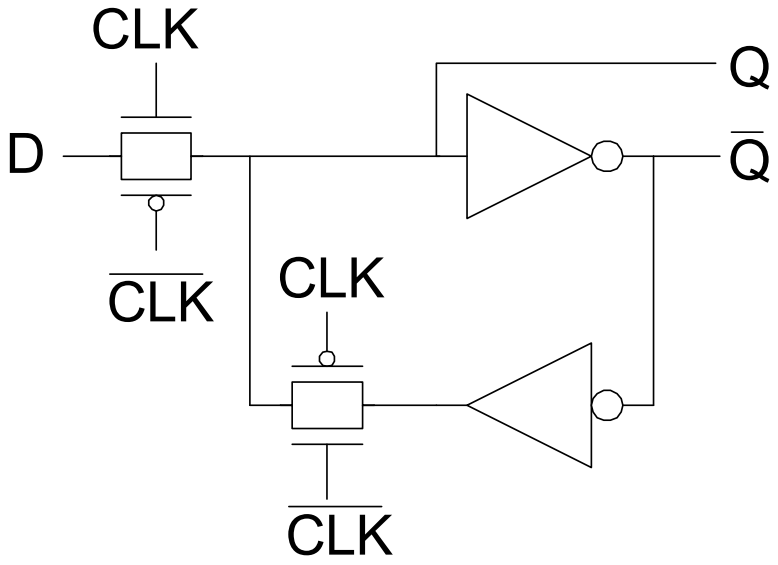
- **D Latch:**
  - When CLK = 1, latch is *transparent*
    - D flows through to Q like a buffer
  - When CLK = 0, the latch is *opaque*
    - Q holds its old value independent of D
  - a.k.a. *transparent latch* or *level-sensitive latch*



MOS LOGIC CIRCUITS

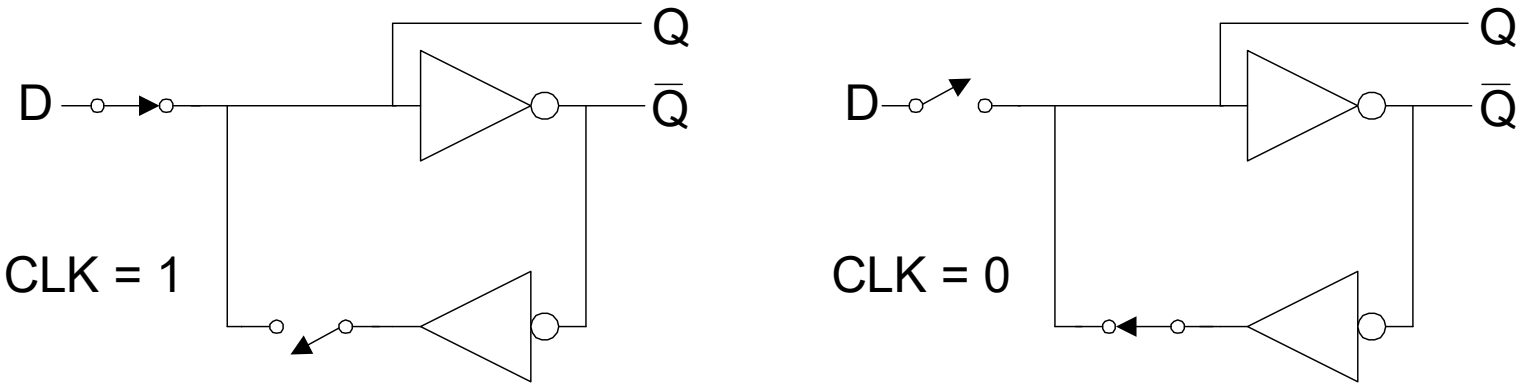
- **D Latch:**
  - Use a MUX and two inverters

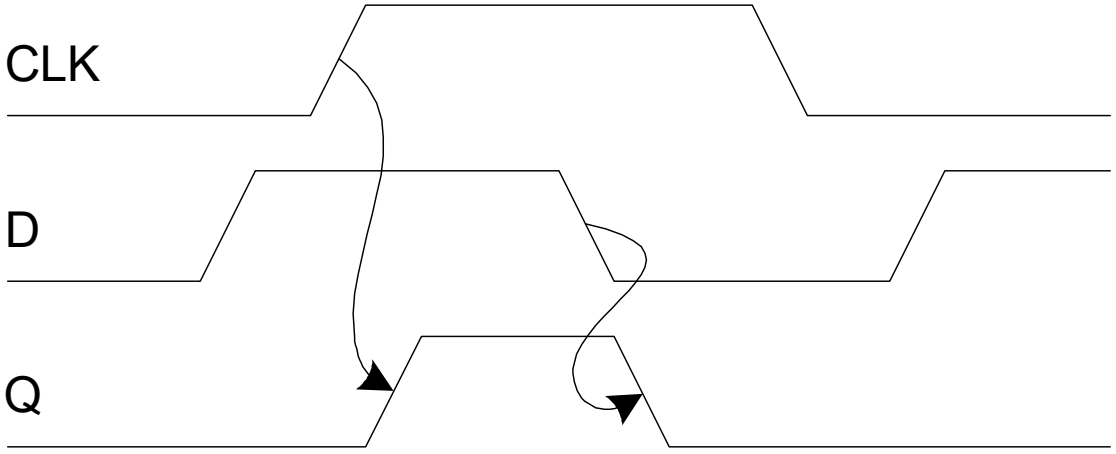




MOS LOGIC CIRCUITS

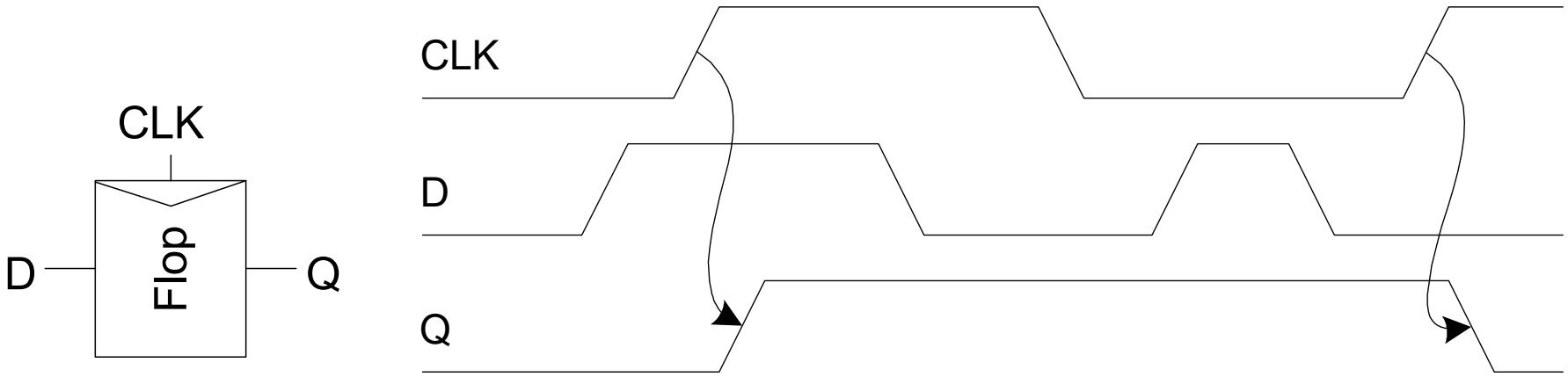
- **D Latch:**
  - Operation





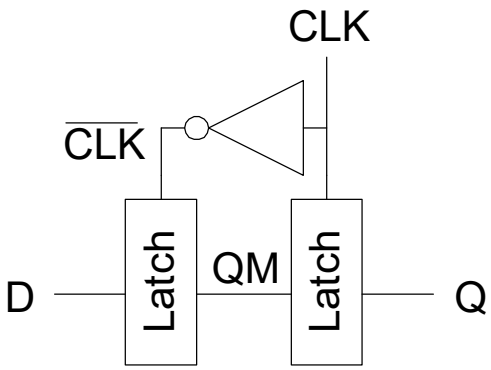
MOS LOGIC CIRCUITS

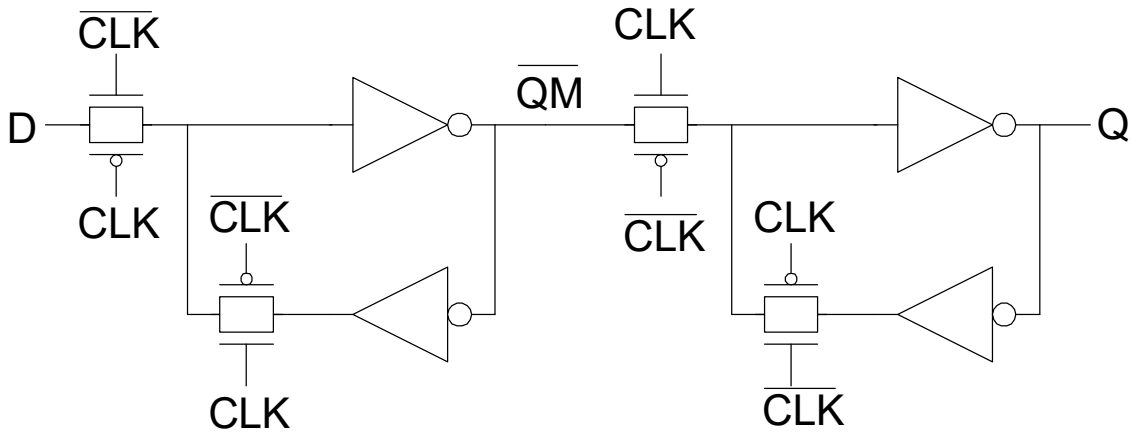
- **Flip-Flops:**
  - When CLK rises, D is copied to Q
  - At all other times, Q holds its value
  - a.k.a. *positive edge-triggered flip-flop, master-slave flip-flop*



MOS LOGIC CIRCUITS

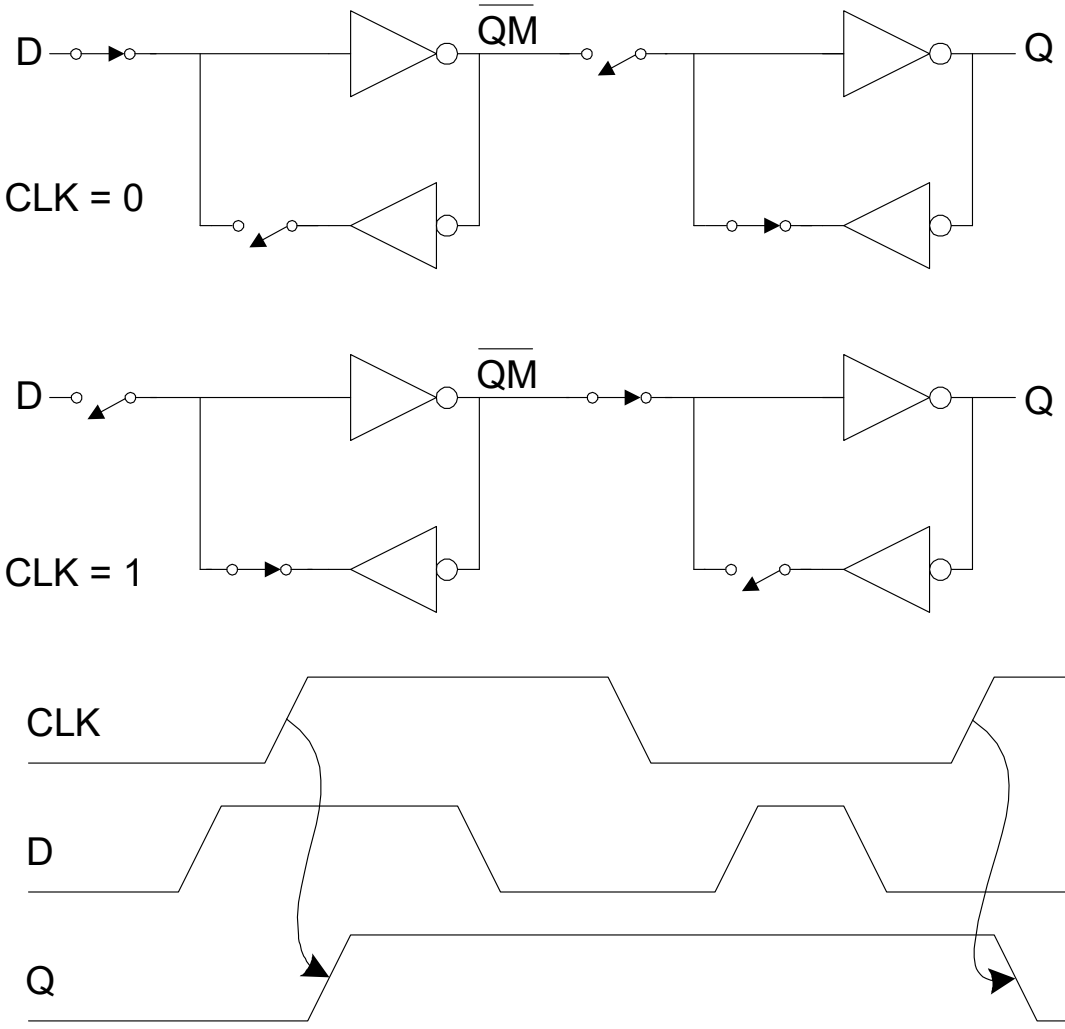
- **Flip-Flops:**
  - Combining between one negative-sensitive D latch and one positive-sensitive D latch





MOS LOGIC CIRCUITS

- **Flip-Flops:**
  - Operation: triggered by positive-edge clock



Outline

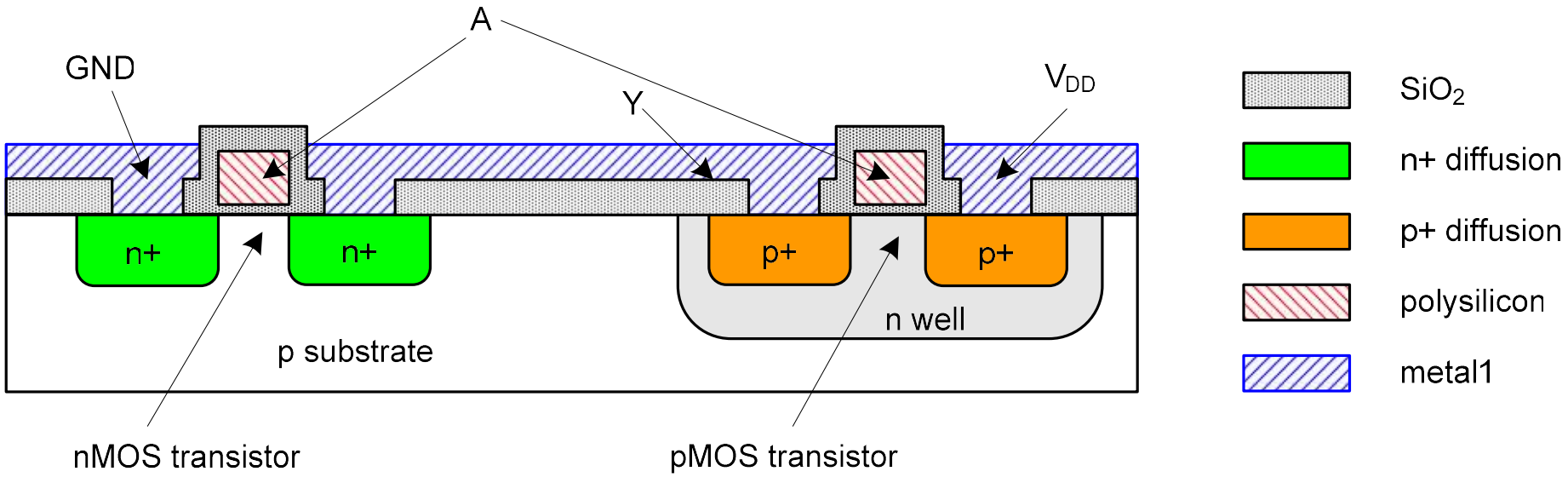
- MOS Transistors
- NMOS vs. CMOS Logic Circuits
- MOS Logic Circuits
- **CMOS Fabrication and Layout**
- Summary

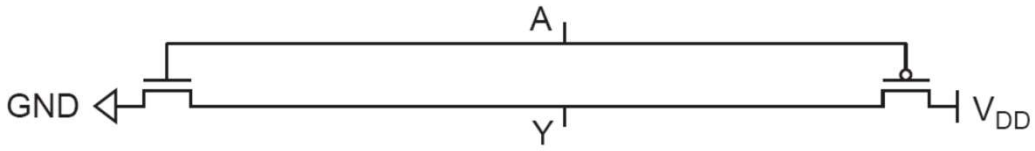
CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer with set of masks
- *Photolithography* process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

CMOS Fabrication

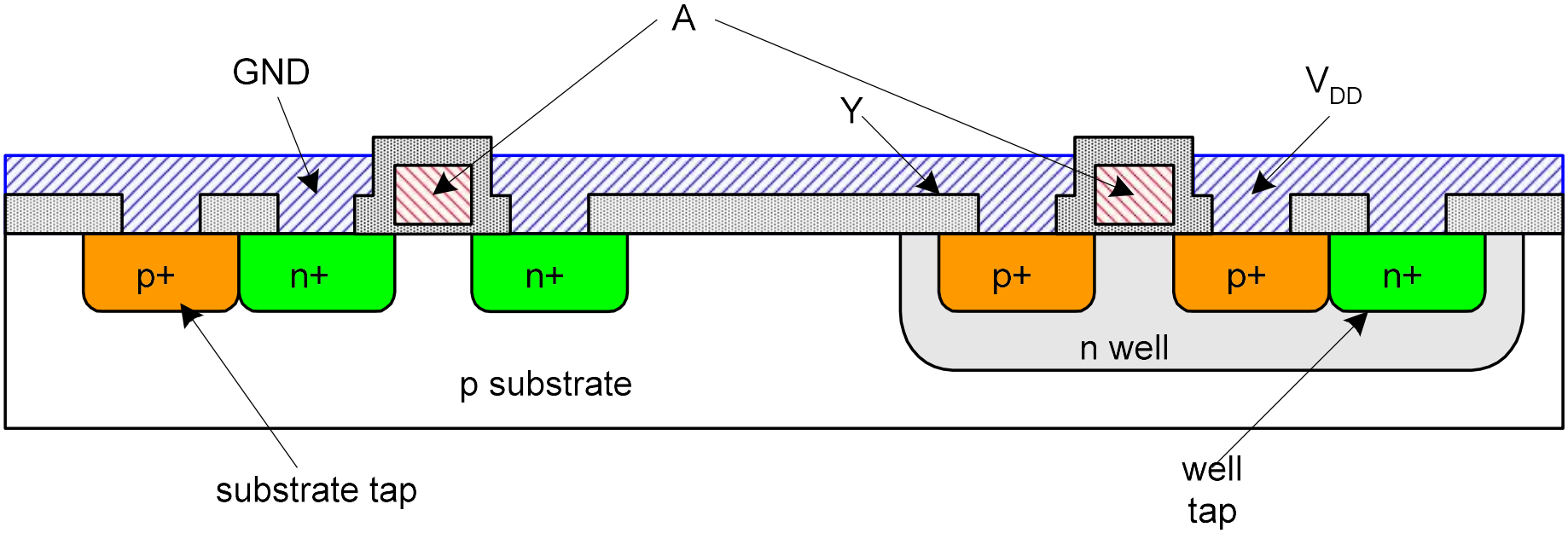
- **Cross-section and corresponding schematic of an inverter**
  - **p-type substrate**
  - An **n-well** is diffused (khuếch tán) into the substrate to create n-type body of pMOS transistor.

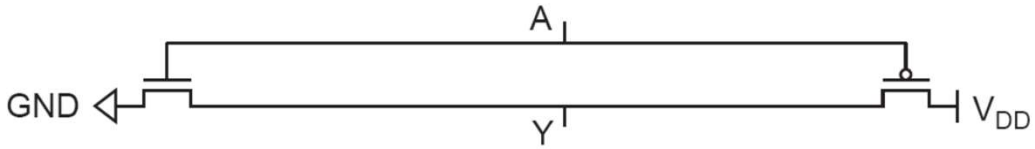




CMOS Fabrication

- **Cross-section and corresponding schematic of an inverter**
  - Substrate must be tied to GND and n-well to VDD
  - Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
  - Use heavily doped well and substrate contacts / taps



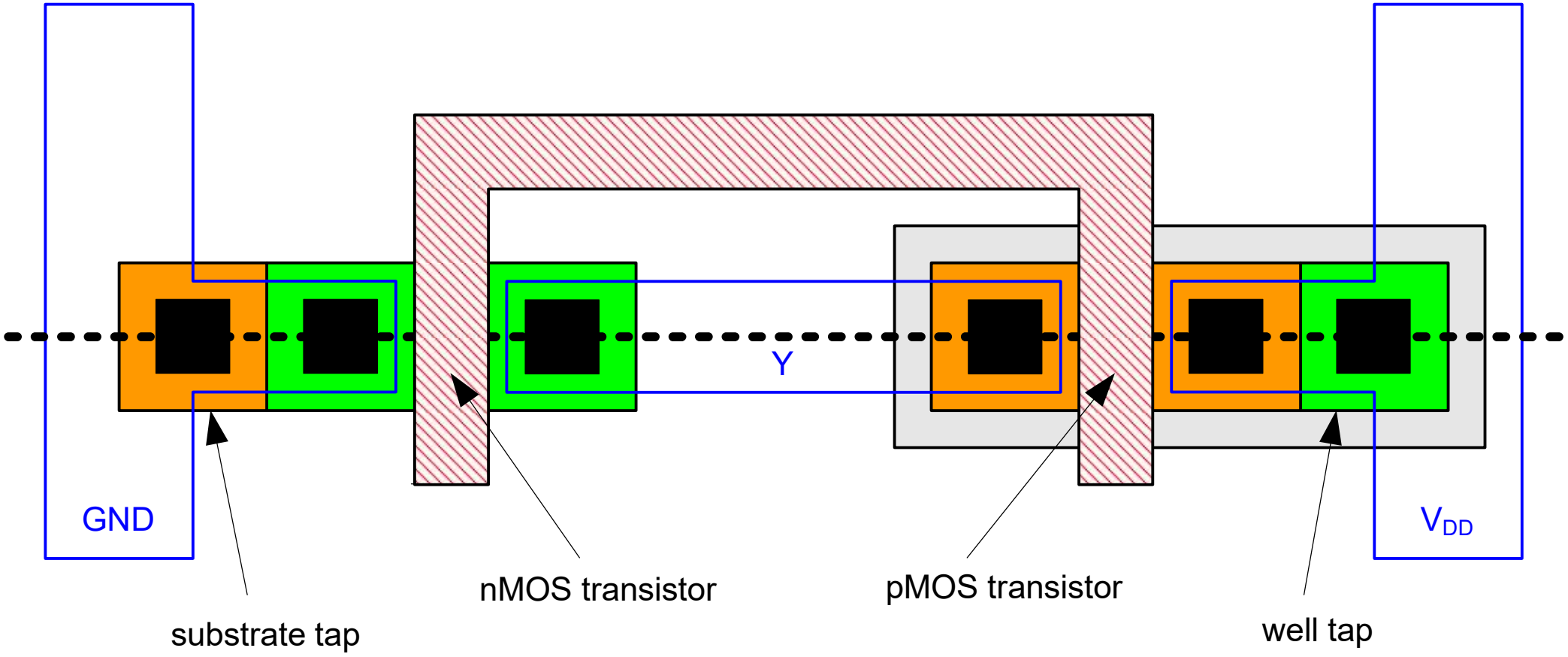


CMOS Fabrication

- **The fabrication sequence consists of a series of steps in which layers of the chip are defined through a process called *photolithography (quang khắc)*:**
  - Etching (Ăn mòn)
  - Doping (pha tạp): Diffusion (khuyếch tán) or *Ion Implantation (Cấy ion)*
  - Oxidation
  - Deposition techniques (*phương pháp tạo màng mỏng*): chemical vapor deposition (*Kết tủa hóa trong pha hơi*), …

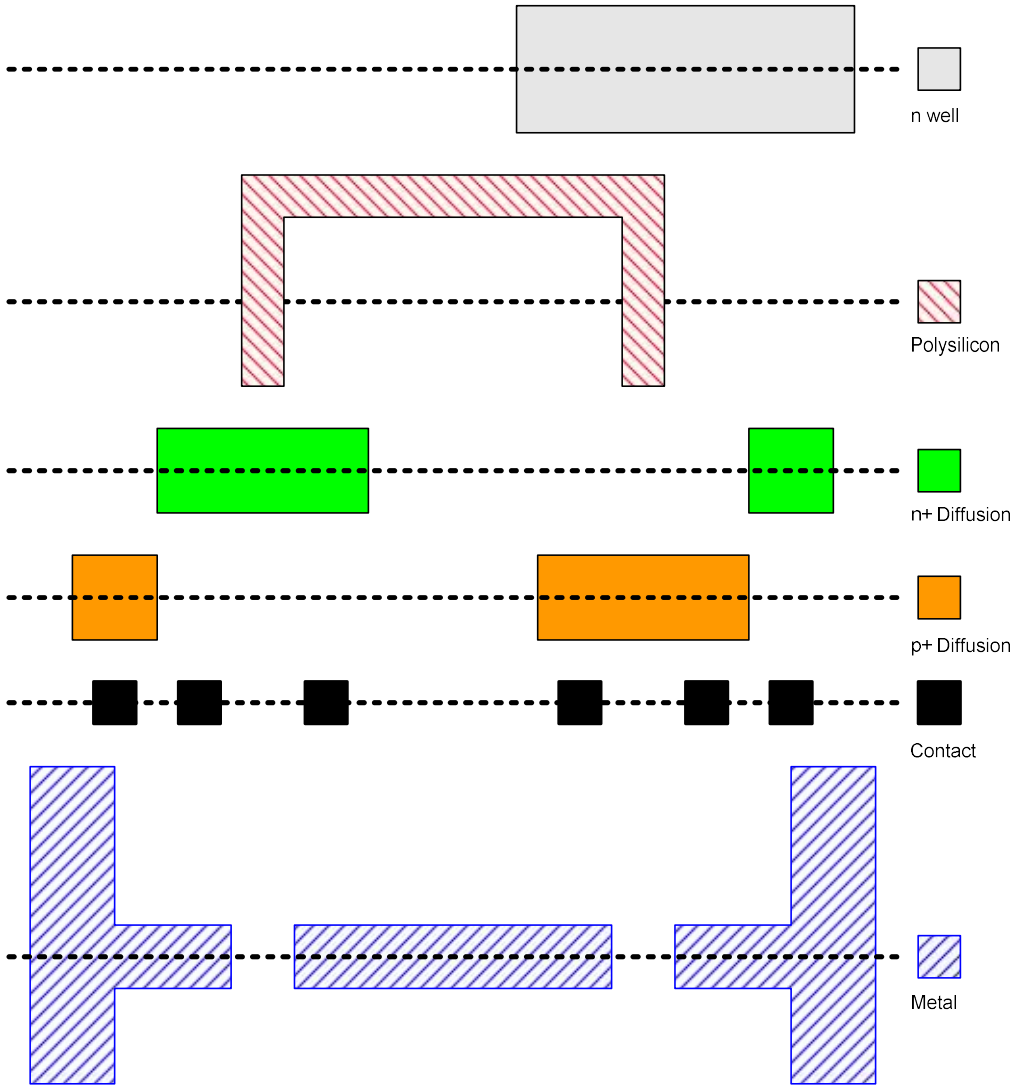
CMOS Fabrication

- **Masks** specify where the components (i.e. Transistors and wires) will be manufactured on the chip.



CMOS Fabrication

- The inverter could be defined by a **hypothetical set of six masks:**
  - **n-well,**
  - **polysilicon,**
  - **n+ diffusion,**
  - **p+ diffusion,**
  - **contacts,**
  - **and metal.**



Fabrication

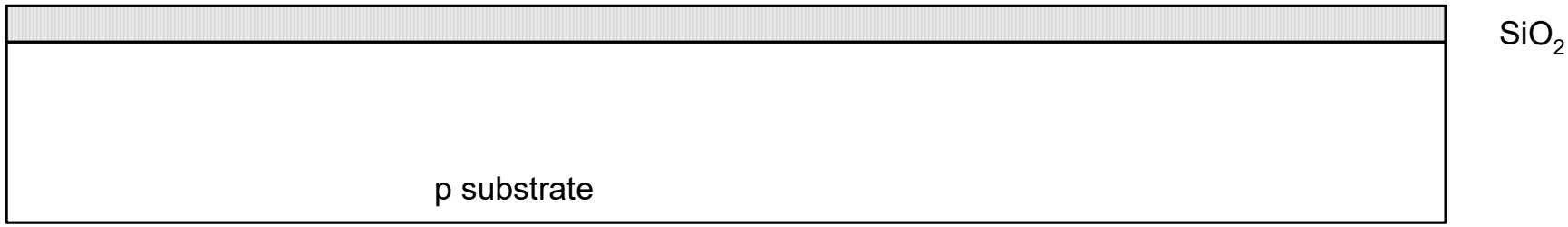
- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields

Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

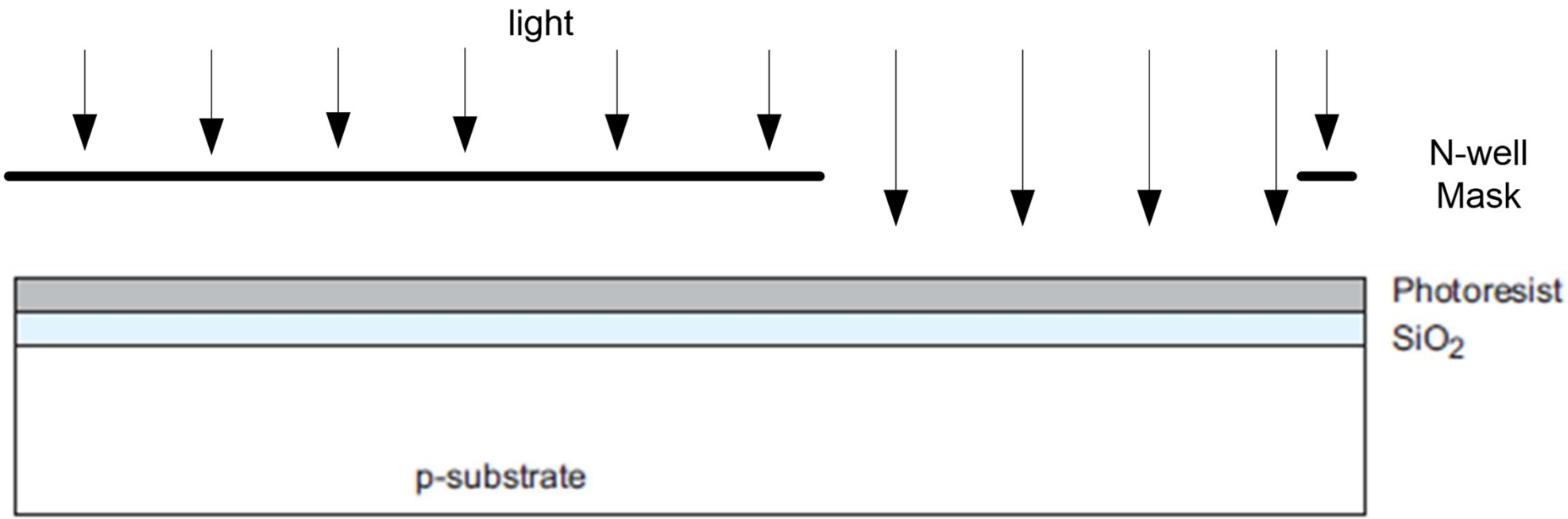
Oxidation

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 C with H_2O or O_2 in oxidation furnace



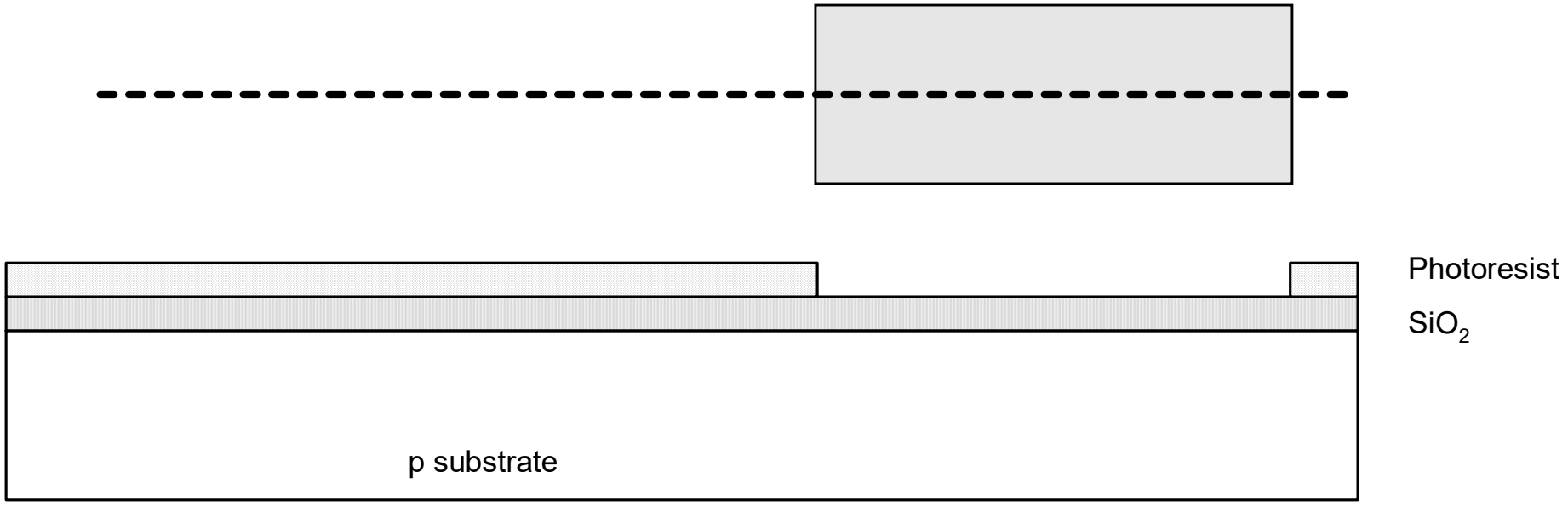
Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



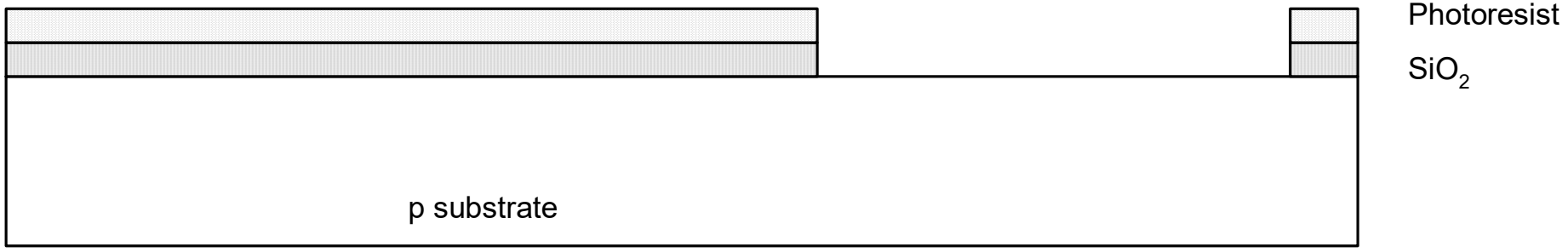
CMOS Fabrication and Layout

- Expose photoresist through n-well mask
- Strip off exposed photoresist



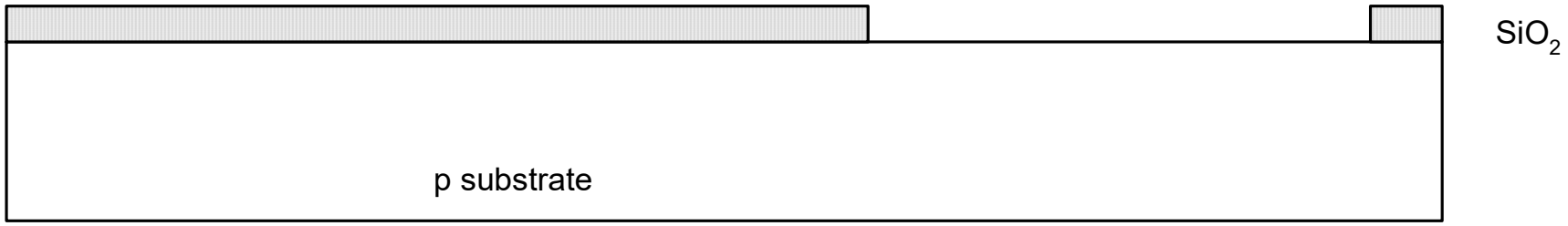
Etch

- Etch oxide with hydrofluoric (HF) acid
  - Only attacks oxide where photoresist has been exposed



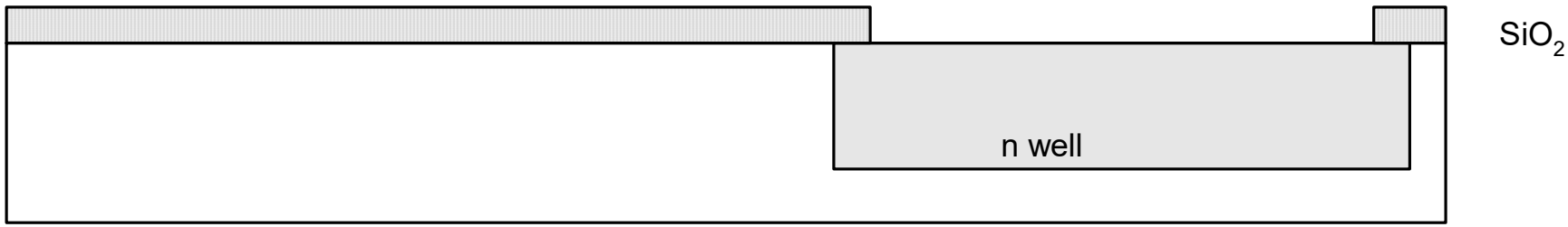
Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so photoresist doesn't melt in next step



n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si

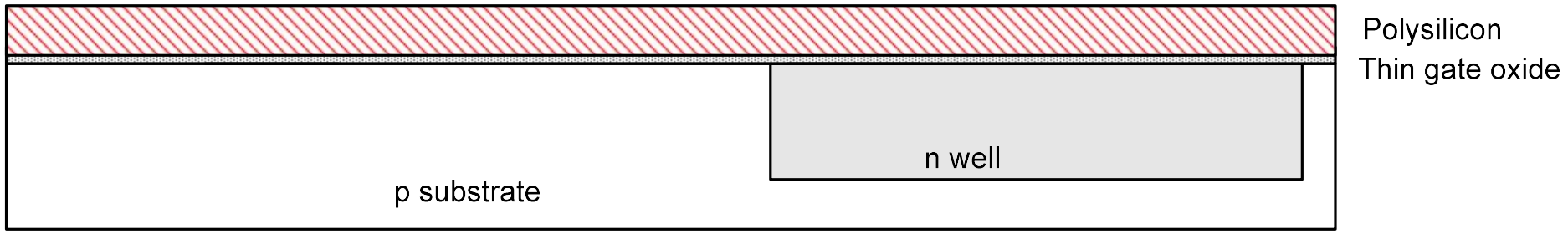


Strip Oxide

- Strip off the remaining oxide using HF acid
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

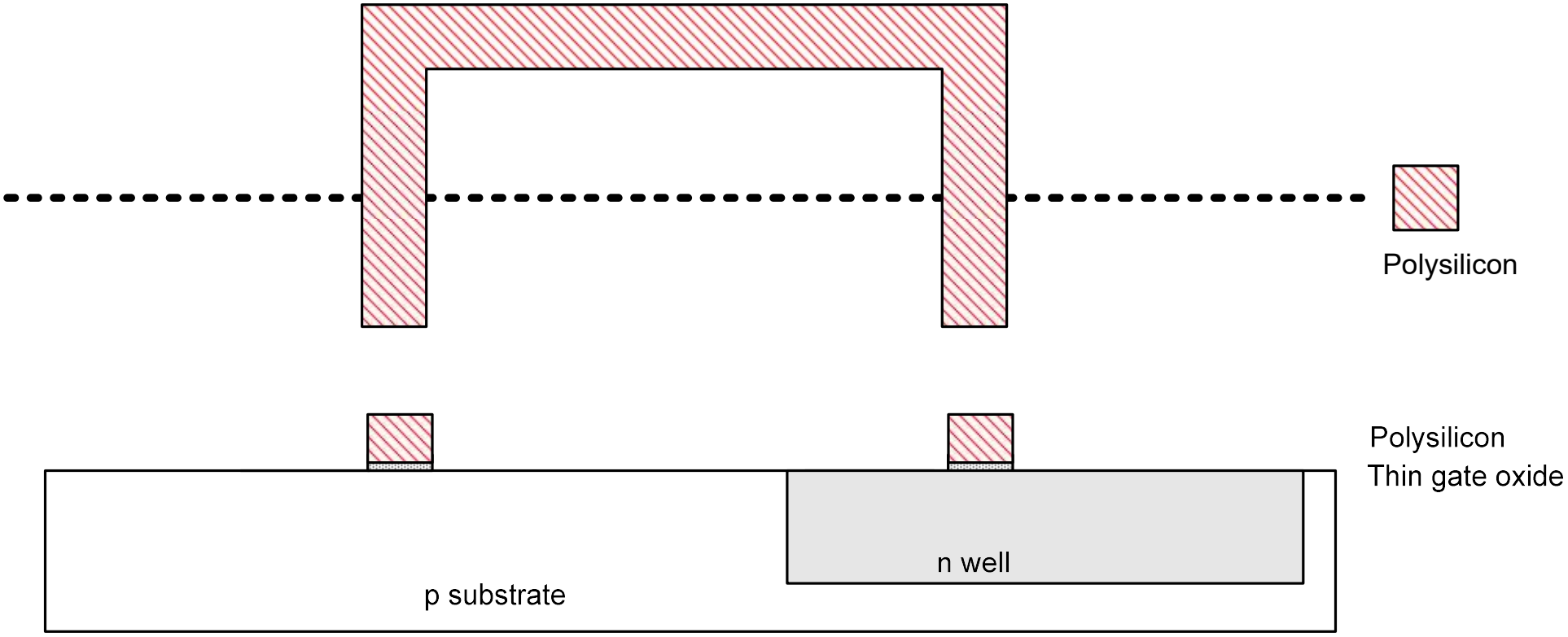
Polysilicon

- Deposit very thin layer of gate oxide
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



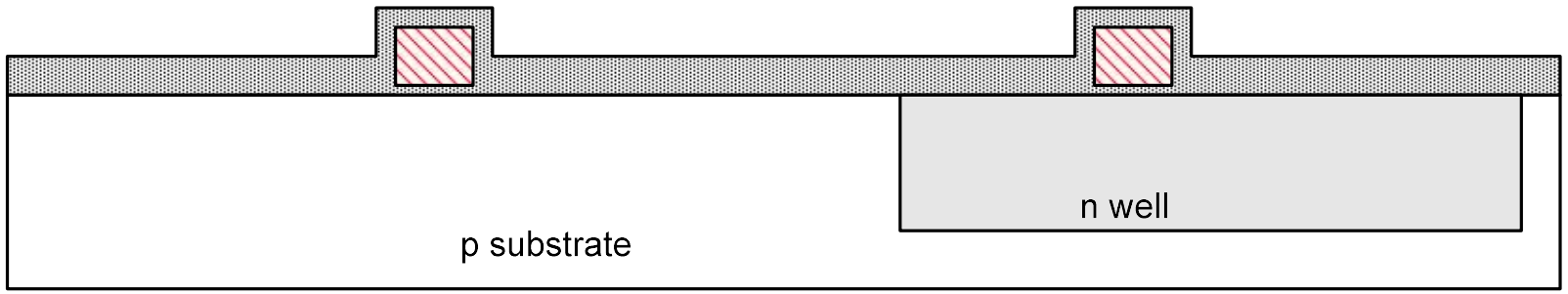
Polysilicon Patterning

- Use same lithography process to pattern polysilicon



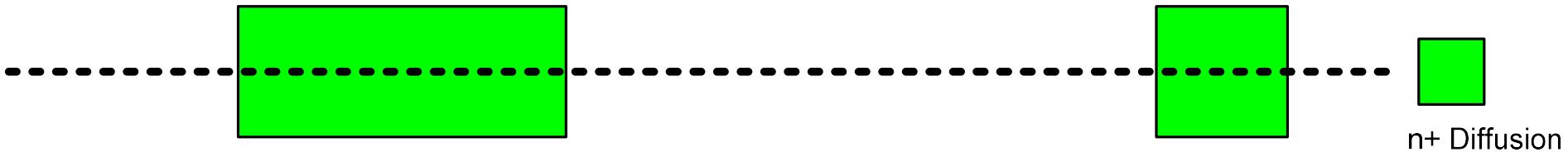
Self-Aligned Process

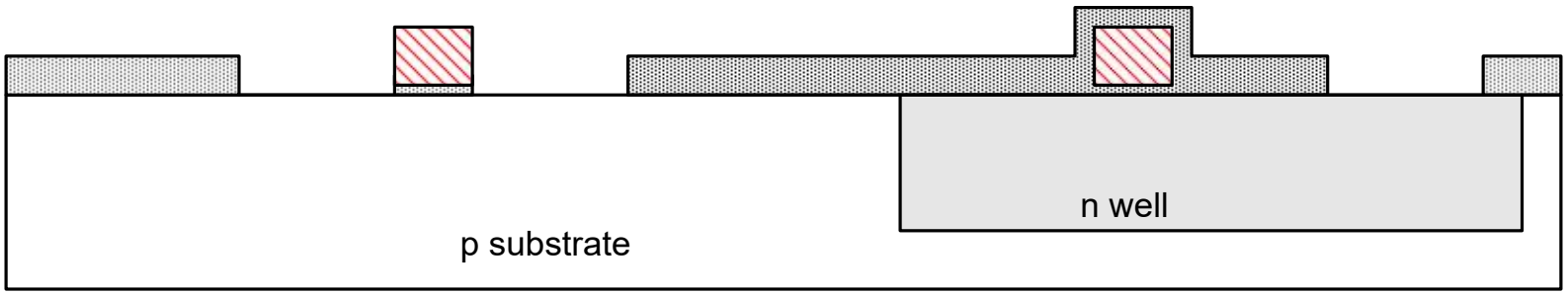
- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



N-diffusion

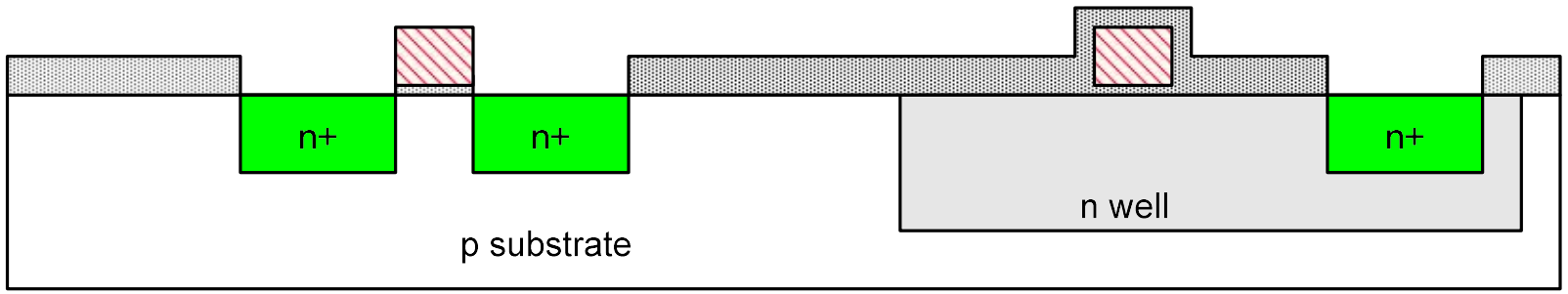
- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing





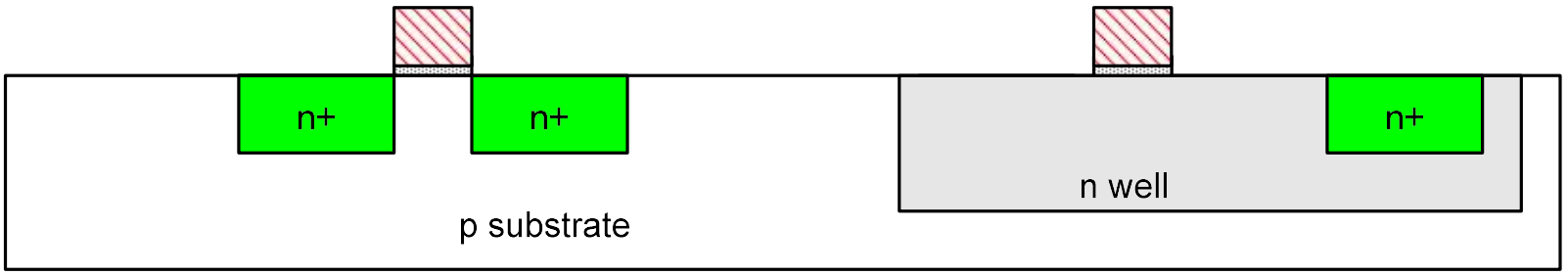
N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



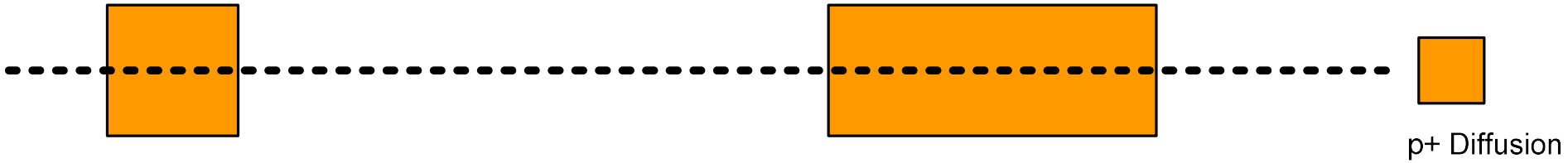
N-diffusion cont.

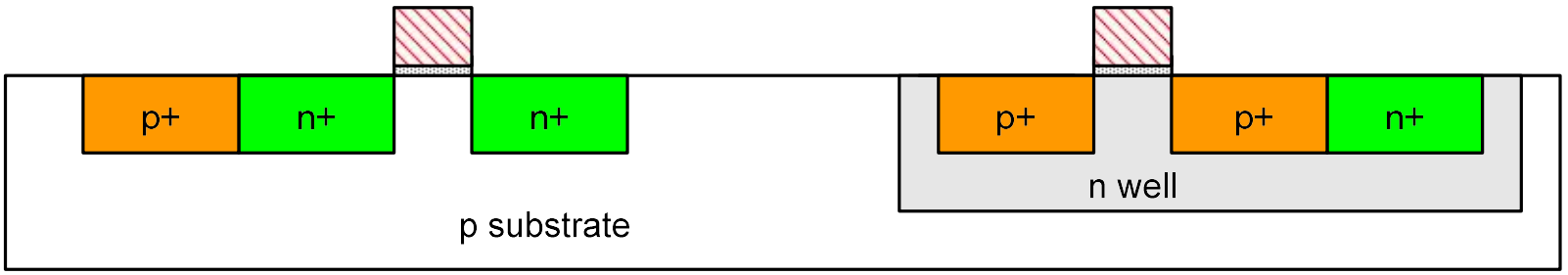
- Strip off oxide to complete patterning step



P-Diffusion

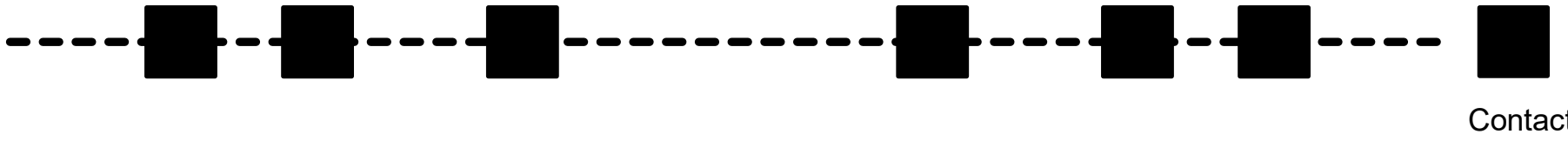
- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact

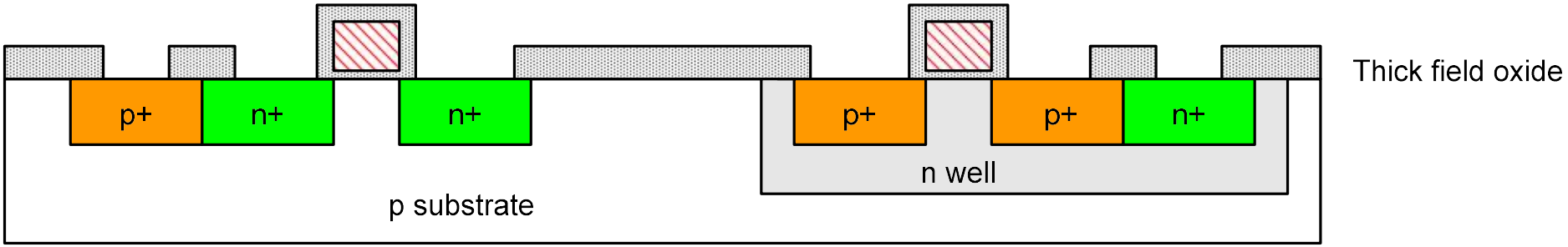




Contacts

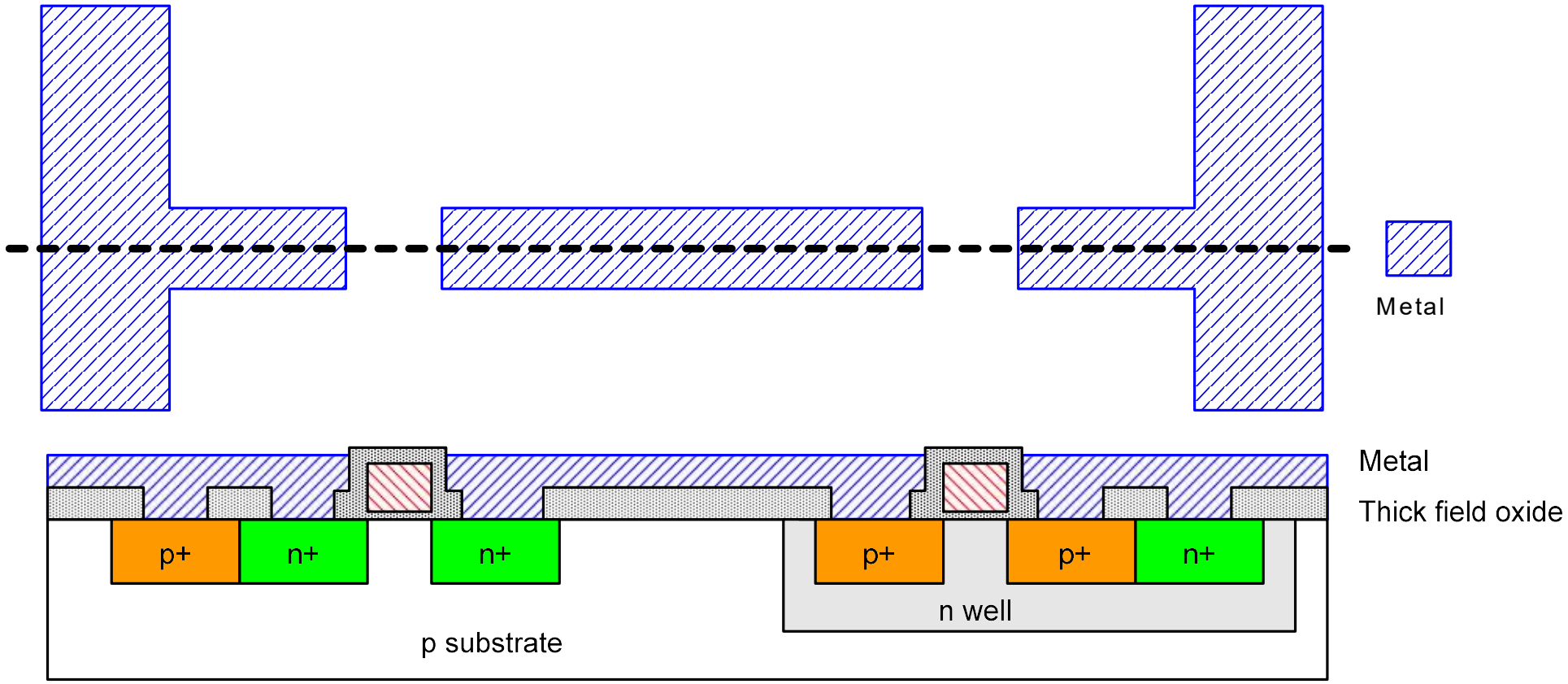
- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed





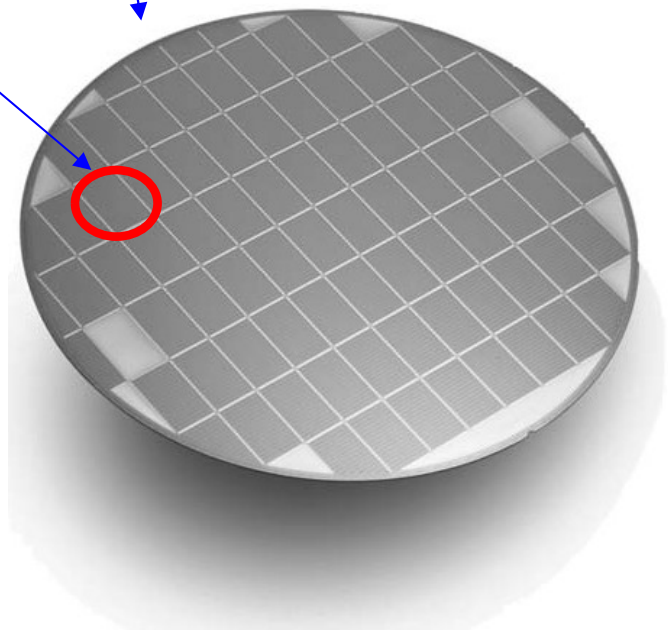
Metalization

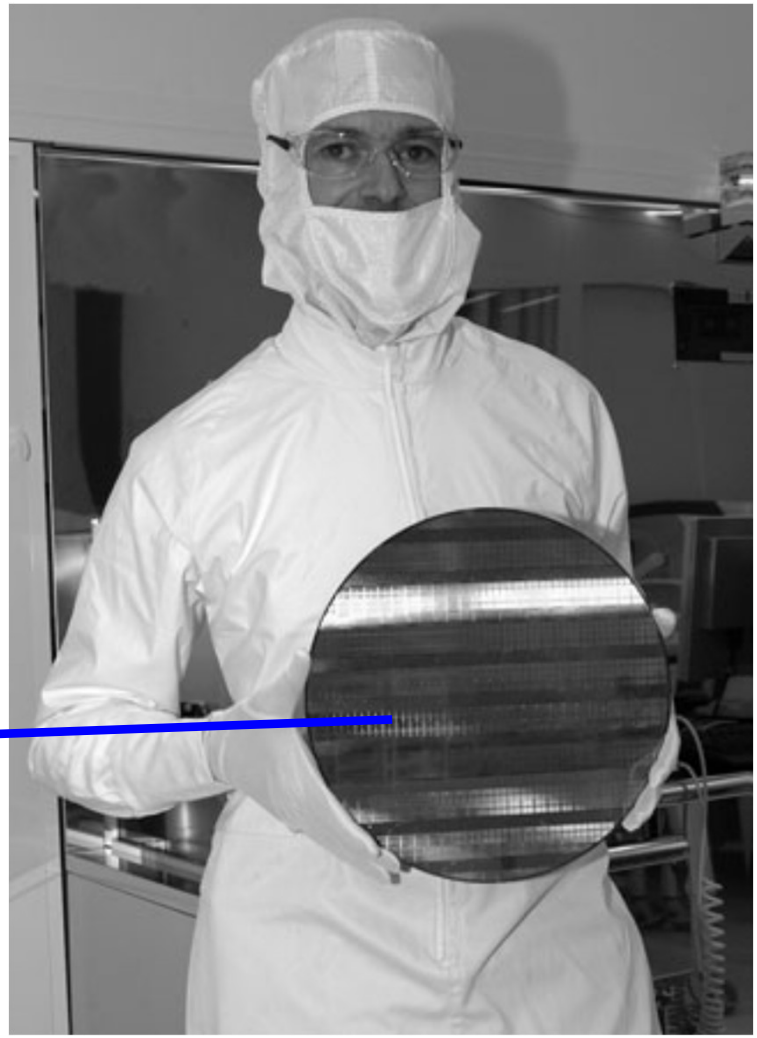
- Sputter aluminum over whole wafer
- Pattern to remove excess metal, leaving wires



Fabrication and Package

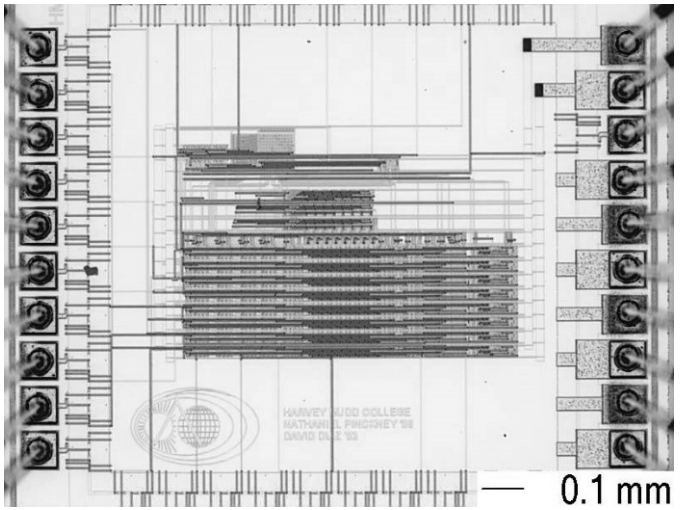
- Tapeout final layout
- Fabrication
  - 6, 8, 12" wafers
  - Cut into individual dice
- A single dust particle or wafer defect kills a die

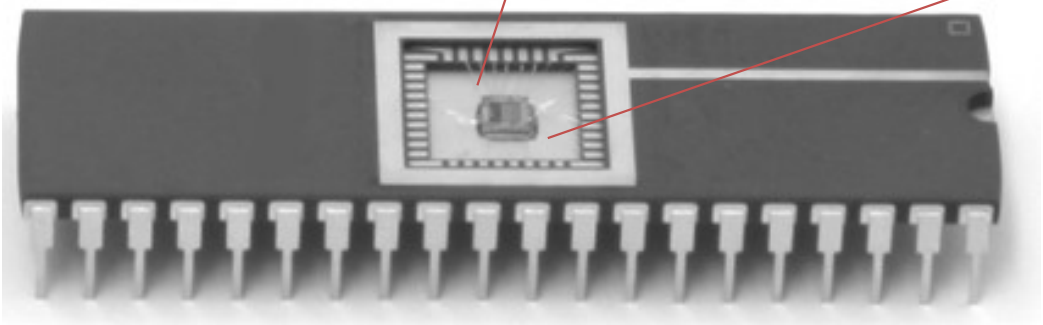




Fabrication and Package

- **Packaging**
  - Bond gold wires from die I/O pads to package
- **Test that chip operates**
  - Design errors
  - Manufacturing errors





Outline

- MOS Transistors
- NMOS vs. CMOS Logic Circuits
- MOS Logic Circuits
- CMOS Fabrication and Layout
- **Summary**

Summary

- Concepts and applications of MOS Transistors in digital designs
  - MOS transistors are stacks of gate, oxide, silicon
  - Act as electrically controlled switches
  - Build logic gates out of switches
- MOS Logic Circuits
  - NMOS Vs. CMOS
  - Basic CMOS logic Circuits
- CMOS Layout and Fabrication
  - Draw masks to specify layout of transistors