	King Saud University **College of Computer and Information Sciences** **Computer Science Department**

Course Code:	CSC 220
Course Title:	Computer Organization
Semester:	Spring 2015-2016
Exercises Cover Sheet:	**Final Exam**

Duration: 2 Hours

Student Name:	
Student ID:	
Student Section No.	

Note: Shaded cells in the table below should be updated by the instructor of the course as needed.

	Computer Science B.Sc. Program: **NCAAA: Intended Learning Outcomes (ILO) Student Outcomes** **ABET: Program Learning Outcomes (PLO) Student outcomes**	**Question No. Relevant Is Hyperlinked**	**Covering %**
NCAAA	**1. Knowledge (NCAAA)** **Suggested verbs (list, name, record, define, label, outline, state, describe, recall, memorize, reproduce, recognize, record, tell, write)**	**Exercise 1 and 2**	$\sum ABET\%$
ABET	**(a) Apply knowledge of computing and mathematics appropriate to the discipline;**		40%
NCAAA	**2. Cognitive Skills (NCAAA)** **Suggested verbs (estimate, explain, summarize, write, compare, contrast, diagram, subdivide, differentiate, criticize, calculate, analyze, compose, develop, create, prepare, reconstruct, reorganize, summarize, explain, predict, justify, rate, evaluate, plan, design, measure, judge, justify, interpret, appraise)**	**Exercise 3, 4, and 5**	$\sum ABET\%$ 60%
ABET	**(b) Ability to analyze a problem, and identify and define the computing requirements appropriate to its solution.**	40%	
	(c) An ability to design, implement and evaluate a computer-based system, process, component, or program to meet desired needs.	20%	

RESULTS					
Note: Shaded cells in the table below should be updated by the instructor of the course as needed.					
Tick the Relevant	**Computer Science B.Sc. Program: NCAAA: Intended Learning Outcomes (ILO) Student Outcomes ABET: Program Learning Outcomes (PLO) Student outcomes**	**Question No. Relevant Is Hyperlinked**	**Covering %**	**Full Mark**	**Student Mark**
NCAAA	**1. Knowledge (NCAAA) Suggested verbs (list, name, record, define, label, outline, state, describe, recall, memorize, reproduce, recognize, record, tell, write)**				
ABET	Outcome (a)	**Question 1**	**25%**	**10**	
		Question 2	**15%**	**6**	
NCAAA	**2. Cognitive Skills (NCAAA) Suggested verbs (estimate, explain, summarize, write, compare, contrast, diagram, subdivide, differentiate, criticize, calculate, analyze, compose, develop, create, prepare, reconstruct, reorganize, summarize, explain, predict, justify, rate, evaluate, plan, design, measure, judge, justify, interpret, appraise)**				
ABET	Outcome (c)	**Question 3**	**20%**	**8**	
	Outcome (b)	**Question 4**	**10%**	**4**	
		Question 5	**30%**	**12**	
		Total		**40**	

Feedback and Remarks:

I certify that the work contained within this assignment is all my own work and referenced where required. **Student Signature:** **Date:**		**Feedback Received:** **Student Signature:** **Date:**

Question 1 [4+6=8 Marks]

1.1 Write T in front the correct statements and F in front the wrong statements:

Statement	T or F
a) One of the advantages of one's complement notation is two representations of zero.	F
b) In two's complement notation, adding **1011** and **1100** causes overflow.	T
c) In two's complement notation, adding **0111** and **1100** gives result **0011**	T
d) Increasing the number of registers in register file will not affect the main memory capacity.	T
e) A program counter (PC) keeps track of the current instruction address.	T
f) In two's complement notation, the binary number **110101** is equivalent to **-21** in decimal.	F
g) In two's complement notation, Sign Overflow is impossible when adding a negative and a positive number.	T
h) Division and Multiplication are often implemented as collections of operations rather than as single micro-ops.	T

1.2 For each statement select the correct choice: [6 Marks]

a) Assembly statement that corresponds to the following RTL statement is : R0 ← 1000

i. LD R0 , #1000
ii. LD (R0) , 1000
iii. LD R0 ,1000
iv. LD (R0) ,#1000

b) Assembly statement that corresponds to the following RTL statement is : M[R0] ←R1

i. ST R1 ,R0
ii. ST R0,R1
iii. ST (R0) , R1
iv. ST (R1) , R0

c) The decimal number 23 may be represented in 2's complement by:

i. 00010111
ii. 01111001
iii. 11101000
iv. 11101001

d) The decimal number -40 may be represented in 2's complement by:

i. 00101000
ii. 10101000
iii. 11011000
iv. 11010111

e) A digital computer has a common bus system for 64 registers of 16 bits each. The bus is constructed with multiplexers. The number of multiplexers are there in the bus is

i. 64
ii. 16
iii. 32
iv. 8

f) A digital computer has a common bus system for 16 registers of 8 bits each. The bus is constructed with three-state gates. The size of decoder is

i. 4x16
ii. 3x8
iii. 5x32
iv. 2x4

g) Digital System

i. is a collection of digital hardware modules contacted via paths .
ii. routes on which information is moved
iii. routes on which control signals moved
iv. are operations on data stored on registers

h) Data path

i. is a collection of digital hardware modules contacted via paths .
ii. routes on which information is moved
iii. routes on which control signals moved
iv. are operations on data stored on registers

i) CPU does not perform the operation .....

i. I/O operations
ii. logic operation
iii. arithmetic operation
iv. addition

j) Where does a computer add and compare data?

i. Hard disk
ii. Floppy disk
iii. CPU chip
iv. Memory chip

k) Which is not valid RTL

i. k: R1 <--- R2, R1 <--- R3
ii. k: R1 <--- R2, R2 <--- R3
iii. k: R1 <--- R2, R2 <--- R1
iv. k: R1 <--- R1, R2 <--- R1

l) Assuming registers are 8-bits width, and R1 = CE, R2 = 6F, R3 = 9F, R4 = FF, ""numbers are represented in HEX and in 2's complement" what is the contents of overflow Flag "V" and Zero Flag "Z" and Carry "C' if the instruction SUB, R1, R1, R4 (in RTL: R1 ← R1 - R4) is executed?

[i] **V = 0, Z = 0, C=0** [ii] V = 1, Z = 0 , C =1
[iii] V = 0, Z = 1, C = 0 [iv] V = 0, Z = 0, C=1

Question 2: Complete the following tables: (4+2=6 Marks)

2.1 Given the following values for A and B in 2's complement notation compute the Addition result and write yes if there will be a sign overflow and no otherwise.

A	B	A+B	Sign Overflow (yes/no)
00000011	11111011	11111110	no
00000011	00000011	00000110	no
11111011	11111100	11110111	no
00000111	00000011	00001010	no

2.2 Consider going form 4 bits to 8 bits for the following numbers in the following different notations.

4-bits	8 bits (Signed magnitude)	8 bits (2's complement)
1100	1000 0100	1111 1100
0011	0000 0011	0000 0011

Question 3[3+5=8 Marks]

3.1 In an **eight-bit** system, write the RTL expression(s) that do the following:

a) Transfer the data from register R0 to R1..

Answer:

R1←R0

b) Increment the value of a word in the memory that its address in R0. (Note: assume no direct access between ALU and Main Memory and between Constants and Main Memory address line).(use the datapath you have studied)

Answer:

R1←M[R0]

R1←R1+1

M[R0]←R1

c) Clear the most significant bit in R5. (i.e. make MSB 0)

Answer:

R5(7)← 0

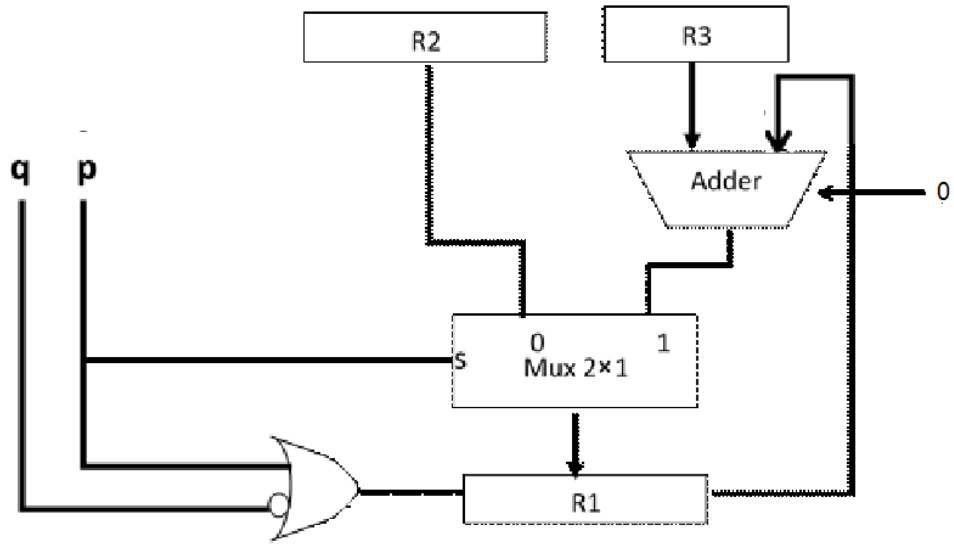
3.2 Design the circuit for the following conditional statement

If (p = 0 and q =0) then R1= R2 else if (p=1) R1= R3 + R1

Answer:

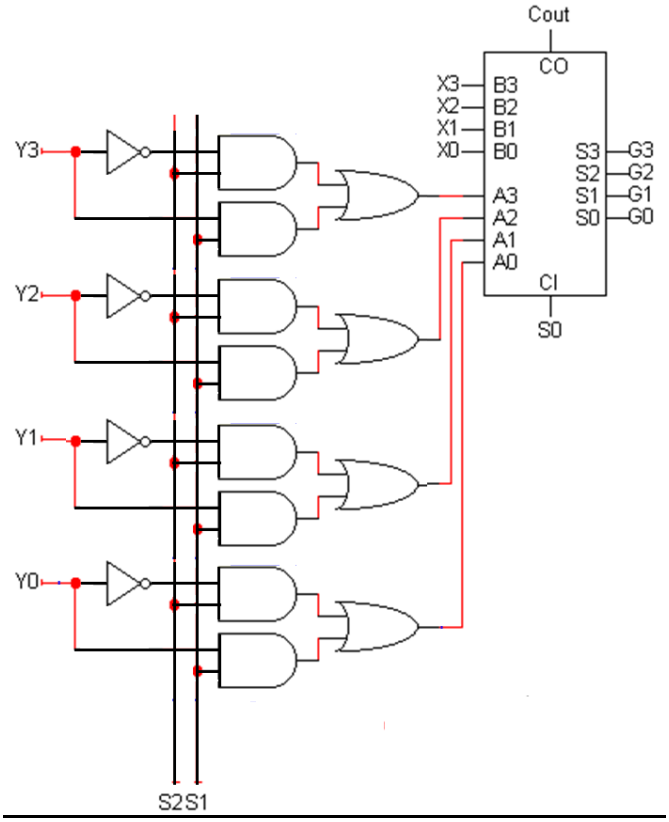
P' ∧ Q': R1 ← R2

P : R1 ← R3 + R1



Question 4 [4 Marks]

4.1 Fill the operation table which describes the functions provided by the following circuit:



S2	S1	S0	G Operation (3 marks)
0	0	1	X +1
0	1	0	Y + X
0	1	1	Y + X +1
1	0	1	Y' + X + 1 (Y-X)
1	1	0	X-1
1	1	1	X

Question 5 [4+8 =12 Marks]

a. What is name of the circuit:(1 mark)

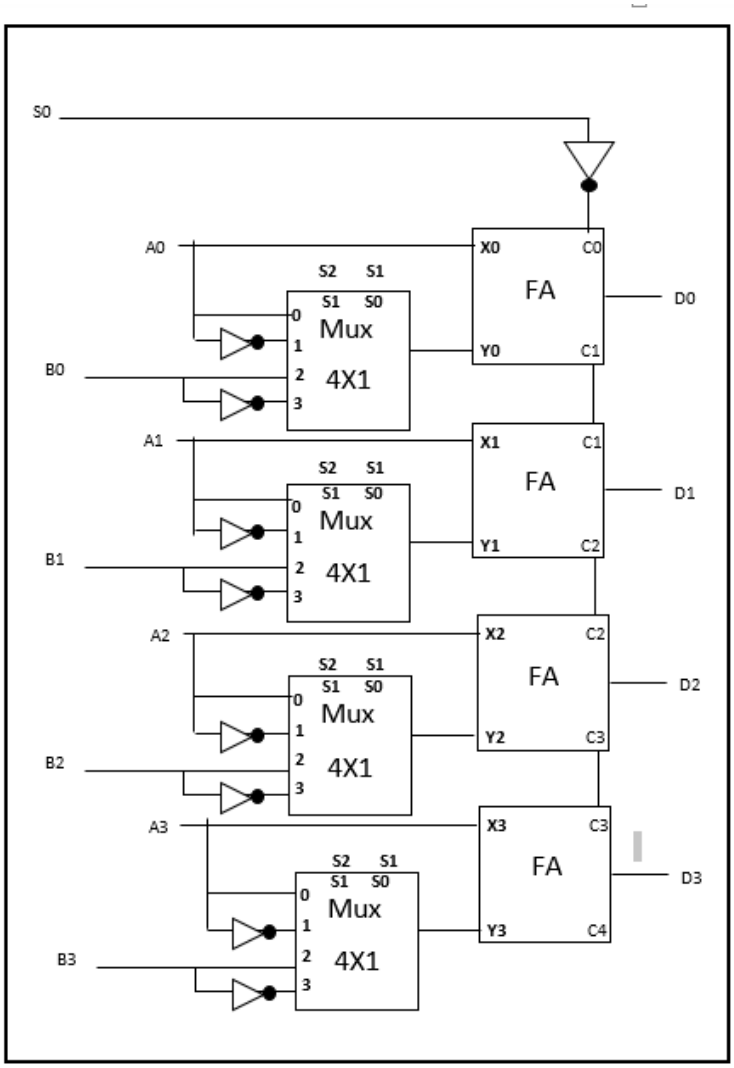
i. Arithmetic circuit

ii. Register

iii. Counter

iv. Decoder

5.1 Fill the operation table which describes the functions provided by the following ALU design:

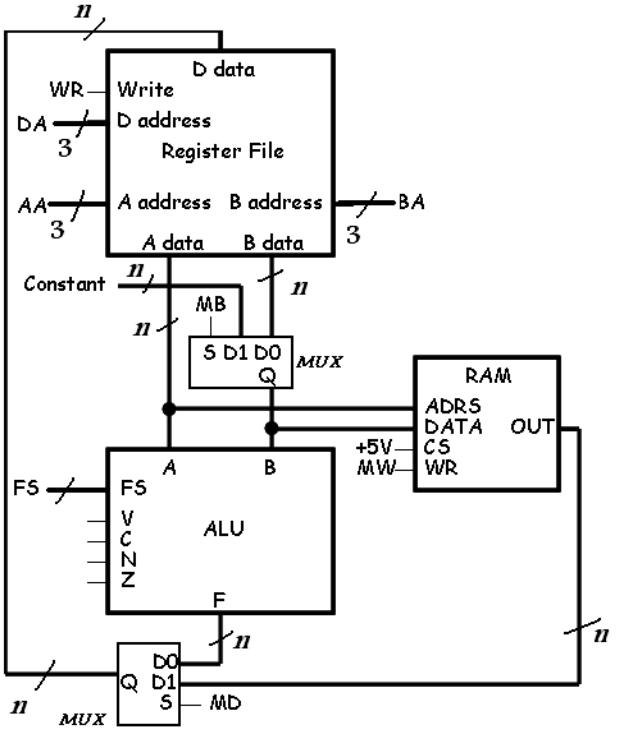


S2	S1	S0	D Operation
0	0	0	D = A+A+1
0	0	1	D = A +A
0	1	0	D = A + A' +1 (=0)
0	1	1	D = A + A' (1's)
1	0	0	D = A +B +1
1	0	1	D = A +B
1	1	0	D = A +B'+1 (A-B)
1	1	1	D = A +B'

5.2 Here is the most basic datapath you have studied (8 Marks)

– The ALU's two data inputs.

– The ALU computes a result, which is saved back to the registers. AA, BA, DA, WR, MB, MD, MW, and FS are control signals. Their values determine the exact actions taken by the datapath, and which registers are used and for what operation.



FS	Operation
0000	F = A
0001	F = A + 1
0010	F = A + B
0011	F = A + B + 1
0100	F = A + B'
0101	F = A + B' + 1
0110	F = A - 1
0111	F = A
1000	F = A ∧ B (AND)
1001	F = A ∨ B (OR)
1010	F = A ⊕ B (XOR)
1100	F = B
1011	F = A'

Fill in the required information in the answer table to perform the following instructions assuming that the registers of 8 bits, and their initial signed 2's complement values were, R0= 0E, R1 = 0F, R2 = 09, R3 = 0B, data in memory as shown, and the initial values of V, C, N, Z were 0's. The required information are:

a. The generated control signals (**AA, BA, DA, WR, MB, MD, MW, FS**) on the diagram to perform the instruction.

b. The values **of V, C, N, and Z status flags** after each instruction.

c. The **contents of memory and registers** after executing the 5 instructions.

```
LD R0, (R3)
LD R3, (R2)
ADD R1, #F0
ST (R2), R1
ST (R1), R3
```

address	memory
09	**20**
0A	**A3**
0B	**21**

FD	**34**
FE	**E4**
FF	**71**

Answer (fill in the information needed in place of dots**)**

Each row 0.5 marks								Each row 0.5 marks				Each row 0.5 marks
AA	**BA**	**DA**	**WR**	**MB**	**MD**	**MW**	**FS**	**V**	**C**	**N**	**Z**	**Instruction in RTL**
011	XXX	000	1	X	1	0	XXXX					LD R0, (R3)
												R0 ← M[R3]
010	**xxx**	**011**	**1**	**x**	**1**	**0**	**xxxx**					LD R3, (R2)
												… R3 ← M[R2]
001	**xxx**	**001**	**1**	**1**	**0**	**0**	**0010**	**0**	**0**	**1**	**0**	ADD R1, #F0
												R1 ← R1 + F0
010	**001**	**xxx**	**0**	**0**	**x**	**1**	**xxxx**					ST (R2), R1
												M[R2] ← R1
001	**011**	**xxx**	**0**	**0**	**x**	**1**	**xxxx**					ST (R1), R3
												M[R1] ← R3

The contents of Registers and Memory are as shown: (0.5 marks each)

R0= 21

R1 = FF

R2 = 09

R3 = 20

memory

address	
09	**FF**
0A	**A3**
0B	**21**
FD	**34**
FE	**E4**
FF	**20**

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