King Saud University
College of Computer and Information Sciences
Computer Science Department

Course Code:	CSC 220
Course Title:	Computer Organization
Semester:	Fall 2018
Exercises Cover Sheet:	**Final Exam**
Duration: 3 hours	

Student Name:	
Student ID	
Student Serial No.	

	Computer Science B.Sc. Program: **NCAAA: Intended Learning Outcomes (ILO) Student Outcomes** **ABET: Program Learning Outcomes (PLO) Student outcomes**	**Question No. Relevant Is Hyperlinked**	**Covering %**
NCAAA	**1. Knowledge (NCAAA)** **Suggested verbs (list, name, record, define, label, outline, state, describe, recall, memorize, reproduce, recognize, record, tell, write)**	**Exercise**	$\sum ABET\%$
ABET	**(a) Apply knowledge of computing and mathematics appropriate to the discipline;**	1	25%
NCAAA	**2. Cognitive Skills (NCAAA)** **Suggested verbs (estimate, explain, summarize, write, compare, contrast, diagram, subdivide, differentiate, criticize, calculate, analyze, compose, develop, create, prepare, reconstruct, reorganize, summarize, explain, predict, justify, rate, evaluate, plan, design, measure, judge, justify, interpret, appraise)**	**Exercise**	$\sum ABET\%$
ABET	**(b) Ability to analyze a problem, and identify and define the computing requirements appropriate to its solution.**	2	30 %
	(c) An ability to design, implement and evaluate a computer-based system, process, component, or program to meet desired needs.	3 & 4	45%

RESULTS					
Note: Shaded cells in the table below should be updated by the instructor of the course as needed.					
Tick the Relevant	**Computer Science B.Sc. Program: NCAAA: Intended Learning Outcomes (ILO) Student Outcomes ABET: Program Learning Outcomes (PLO) Student outcomes**	**Question No. Relevant Is Hyperlinked**	**Covering %**	**Full Mark**	**Student Mark**
NCAAA	**1. Knowledge (NCAAA) Suggested verbs (list, name, record, define, label, outline, state, describe, recall, memorize, reproduce, recognize, record, tell, write)**		$\sum ABET$		
ABET	Outcome (a)	**1**		**10**	
NCAAA	**2. Cognitive Skills (NCAAA) Suggested verbs (estimate, explain, summarize, write, compare, contrast, diagram, subdivide, differentiate, criticize, calculate, analyze, compose, develop, create, prepare, reconstruct, reorganize, summarize, explain, predict, justify, rate, evaluate, plan, design, measure, judge, justify, interpret, appraise)**		$\sum ABET$		
ABET	Outcome (b)	**2**		**12**	
	Outcome (c)	**3**		**8**	
		4		**10**	
		Total		**40**	
Feedback and Remarks:					
I certify that the work contained within this assignment is all my own work and referenced where required. Student Signature: Date:			**Feedback Received: Student Signature: Date:**		

Exercise (1): (5+5 = 10 points)

A. Choose the correct answer (0.5/each):

Note: fill your answers in the table below.

1	2	3	4	5	6	7	8	9	10
c	d	a	b	d	c	d	b	a	a

1. The decimal number **-5** may be represented in 2's complement by:

   a) 1010
   b) 0101
   c) 1011
   d) 1101

2. The decimal number **-40** may be represented in 1's complement by:

   a) 00101000
   b) 10101000
   c) 11011000
   d) 11010111

3. The decimal number **23** may be represented in 2's complement by:

   a) 00010111
   b) 01111001
   c) 11101000
   d) 11101001

4. The equivalent hexadecimal number for the binary number 0101001 is:

   a) 52
   b) 29
   c) 49
   d) 51

5. How many selection lines are required in **16x1** MUX?

   a) 1
   b) 2
   c) 3
   d) 4

6. 16-bit binary machine codes for **M[R1] ←R3** Instruction (see **Table1** below)

   a) 0100000 001 011 000
   b) 0010000 011 001 011
   c) 0100000 000 001 011
   d) 0010000 000 011 001

7. The register file, function unit and the interconnection between them is called _____

   a) Compiler.
   b) Control Unit.
   c) Information path.

d) Data path.

8. A circuit of size 1x8 can be :

a) Multiplexer
b) Demultiplexer
c) Decoder
d) Encoder

9. If a register containing data (1100110) is subjected to **circular left shift** operation, then the content of the register will be

a) 1001101
b) 0110011
c) 1001100
d) 0110010

10. Assembly statement that corresponds to the following RTL statement is :

R0 ← 1000

a) LDI R0 , 1000
b) LD (R0) , 1000
c) LDI 1000,R0
d) LD (R0) ,#1000

Table1: **Instruction Specifications for the Simple Computer**

Instruction	Opcode	Mnemonic	Format	Description	Status Bits
Move A	0000000	MOVA	RD, RA	R[DR] ← R[SA]*	N, Z
Increment	0000001	INC	RD, RA	R[DR] ← R[SA] + 1*	N, Z
Add	0000010	ADD	RD, RA, RB	R[DR] ← R[SA] + R[SB]*	N, Z
Subtract	0000101	SUB	RD, RA, RB	R[DR] ← R[SA] − R[SB]*	N, Z
Decrement	0000110	DEC	RD, RA	R[DR] ← R[SA] − 1*	N, Z
AND	0001000	AND	RD, RA, RB	R[DR] ← R[SA] ∧ R[SB]*	N, Z
OR	0001001	OR	RD, RA, RB	R[DR] ← R[SA] ∨ R[SB]*	N, Z
Exclusive OR	0001010	XOR	RD, RA, RB	R[DR] ← R[SA] ⊕ R[SB]*	N, Z
NOT	0001011	NOT	RD, RA	R[DR] ← $\overline{R[SA]}$*	N, Z
Move B	0001100	MOVB	RD, RB	R[DR] ← R[SB]*	
Shift Right	0001101	SHR	RD, RB	R[DR] ← sr R[SB]*	
Shift Left	0001110	SHL	RD, RB	R[DR] ← sl R[SB]*	
Load Immediate	1001100	LDI	RD, OP	R[DR] ← zf OP*	
Add Immediate	1000010	ADI	RD, RA, OP	R[DR] ← R[SA] + zf OP*	N, Z
Load	0010000	LD	RD, RA	R[DR] ← M[SA]*	
Store	0100000	ST	RA, RB	M[SA] ← R[SB]*	
Branch on Zero	1100000	BRZ	RA, AD	if (R[SA] = 0) PC ← PC + se AD, if (R[SA] ≠ 0) PC ← PC + 1	N, Z
Branch on Negative	1100001	BRN	RA, AD	if (R[SA] < 0) PC ← PC + se AD, if (R[SA] ≥ 0) PC ← PC + 1	N, Z
Jump	1110000	JMP	RA	PC ← R[SA]*	

* For all of these instructions, PC ← PC + 1 is also executed to prepare for the next cycle.

B. True or False (0.5/each)

Note: fill your answers in the table below.

1	2	3	4	5	6	7	8	9	10
F	T	T	F	F	T	F	F	T	F

Statement	True/False
1. The sign extension for the 2's complement binary number 1011 is: 0000 1011	
2. A program counter (PC) keeps track of the address of the next instruction in memory.	
3. In the Register File, data is written only on the positive edge of the clock.	
4. One of the advantages of one's complement notation is two representation of zero.	
5. The control unit is responsible for generating statues bits in the CPU.	
6. In the Register File, two registers can be read at once because most arithmetic operations require two operands.	
7. In ALU, a Decoder is used to determine whether the final result comes from the arithmetic or logic unit.	
8. In two's complement notation, Sign Overflow is possible when adding a negative and a positive number.	
9. Kmaps provide an easy graphical method of simplifying Boolean expressions.	
10. In sequential circuits, the output depends only on the present values of the input.	

Exercise (2): (2+2+2+3+3=12 points)

A. Consider a program consists of following instructions and assume that the contents of 8-bit registers are (in HEX): R0=0D, R1=0C, R2= 0B, R4=8F, R5=01, R6=0C. What are the contents of the **registers** after execution of the program (select correct answers and write them in the table below)?

LD R6, (R1)

ADD R1, R4, #0F

INC R0, R1

1. Register R6 contains
   a) A3 b) 30 c) 21 d) 0C
2. Register R1 contains
   a) 8F b) 9E c)E1 d) 0C
3. Register R0 contains
   a) 9F b) EC c) 0D d) 0C
4. Register R4 contains
   a) EC b) 8F c) 21 d) 0C

memory

address	
0B	**30**
0C	**A3**
0D	**21**

Note: fill your answers in the table below.

1	2	3	4
a	b	a	b

B) For a **128X64** Random Access Memory. (2 points)

How many words are in this RAM?	128 (0.5)
What Is the total storage capacity in KB?	١ (0.5)
How many bit in each word?	64 (0.5)
How many address lines in this RAM?	7 (0.5)

C) A digital computer has a common bus system for **16** registers of **8** bit each. The bus is constructed with multiplexers. (2 points)

How many selection inputs are there in each multiplexer?	4 (0.5)
What size of multiplexers is needed?	16x1 (.75)
How many multiplexers are the in the bus?	8 (.75)

D) Given the following values for **A** and **B** in 2's complement notation, complete the following tables (3 points, 0.5/each)

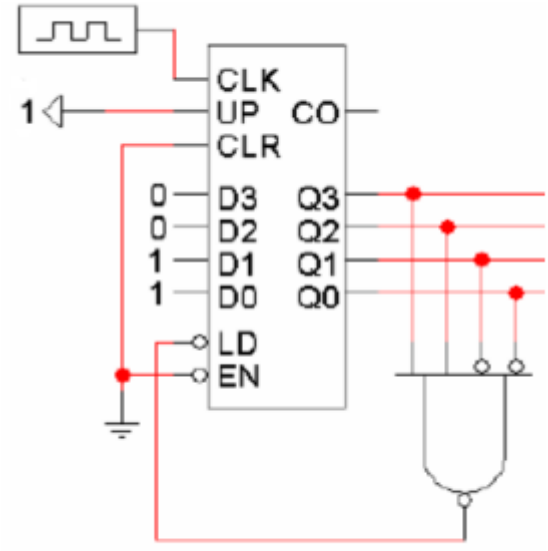
A	B	Operation	Result
0011	1011	A+B	**1110**
0011	1011	Rotate right of B	**1101**
1011	1100	Extends A to 8 bit representation	**1111 1011**
1001	0011	A ⊕ B	**1010**
0011	1001	Arithmetic right of A	**0001**
0001	0111	Overflow result after (A+B)	**V = 1**

E) Complete the following table, giving the instruction in binary for the single-cycle computer that executes the register transfer (if any field is not used, give it the value 0)؛ **(0.75/each)**

No.	Instruction	Opcode	DR	SA	SB or Operand
1	SHR R3 , R5	0001101	011	000	101
2	INC R1, R2	0000001	001	010	000
3	SUB R4, R5, R4	0000101	100	101	100
4	JMP R1	1110000	000	001	000

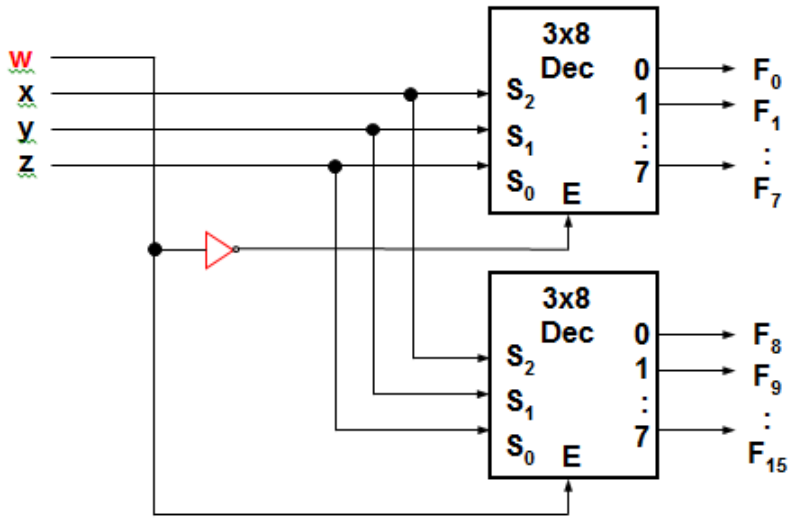
Exercise (3): (2.5+3+2.5=8 points)

1. Using the circuit below, design a counter that counts the following cycle: 3, 4, 5, 6, 7, 8, 9, 10, 11, 12



0.25 up=1
1 for parallel load (0.25 each)
1 for end value 12 and use nand (if use and -0.25)
0.25 for connect nand to LD
Total 2.5

1) Construct a **4x16** decoder from **two 3x8** decoders with 1-enable**.**



.75 for using most significant bit as enable

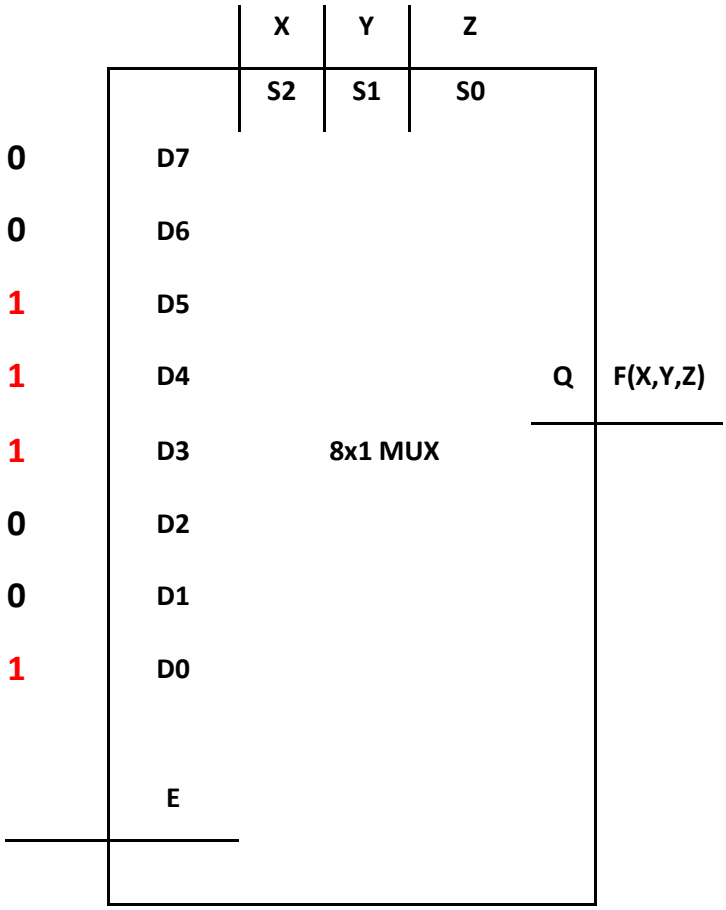
(1.5)-->.25 for conecting inputs correclty for each decoder (1.5)

0.5 labelling output correctly (F0-F7 when W is 0, F8-F15when W is 1,)

.25 for label decoder information

Total 3

2) Assume we want to implement a function **F(X, Y, Z)** = Π **M** (1, 2, 6, 7).
Show how to implement the function F using only one line multiplexer.



2--> .25 for each input (0, 1)

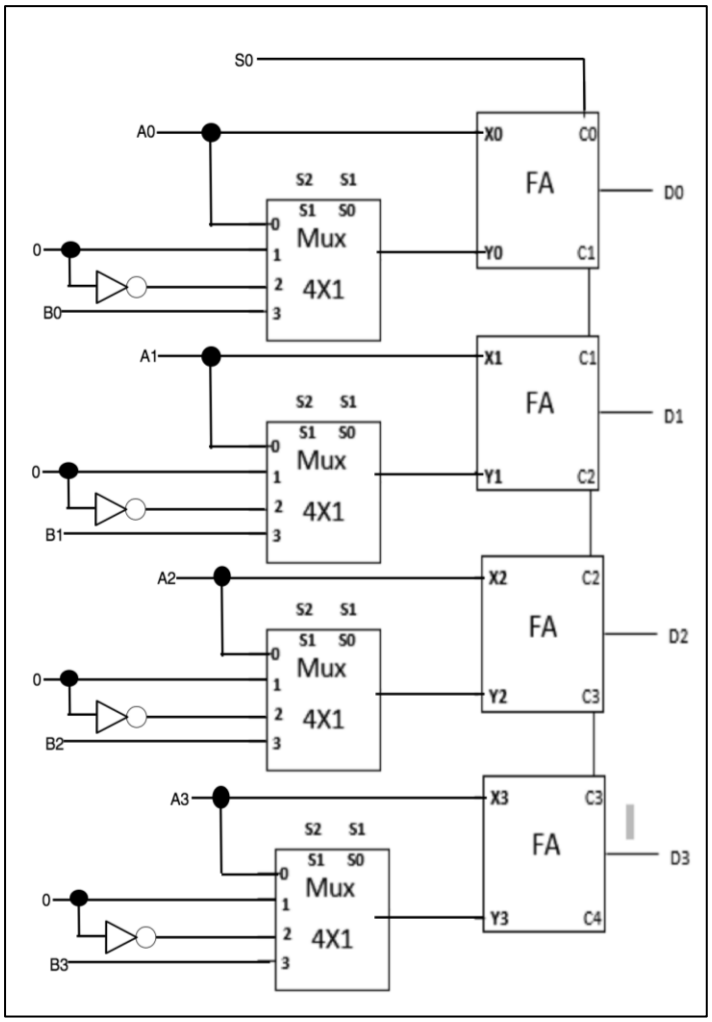
.25 for selection

.25 for using 8X1 Mux

Total 2.5

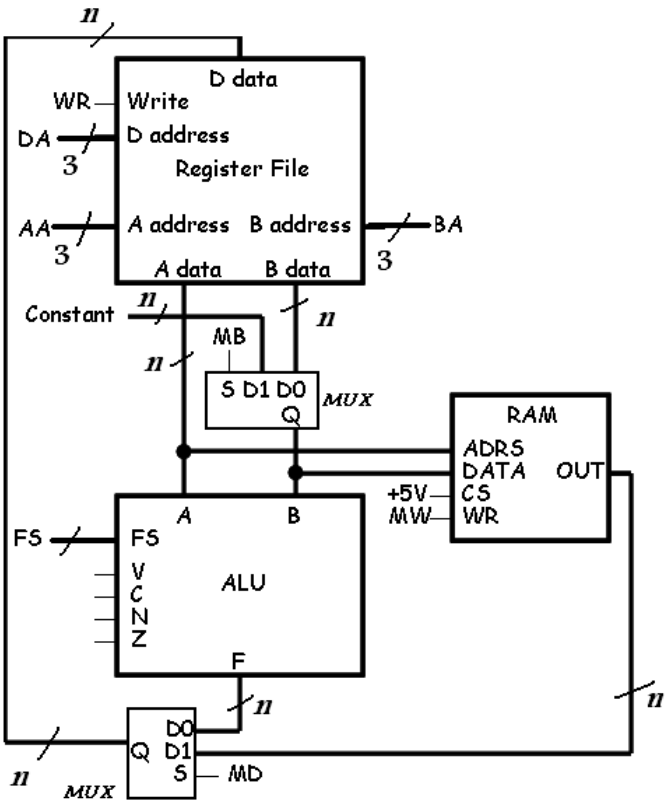
Exercise (4): (5+5=10 points)

A. Fill the operation table which describes the functions provided by the following ALU design:



S2	S1	S0	D Operation	
0	**0**	**0**	D= A+A	**.5**
0	**0**	**1**	D=A+A+1	**.75**
0	**1**	**0**	D=A	**.5**
0	**1**	**1**	D=A+1	**.75**
1	**0**	**0**	D=A-1	**.5**
1	**0**	**1**	D=A	**.75**
1	**1**	**0**	D=A+B	**.5**
1	**1**	**1**	D=A+B+1	**.75**
			Total	٥

Here is the most basic datapath you have studied. The ALU has two data inputs. The ALU computes a result, which is saved back to the registers. The control signals values determine the exact actions taken by the datapath, and which registers are used and for what operation.



FS	Operation
0000	F = A
0001	F = A + 1
0010	F = A + B
0011	F = A + B + 1
0100	F = A + B'
0101	F = A + B' + 1
0110	F = A - 1
0111	F = A
1000	F = A ∧ B (AND)
1001	F = A ∨ B (OR)
1010	F = A ⊕ B (XOR)
1100	F = B
1011	F = A'

B. Fill the below table with the generated control signals (**AA, BA, DA, WR, MB, MD, MW, FS**) to perform each of the following RTL instruction (USE R6 as temporary register if needed)

1. R4←R2-R1
2. R7← R7+1
3. M[R0]←R1
4. R5← M[R3]+5

AA	BA	DA	WR	MB	MD	MW	FS	RTL
٠١٠	٠٠١	١٠٠	١	٠	٠	٠	٠١٠١	R4←R2-R1
١١١	XXX	١١١	١	X ١	٠	٠	٠٠٠١ ٠٠١٠	R7← R7+1
٠٠٠	٠٠١	XXX	٠	٠	X	١	XXX	M[R0]←R1
٠١١	XXX	١١٠	١	X	١	٠	XXX	R6← M[R3]
١١٠	XXX	١٠١	١	١	٠	٠	٠٠١٠	R5← R6+5
.125 for each								٥

This page is a draft and will not be graded under any circumstance