King Saud University
College of Computer and Information Sciences
Department of Computer Science

CSC 220: Computer Organization

Tutorial 12: CPU Programming

Q1: MCQ (Which is true in the following questions)

I. Where does a computer add and compare data?

A) Hard disk C. Floppy disk
B) CPU chip D:Memory chip

ANSWER: (B)

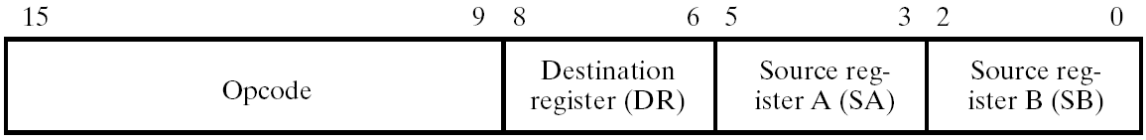
II. Which of the following registers is used to keep track of address of the memory location where the next instruction is located?

A) Memory Address Register
B) Memory Data Register
C) Instruction Register
D) Program Counter

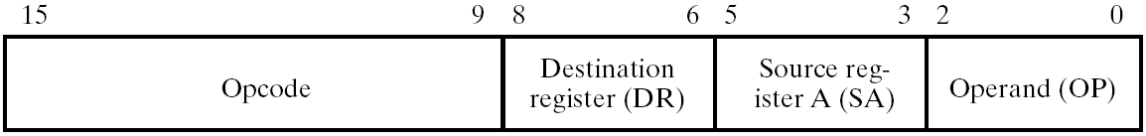
ANSWER: (D)

Q2: Specify for the following three instruction formats for 16-bit instructions: i) Register, ii) immediate, iii) Jump and branch.

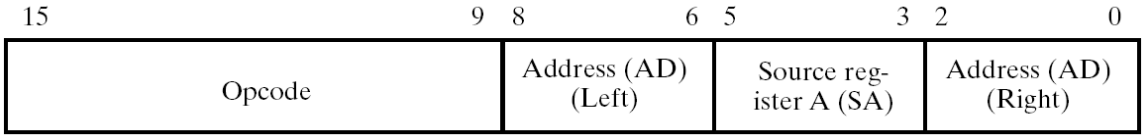
i. Register



ii. Immediate

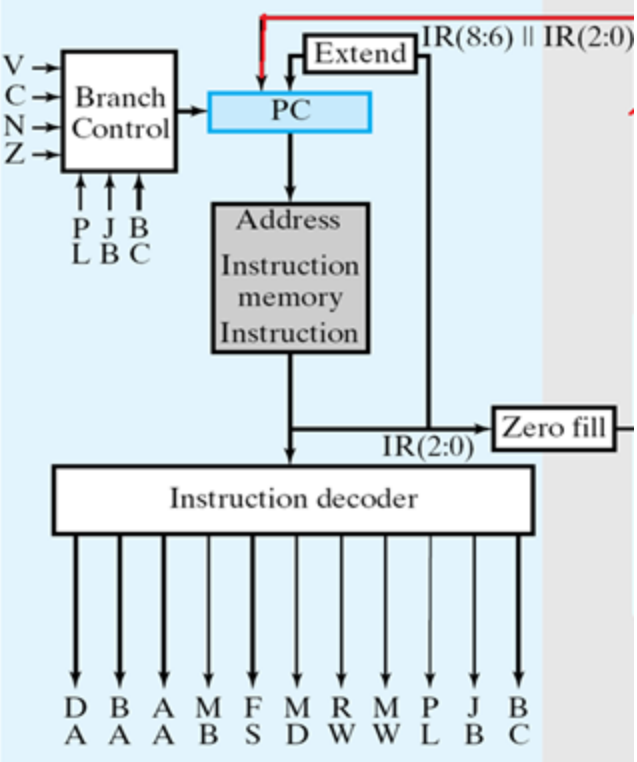


iii. Jump and Branch



Q3. Give the block diagram of a single cycle hardwired control Unit.

Solution:



Q4. Consider table 8-8 containing instruction specification for a simple computer. Translate the following instructions into 16-bit binary machine codes

Solution:

Instruction	**Binary machine code**
ADD R3, R2, R3	**0000010 011 010 011**
LD R5, (R1)	**0010000 101 001 000**
LDI R7, 5	**1001100 111 000 101**
BRN R4 AD (AD = 100 001)	**1100001 100 100 001**

TABLE 8-8
Instruction Specifications for the Simple Computer

Instruction	Opcode	Mnemonic	Format	Description	Status Bits
Move A	0000000	MOVA	RD, RA	R[DR] ← R[SA]*	N, Z
Increment	0000001	INC	RD, RA	R[DR] ← R[SA] + 1*	N, Z
Add	0000010	ADD	RD, RA, RB	R[DR] ← R[SA] + R[SB]*	N, Z
Subtract	0000101	SUB	RD, RA, RB	R[DR] ← R[SA] − R[SB]*	N, Z
Decrement	0000110	DEC	RD, RA	R[DR] ← R[SA] − 1*	N, Z
AND	0001000	AND	RD, RA, RB	R[DR] ← R[SA] ∧ R[SB]*	N, Z
OR	0001001	OR	RD, RA, RB	R[DR] ← R[SA] ∨ R[SB]*	N, Z
Exclusive OR	0001010	XOR	RD, RA, RB	R[DR] ← R[SA] ⊕ R[SB]*	N, Z
NOT	0001011	NOT	RD, RA	R[DR] ← $\overline{R[SA]}$*	N, Z
Move B	0001100	MOVB	RD, RB	R[DR] ← R[SB]*	
Shift Right	0001101	SHR	RD, RB	R[DR] ← sr R[SB]*	
Shift Left	0001110	SHL	RD, RB	R[DR] ← sl R[SB]*	
Load Immediate	1001100	LDI	RD, OP	R[DR] ← zf OP*	
Add Immediate	1000010	ADI	RD, RA, OP	R[DR] ← R[SA] + zf OP*	N, Z
Load	0010000	LD	RD, RA	R[DR] ← M[SA]*	
Store	0100000	ST	RA, RB	M[SA] ← R[SB]*	
Branch on Zero	1100000	BRZ	RA, AD	if (R[SA] = 0) PC ← PC + se AD, if (R[SA] ≠ 0) PC ← PC + 1	N, Z
Branch on Negative	1100001	BRN	RA, AD	if (R[SA] < 0) PC ← PC + se AD, if (R[SA] ≥ 0) PC ← PC + 1	N, Z
Jump	1110000	JMP	RA	PC ← R[SA]*	

* For all of these instructions, PC ← PC + 1 is also executed to prepare for the next cycle.

Q5: Assume that variable x is located at the address 283 in data memory contains 5, and variable y is located at the address 284 contains 10. Write an assembly language program to evaluate the equation $z = y + (x - 3)$ where variable z is located at the address 285.

Solution:

```
LDI   R3, 283
LD    R1, (R3)
LDI   R2, 3
SUB   R1, R1, R2

INC   R3, R3
LD    R2, (R3)
ADD   R2, R2, R1

INC   R3, R3
ST    (R3), R2
```