King Saud University College of Computer and Information Sciences Computer Science Department			
Course Code	CSC 220		
Course Title	Computer Organization		
Semester	S2 – 1440/1441 (Sprint-2019-20)		
Exam	Final		
Date	12/05/2020	**Duration**	**3 Hours**
Student's Name			
Student ID			
Section No.			

Course Learning Outcomes		**Relevant question**	**Full mark**	**Student mark**
Knowledge	**CLO 1, 2, 3**	**1**	**4**	
Knowledge	**CLO 4, 5, 6, 7**	**2**	**4**	
Cognitive Skills	**CLO 2, 3, 5**	**3**	**3**	
Cognitive Skills	**CLO 4, 5**	**4**	**3**	
Cognitive Skills	**CLO 3, 5**	**5**	**3**	
Cognitive Skills	**CLO 3, 6, 7**	**6**	**3**	

Instructions (read them carefully before solving questions):

1. This question paper is in Microsoft Word Document (.docx) format. You may use Microsoft Word or any other method to prepare you answers.
2. Write your Name, ID, and Section # on the top of each page.
3. Solve all the questions and insert the solutions in the space provided. You may extend the space to accommodate your solutions. However, solution provide in other locations will not be considered.
4. After writing/inserting all your solutions, **convert the paper into PDF, check your PDF file carefully, and submit it on LMS**.
5. **Plagiarism (copying others) is strictly prohibited.** All such solution will obtain a zero (0) score.
6. Thirty (30) additional minute will be given to complete the submission process. All submission must be done within this time. **Any late submission will not be accepted**.

Feedback/Comments:

Question 1. (4 Marks) multiple choice

1	2	3	4	5	6	7	8

1- In ------- circuits, applying the same input always produce the same output

A. Sequential

B. Combinational

C. Flipflops

D. Latch

2- 1 bit adder can be converted to adder/ subtractor by

A. Adding 1 OR gate

B. Adding 1 XOR gate

C. Adding 2 OR gate

D. Adding 2 XOR gate

3- The only situation where overflow can never occur is

A. Adding 2 positive numbers

B. Adding 2 negative numbers

C. Adding a positive to negative number

D. It is impossible to guarantee that

4- The demultiplexer can be used to implement any sum of minterms expression

A. True

B. False

5- The arithmetic unite is basically an (Adder/subtractor) circuit plus

A. Decoder

B. Encoder

C. Multiplexer

D. Demultiplexer

6- The advantage of the combinational shifter over the bidirectional shift register is

A. It stores the value

B. It is faster

C. More accurate

D. Uses zero as the defaulter serial input

7- In a 2^3 x 4 register file we use ---------- to read from the register

A. 4x1 Mux

B. 8x1 Mux

C. 3x8 Decoder

D. 2x4 Decoder

8- Which component of the control unite contain the current instruction being executed

A. Program counter (PC)

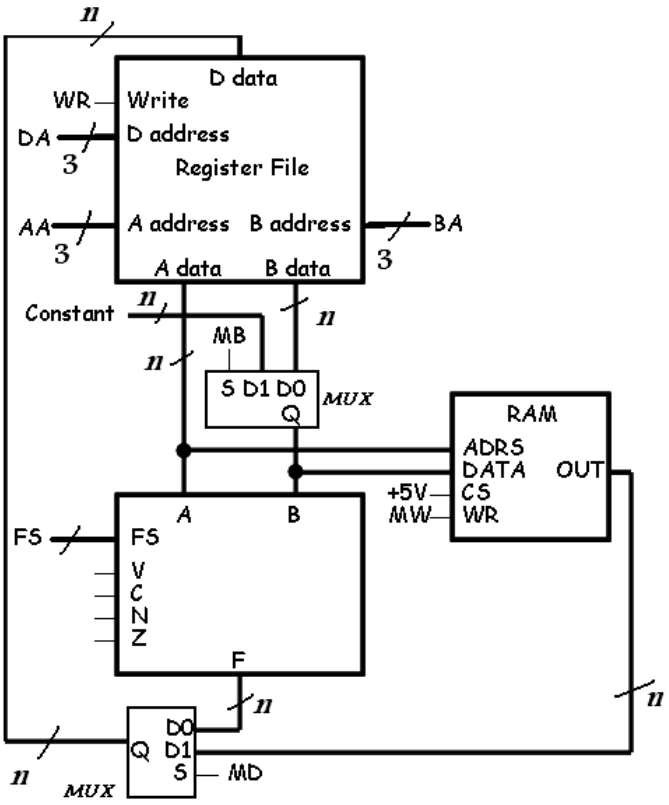
B. Instruction register (IR)

C. Branch control

D. Register file

Question 2. (4 Marks)

Here is the basic datapath + RAM you have studied. The control signals values determine the operation taken is also provided.



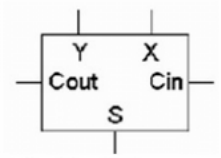
FS	Operation
0000	F = A
0001	F = A + 1
0010	F = A + B
0011	F = A + B + 1
0100	F = A + B'
0101	F = A + B' + 1
0110	F = A - 1
0111	F = A
1000	F = A ∧ B (AND)
1001	F = A ∨ B (OR)
1010	F = A ⊕ B (XOR)
1011	F = A'
1100	F = B
1101	F = sr B (shift right)
1110	F = sl B (shift left)

Fill the below table with the generated control signals (**AA, BA, DA, WR, MB, MD, MW, FS**) to perform each of the following RTL instruction (Use XXX in case you don't care what is the value of this control signal)

AA	BA	DA	WR	MB	MD	MW	FS	RTL
								R3←R4-R2
								R6←sl R4
								M[R1]←R0
								R5 ← 2

Question 3 (3 Marks)

Use Full adders (FAs) as the one shown below to construct 3-bit parallel adder-subtractor with over-flow detection.



Full adder (FA)

And perform the binary addition A − B , where A = 1 and B = -3 , show the values of the inputs and the outputs of this circuit

Question 4 (3 Marks)

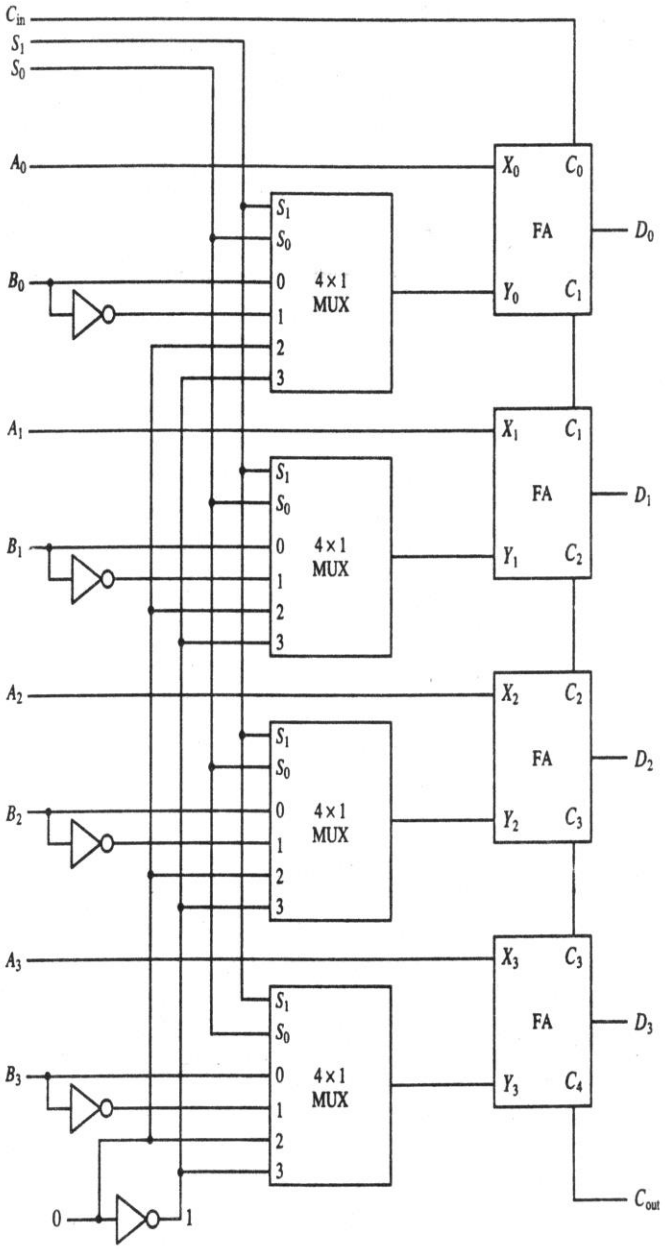
Assuming registers are **8-bits** width, and **R0** = 0F, **R1** = 7D, **R2** = 1F, **R3** = 1B, **R4**= 15 and **PC** = AA "numbers are represented in HEX and in 2's complement" what is the contents of the registers after the following program is executed?

```
ST (R1), R2
INC R0, R3
SUB R3, R1, R2
ADI R4, R2, 3
BRZ R2, AD          Note: (AD = 2)
```

R0	R1	R2	R3	R4	PC

Question 5 (3 Marks)

Analyze the following circuit and fill in the accompanied table to show the correct selection for the operations.



S1	S0	Cin	output	Operation
			A+B	Add
			A-B	Subtraction in 2's
			A+1	Increment A
			A-1	Decrement A

Question 6 (3 Marks)

Fill the following table

How many selection lines are required in 8x1 MUX?	
How many selection lines are required in 4x16 DECODER?	
To implement F(W,X,Y,Z)= m3 +m12 using a multiplexer, what is the size of this multiplexer?	
To implement F(W,X,Y,Z)= m3 +m12 using a decoder, what is the size of this decoder ?	
How many 2-1 multiplexers you need to design 4-1 multiplexer?	
How many 3-8 decoders you need to design 4-16 decoder?	

THE END