King Saud University
College of Computer and Information Sciences
Computer Science Department

Course Code	CSC 220		
Course Title	Computer Organization		
Semester	S1 – 1442 (Fall-2020-21)		
Exam	Midterm 1		
Date	15/10/2020	**Duration**	**90 minutes**
Student Name			
Student ID			
Section No.			

Course Learning Outcomes		**Relevant question**	**Full mark**	**Student mark**
Knowledge	**CLO 1, 2, 4**	**1**	**9**	
Cognitive Skills	**CLO 1, 2**	**2**	**8**	
Cognitive Skills	**CLO 1, 2, 4**	**3**	**8**	
Total			**25**	

Feedback/Comments:

Question 1. (2+2+1+2+2)

(a) Perform the following conversions:

i. $(101101.11)_2 = (0100\ 0101.\ 0111\ 0101)_{BCD}$

ii. $(0101\ 0001\ 0011.0101)_{BCD} = (201.8)_{16}$

(b) Using truth table, show that A ⊕ B is logically equivalent to A′B+AB′.

A	B	A ⊕ B	A'B	AB'	A'B+AB'
0	0	0	0	0	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

So A ⊕ B and A′B+AB′. Both are logically same.

(c) Write smallest and largest decimal number that can be represented in 2's complement notation using 8 bits.

Smallest number is: -128

Largest number is : 127

(d) What will be the decimal value for the binary number 1011 0110 when it is represented in the following systems?

i. Signed Magnitude representation Ans. -54

ii. Two's complements representation Ans. -74

(e) What is a full adder? Give the truth table for a full adder.

Three input bits addition to generate sum and carry bit is called full adder.

X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

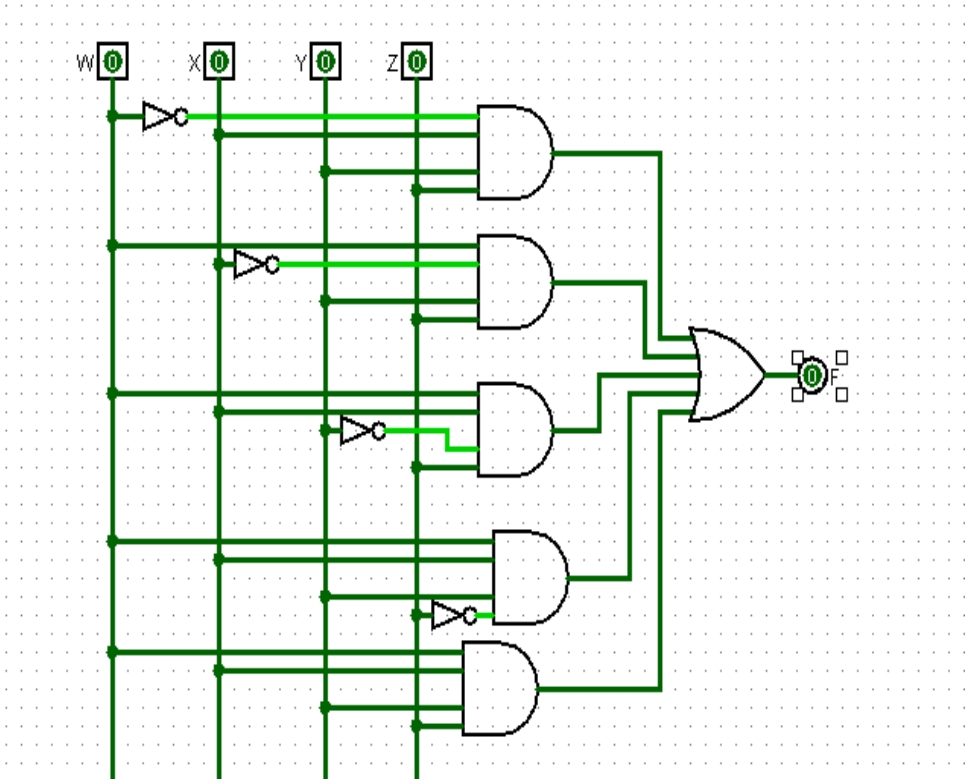
Question 2 (8 Marks: 4+4)

(a) A majority function is generated in a combinational circuit when the output is equal to 1 if the input variables have more 1's than 0's, the output is 0 otherwise.

i. Give truth table **four-input** majority function
ii. Write the output expression in SOP form (without simplification)
iii. Draw the logic circuit.

W	X	Y	Z	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

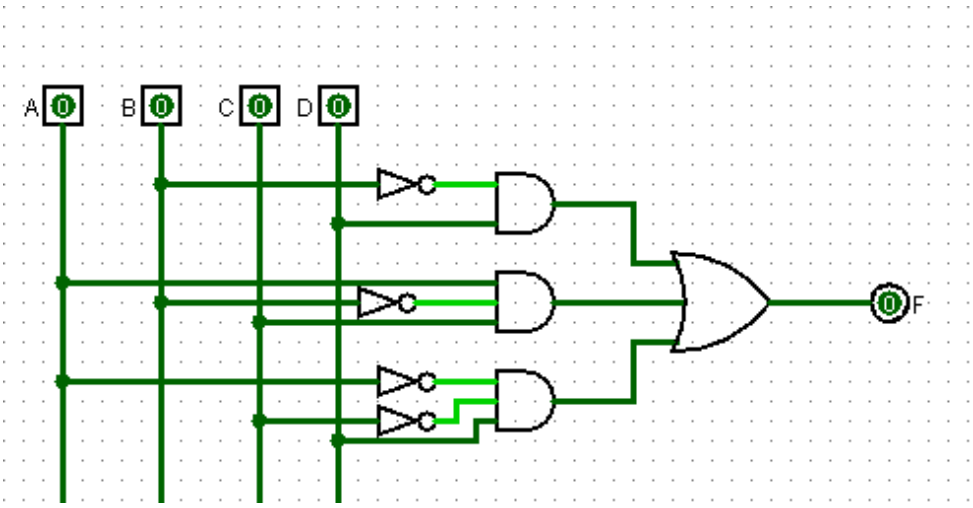
F = W'XYZ+WX'YZ+WXY'Z+WXYZ'+WXYZ



(f) Simplify the following Boolean function *f* together with don't-care condition *d* and implement it with basic logic gates: $f(A, B, C, D) = \Sigma_m(1,3,5,9,10,11) + \Sigma_d(6,12,14)$.

AB \ CD	00	01	11	10
00		1	1	
01		1		X
11	X			X
10		1	1	1

F = B'D+AB'C+A'C'D



Question 3 (8 Marks: 4+4)

(a) Given two decimal numbers A = -32 and B = -7, convert them into 2's complement representation using 8 bits and show how to compute A+B and A-B.

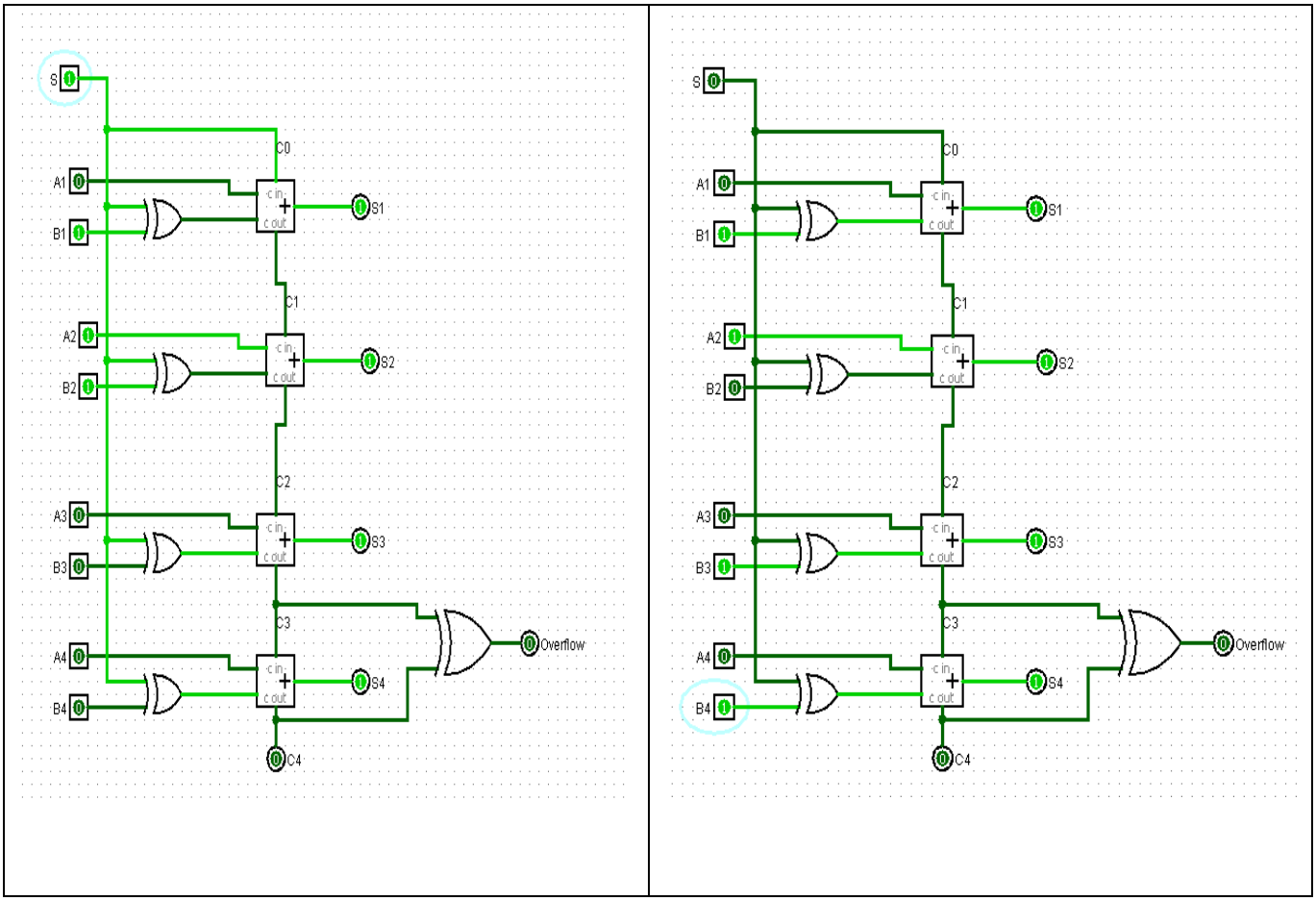
A (2's comp. using 8 bits)	**Ans: 11100000**
B (2's comp. using 8 bits)	**Ans: 11111001**
A+B (2's comp. using 8 bits)	**Ans: 11011001**
A-B (2's comp. using 8 bits)	**Ans: 11100111**

(b) You need to design a binary adder-subtractor circuit with overflow and sign detection for a 4-bit computer

i. Draw the adder-subtractor circuit

ii. Add the functionality of overflow and sign detection

iii. Show the **inputs and outputs** of the circuit to compute **(2 – 3).**



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