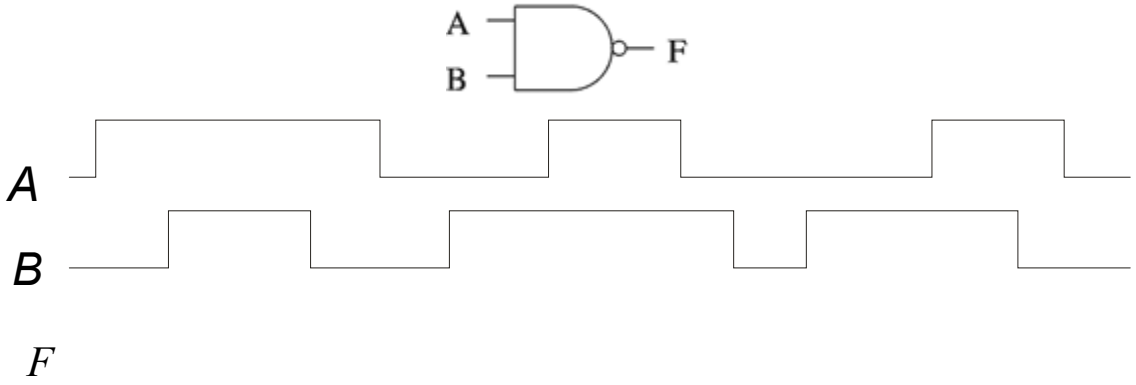
King Saud University
College of Computer and Information Sciences
Department of Computer Science

CSC 220: Computer Organization

Tutorial-2: Logic Gates and Functions

Q1: Given the web-forms for input A and B for the following NAND gate. Draw the output web-form for F.



Q 2: Given the function *f*(A, B, C, D) = Σ(2, 3, 5, 6, 7, 9, 11, 13)

i. Write the output expression in SOP form

ii. Implement it with basic logic gates

Q3: An *n*-bit even parity generator will produce an extra bit based on *n* input bits – it will produce 1 if number of 1's in *n* input bits is odd, 0 otherwise (e.g. for 4-bit input 0111 the extra bit will be 1, and for 1001 it will be 0).

i. Give the truth table for four-bit parity generator using even parity bit

ii. Write the output expression in SOP form

iii. Write the output expression in POS form.

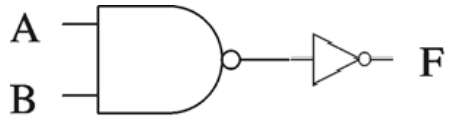
Q4: A majority function is generated in a combinational circuit when the output is equal to 1 if the input variables have more 1's than 0's, the output is 0 otherwise.

i. Give truth table four-input majority function

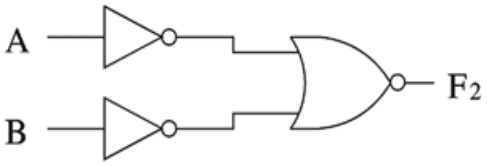
ii. Write the output expression in SOP form

iii. Draw the logic circuit.

Q5: Using truth table, show that the following two circuits are logically equivalent.



(a)



(b)

Home Works

Text book problems: 2-11, 2-13, 3-1, 3-3, 3-8

Additional Problems

1: Which of the following Boolean equations describes the circuit of Fig. 2.5.2?

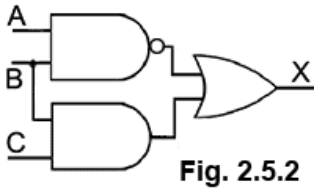


Fig. 2.5.2

a) X = (A • B)' + (B • C)
b) X = (A • B) • (B + C)
c) X =(A•B) + (B • C)
d) X = (A • B) + C

2: Which of the following logic functions is illustrated by Fig. 2.5.3?

Fig.2.5.3

a) XOR b) NOR c) AND d) NAND

3. Design four-bit parity generator using odd parity bit.

i. Give the truth table

ii. Write the output expression in SOP form

iii. Draw the logic circuit.