King Saud University College of Computer and Information Sciences Computer Science Department			
Course Code	CSC 220		
Course Title	Computer Organization		
Semester	S1 – 1440/1441 (Fall-2019-20)		
Exam	Final		
Date	31/12/2019	**Duration**	**3 Hours**
Student Name			
Student ID			
Section No.			

Course Learning Outcomes		**Relevant question**	**Full mark**	**Student mark**
Knowledge	**CLO 1, 2, 3**	**1**	**8**	
Knowledge	**CLO 4, 5, 6, 7**	**2**	**8**	
Cognitive Skills	**CLO 2, 3, 5**	**3**	**6**	
Cognitive Skills	**CLO 4, 5**	**4**	**6**	
Cognitive Skills	**CLO 3, 5**	**5**	**6**	
Cognitive Skills	**CLO 3, 6, 7**	**6**	**6**	

Feedback/Comments:

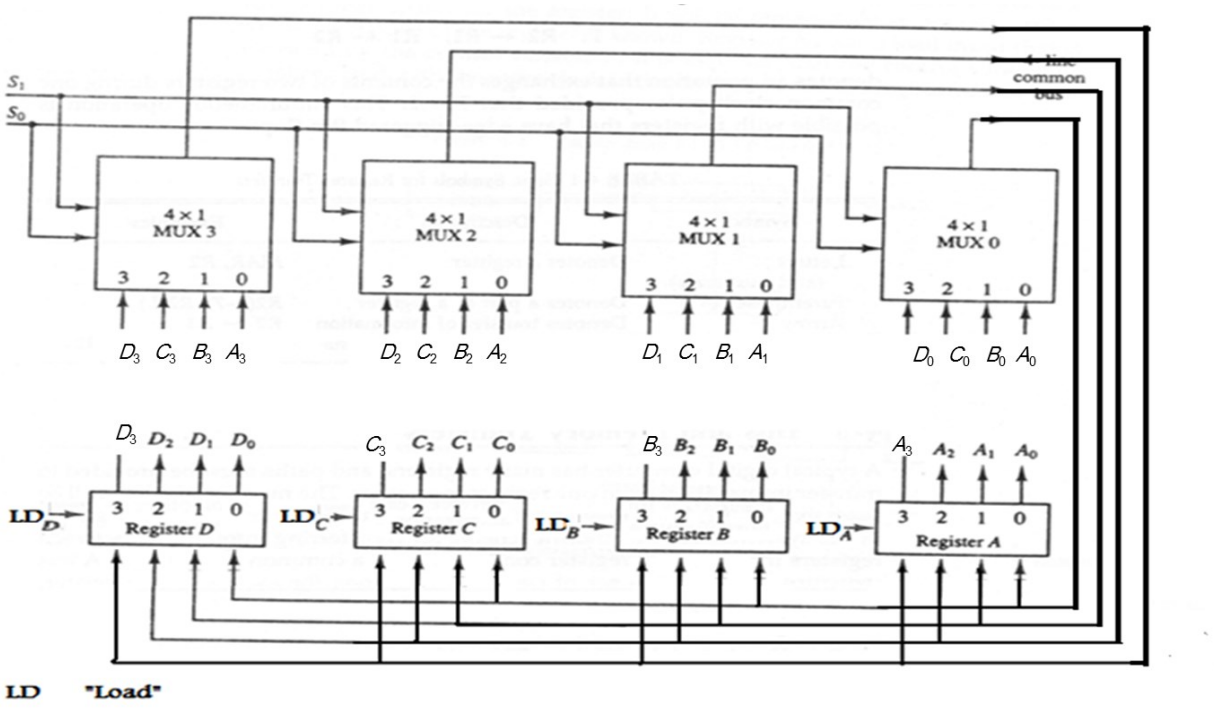
Question 1. Short Questions (2×4=8 Marks)

a) What are the decimal values of the following 8-bit binary number in 2's complement representation

i. 1110 0110

ii. 0110 0110

b) Given the following bus system for 4 registers. What selections are required for following transfer operations?



Operation	S1	S0	LD_A	LD_B	LD_C	LD_D
Register D ← Register B						
Register A ← Register C; Register D ← Register C						

c) Give the abbreviated truth table for **8x1** MUX?

d) Give the transition table of JK Flip Flop. Show how to obtain T Flip Flop from the JK structure?

Question 2. Short Questions (2+2+1+3 Marks)

a) Suppose we have 128 x 16 RAM chips

i. How many different addresses are required for a chip?

ii. How many chips are needed to provide a memory capacity of 2048 bytes?

b) Assuming registers are 8-bits width, and R1 = CE, R2 = 6F, R3 = 9F, R4 = FF, where numbers are represented in HEX and in 2's complement. If the instruction R1 <-- R2 + R3 is executed?

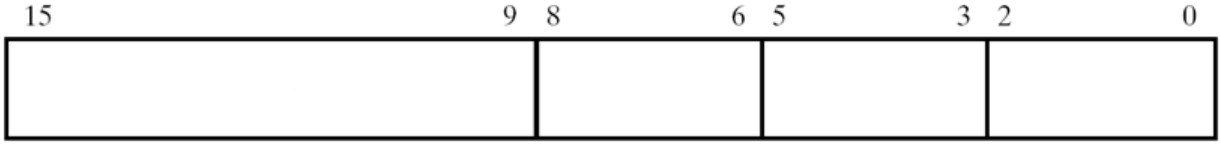
i. What is the content of R1 in Hex?

ii. What are the value of flags overflow "V", zero "Z", carry "C', and negative "N"?

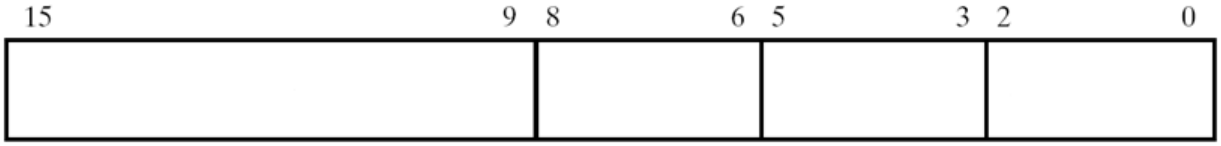
c) What is a datapath? What are the main components of a datapath?

d) Write name of the fields (e.g. Opcode, DR, SA, SB, etc) for the following three instruction formats for 16-bit instructions:

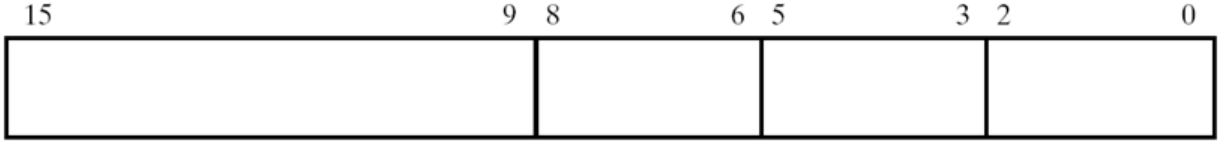
i. Register



ii. Immediate



iii. Jump and Branch



Question 3 (6 Marks: 2+2+2)

(a) Show how to design a 1 × 4 demultiplexer using basic logic gates (Hint: give the truth table, logic function, and circuit diagram).

(b) Design a 4-bits register that performs shift right (LD=0) and parallel load (LD=1) functions using necessary multiplexers and flip-flops.

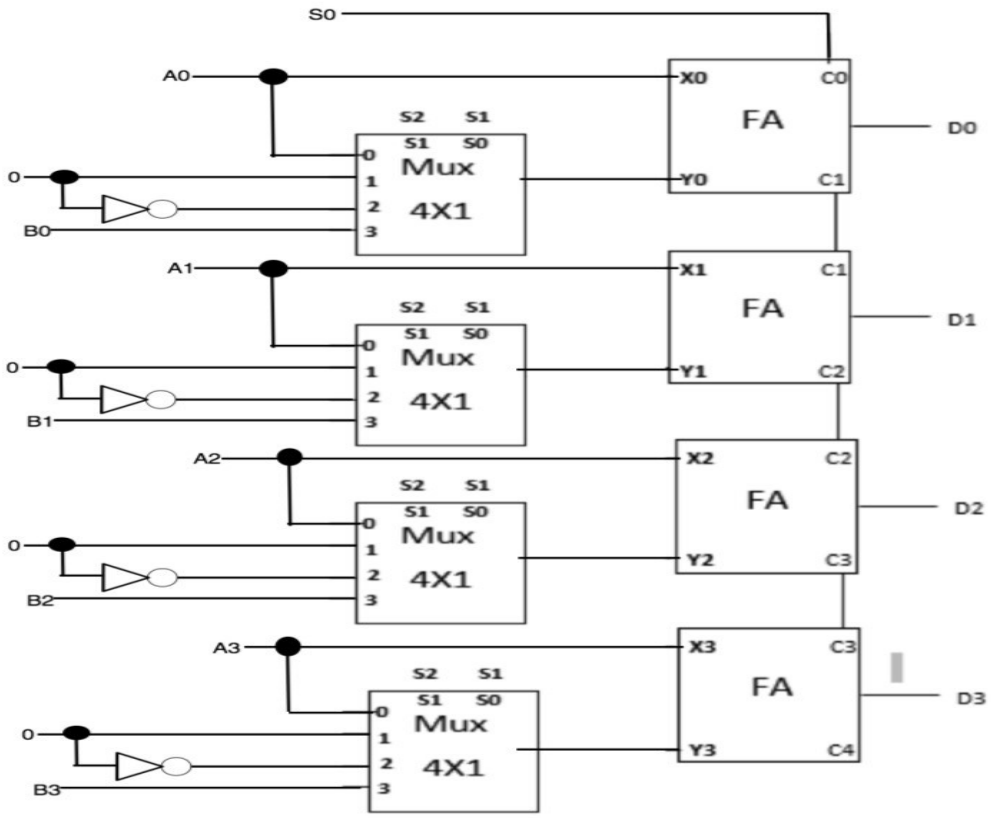
(c) Design a 4-bit binary **down** counter using JK Flip-Flops.

Question 4 (6 Marks: 2+4)

(a) Design a combinational shifter that can perform the following operations.

S1 S0	Operations
0 0	Transfer
0 1	Rotate right
1 0	Rotate left
1 1	Unused

(b) Analyze the following circuit and fill in the accompanied table to show its



Selection code			Required adder inputs			Resulted arithmetic operation
S_2	S_1	S_0	X	y	Co	D (X + Y + Co)
0	0	0				
0	0	1				
0	**1**	**0**				
0	**1**	**1**				
1	**0**	**0**				
1	**0**	**1**				
1	**1**	**0**				
1	**1**	**1**				

Question 5 (6 Marks: 3 +3)

Consider the datapath below described by table 8.5.

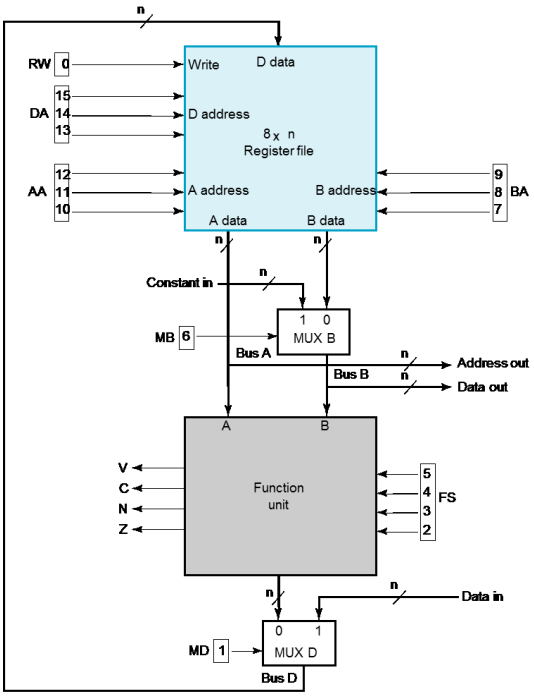


TABLE 8-5
Encoding of Control Word for the Datapath

DA, AA, BA		MB		FS		MD		RW	
Function	Code	Function	Code	Function	Code	Function	Code	Function	Cod
$R0$	000	Register	0	$F = A$	0000	Function	0	No Write	0
$R1$	001	Constant	1	$F = A + 1$	0001	Data in	1	Write	1
$R2$	010			$F = A + B$	0010				
$R3$	011			$F = A + B + 1$	0011				
$R4$	100			$F = A + \overline{B}$	0100				
$R5$	101			$F = A + \overline{B} + 1$	0101				
$R6$	110			$F = A - 1$	0110				
$R7$	111			$F = A$	0111				
				$F = A \wedge B$	1000				
				$F = A \vee B$	1001				
				$F = A \oplus B$	1010				
				$F = \overline{A}$	1011				
				$F = B$	1100				
				$F = \text{sr } B$	1101				
				$F = \text{sl } B$	1110				

Fill in the required information in the table below to perform the following instructions assuming that the registers of 8 bits, and their initial signed 2's complement values were, R0= 0E, R1 = 09, R2 = 0A, R3 = 0B, data in memory as shown. The required information is:

a. The generated control signals (**AA, BA, DA, WR, MB, MD, MW, FS**) on the diagram to perform the instruction.
b. The **contents of memory and registers** after executing following 5 instructions.

R0 ← M[R1]
R1 ← M[R3]
R1 ← R1 – R0
M[R2] ← R1
M[R3] ← R0

address	memory
09	**20**
0A	**A3**
0B	**21**
2E	**34**
2F	**E4**
30	**71**

AA	BA	DA	WR	MB	MD	MW	FS	Microoprations
								R0 ← M[R1]
								R1 ← M[R3]
								R1 ← R1 - R0
								M[R2] ← R1
								M[R3] ← R0

The contents of Registers and Memory are as shown:

R0=

R1 =

R2 =

R3 =

address	memory
09	**20**
0A	
0B	
2E	**34**
2F	**E4**
30	**71**

Question 6 (6 Marks: 2+4)

TABLE 8-8
Instruction Specifications for the Simple Computer

Instruction	Opcode	Mnemonic	Format	Description	Status Bits
Move A	0000000	MOVA	RD, RA	R[DR] ← R[SA]*	N, Z
Increment	0000001	INC	RD, RA	R[DR] ← R[SA] + 1*	N, Z
Add	0000010	ADD	RD, RA, RB	R[DR] ← R[SA] + R[SB]*	N, Z
Subtract	0000101	SUB	RD, RA, RB	R[DR] ← R[SA] − R[SB]*	N, Z
Decrement	0000110	DEC	RD, RA	R[DR] ← R[SA] − 1*	N, Z
AND	0001000	AND	RD, RA, RB	R[DR] ← R[SA] ∧ R[SB]*	N, Z
OR	0001001	OR	RD, RA, RB	R[DR] ← R[SA] ∨ R[SB]*	N, Z
Exclusive OR	0001010	XOR	RD, RA, RB	R[DR] ← R[SA] ⊕ R[SB]*	N, Z
NOT	0001011	NOT	RD, RA	R[DR] ← $\overline{R[SA]}$*	N, Z
Move B	0001100	MOVB	RD, RB	R[DR] ← R[SB]*	
Shift Right	0001101	SHR	RD, RB	R[DR] ← sr R[SB]*	
Shift Left	0001110	SHL	RD, RB	R[DR] ← sl R[SB]*	
Load Immediate	1001100	LDI	RD, OP	R[DR] ← zf OP*	
Add Immediate	1000010	ADI	RD, RA, OP	R[DR] ← R[SA] + zf OP*	N, Z
Load	0010000	LD	RD, RA	R[DR] ← M[SA]*	
Store	0100000	ST	RA, RB	M[SA] ← R[SB]*	
Branch on Zero	1100000	BRZ	RA, AD	if (R[SA] = 0) PC ← PC + se AD, if (R[SA] ≠ 0) PC ← PC + 1	N, Z
Branch on Negative	1100001	BRN	RA, AD	if (R[SA] < 0) PC ← PC + se AD, if (R[SA] ≥ 0) PC ← PC + 1	N, Z
Jump	1110000	JMP	RA	PC ← R[SA]*	

* For all of these instructions, PC ← PC + 1 is also executed to prepare for the next cycle.

(a) Consider Table 8-8 containing instruction specification for a simple computer. Translate the following instructions into 16-bit binary machine codes. (**NB:** use 0 for don't care)

Instruction	**Binary machine code**			
	Opcode	**RD/AD(left)**	**RA**	**RB/OP/AD(Right)**
SUB R7, R3, R0				
ST R6, (R1)				
ADI R0, R2, 5				
BRZ R5 AD (AD = 101 011)				

(b) Assume that the variable *x* is located at the address 105 in data memory containing 3, and the variable *y* is located at the address 106 containing 31. Write an assembly language program to evaluate the equation *z* = (*x*4*) - (*y* - 1) where variable *z* is located at the address 110. (**NB:** use only register R0 as address register).

THE END

b) Assuming registers are 8-bits width, and R1 = CE, R2 = 6F, R3 = 9F, R4 = FF, where numbers are represented in HEX and in 2's complement. If the instruction R1 <-- R2 + R3 is executed?

i. What is the content of R1 in Hex? 0 0 1 6

ii. What are the value of flags overflow "V", zero "Z", carry "C', and negative "N"?

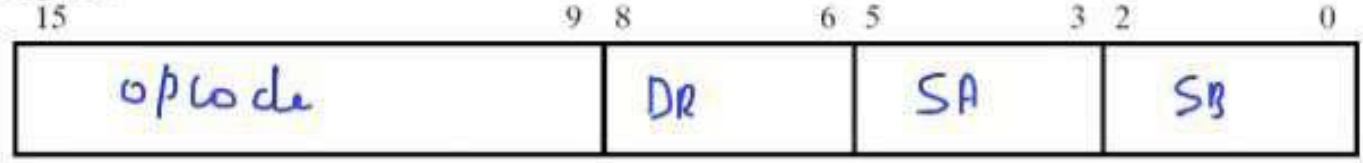
$R_2 = 6F \rightarrow$ 0110 1111

$R_3 = 9F \rightarrow$ 1001 1111

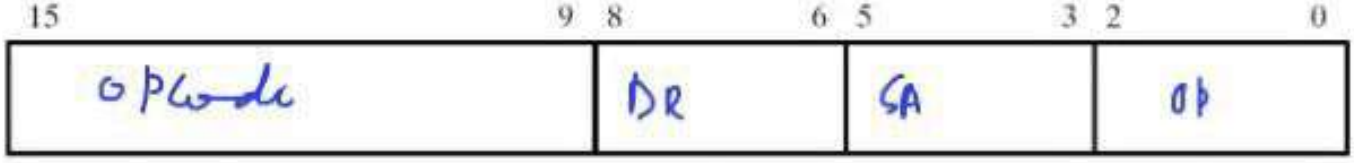
1 0000 1110 → 0E

d) Write name of the fields (e.g. Opcode, DR, SA, SB, etc) for the following three instruction formats for 16-bit instructions:

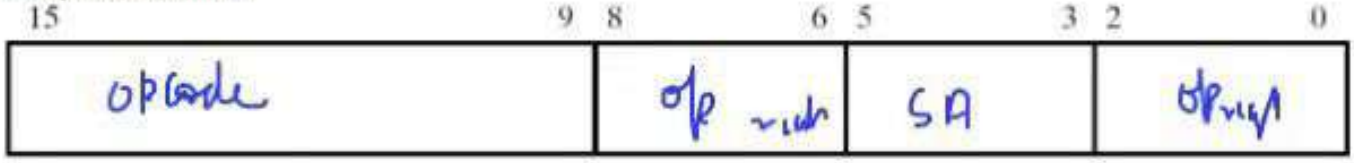
i. Register



ii. Immediate



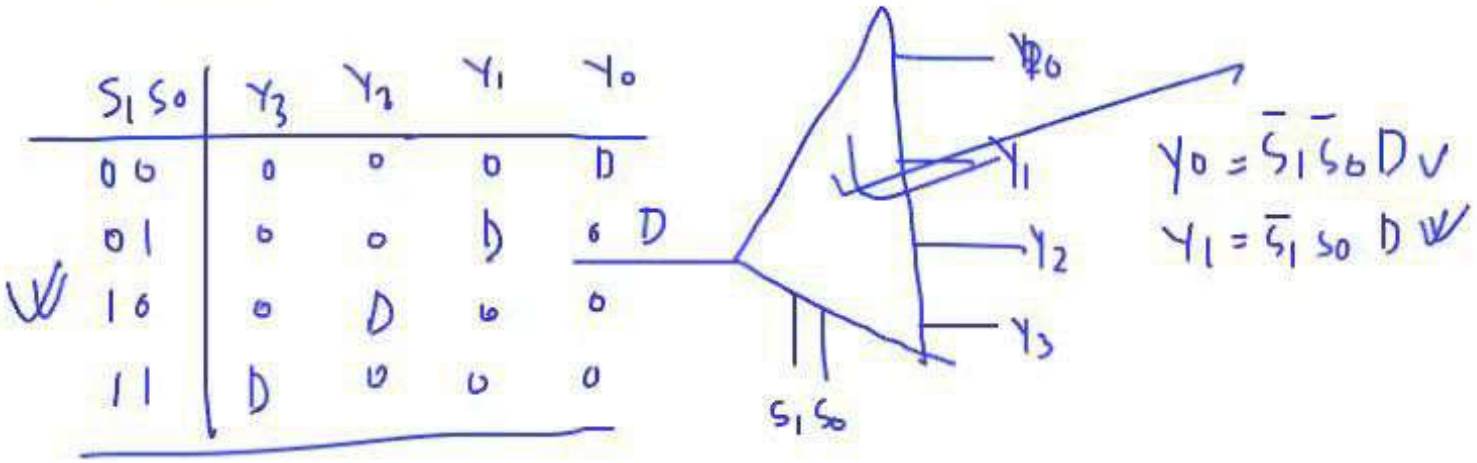
iii. Jump and Branch



Question 3 (6 Marks: 2+2+2)

(a) Show how to design a 1 × 4 demultiplexer using basic logic gates (Hint: give the truth table, logic function, and circuit diagram).

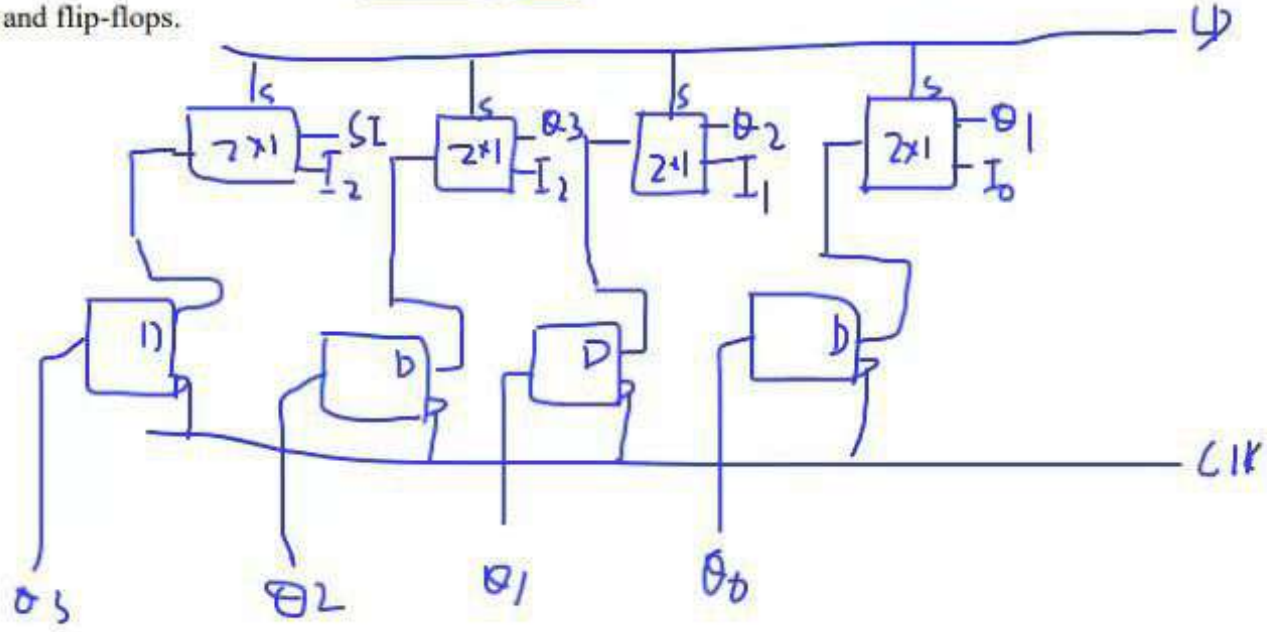
S_1 S_0	Y_3	Y_2	Y_1	Y_0
0 0	0	0	0	D
0 1	0	0	D	0
1 0	0	D	0	0
1 1	D	0	0	0



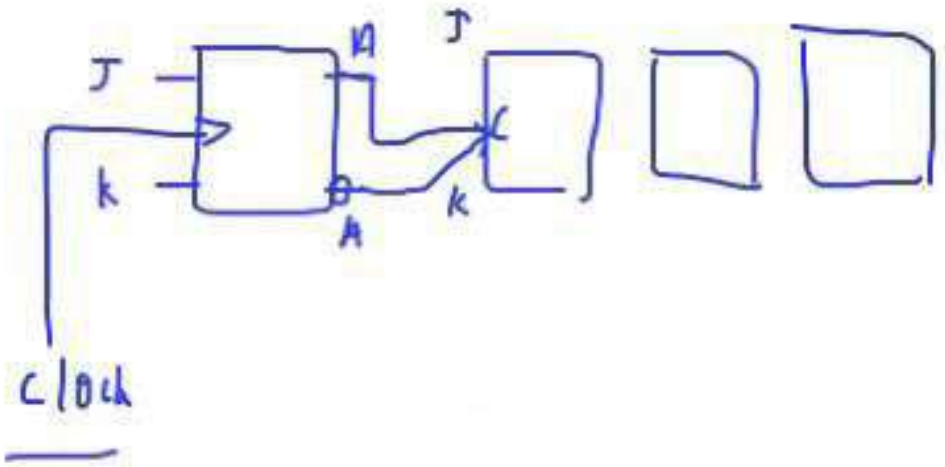
$Y_0 = \bar{S}_1 \bar{S}_0 D$

$Y_1 = \bar{S}_1 S_0 D$

(b) Design a 4-bits register that performs shift right (LD=0) and parallel load (LD=1) functions using necessary multiplexers and flip-flops.



(c) Design a 4-bit binary **down** counter using JK Flip-Flops.



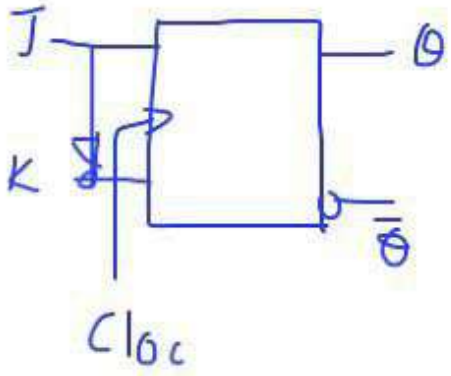
Question 4 (6 Marks: 2+4)

(a) Design a combinational shifter that can perform the following operations.

S1 S0	Operations
0 0	Transfer
0 1	Rotate right
1 0	Rotate left
1 1	Unused

d) Give the transition table of JK Flip Flop. Show how to obtain T Flip Flop from the JK structure?

C	J	K	Q(t+1)
0	X	X	Q(t) ✓
1	0	0	Q(t) ✓
1	0	1	0 ✓
1	1	0	1 ✓
1	1	1	$\bar{Q}$(t) ✓



Question 2. Short Questions (2+2+1+3 Marks)

a) Suppose we have 128 × 16 RAM chips

i. How many different addresses are required for a chip?

ii. How many chips are needed to provide a memory capacity of 2048 bytes?

7
2

0000000

1111111 3

M.size = $2^7 \times 2^4$ bits

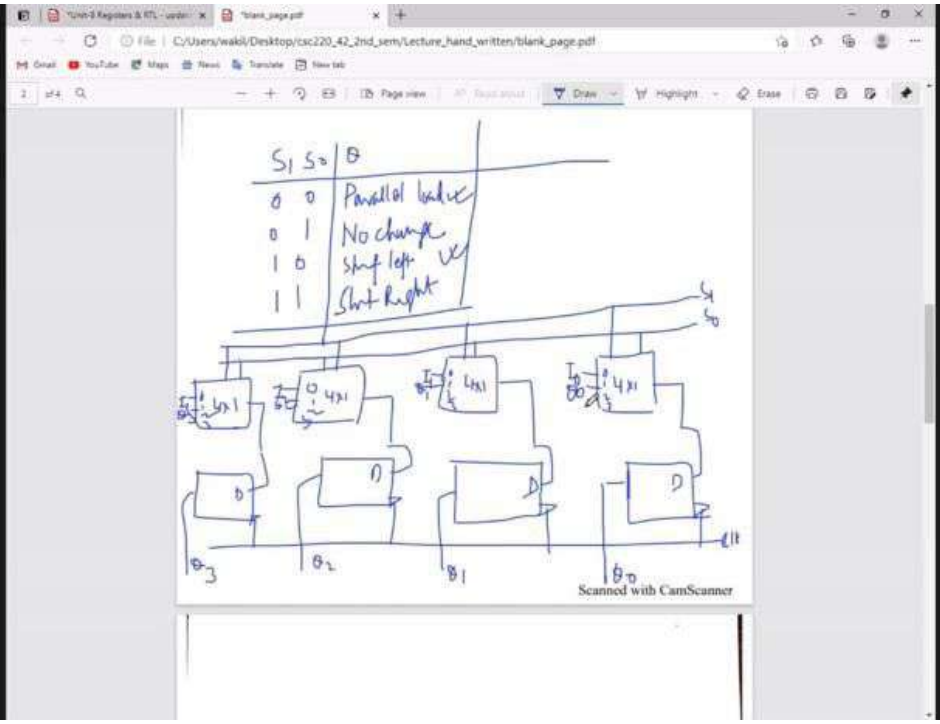
$= 2^8$ byte

2048 B

2^{11} B

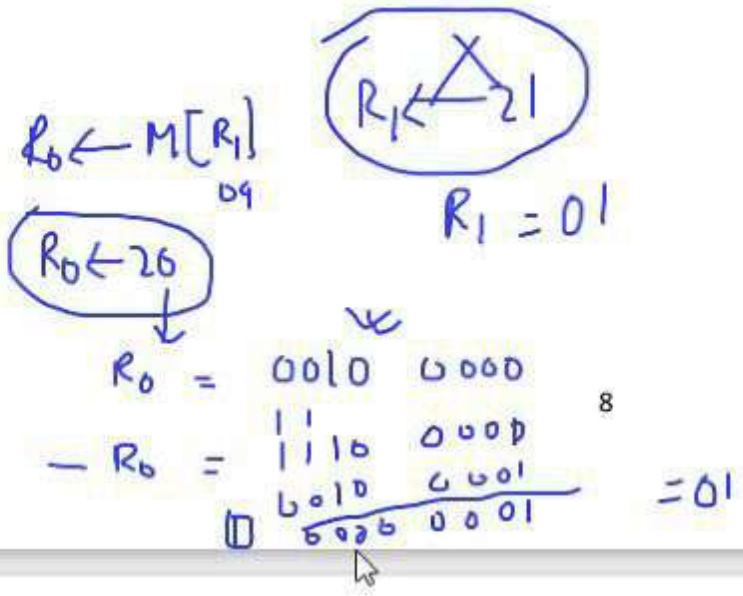
11
2

$\left(\begin{matrix}3\\2\end{matrix}\right)$ = 8



M[R3] ← R0

0B	21
2E	34
2F	E4
30	71



8

AA	BA	DA	WR	MB	MD	MW	FS	Microoprations
001	xxx	000	1	X	1	1	XXXX	R0 ← M[R1]
011	xxx	001	1	X	1	1	XXXX	R1 ← M[R3]
006	000	001	1	6	0	X	0101	R1 ← R1 - R0
								M[R2] ← R1
								M[R3] ← R0

Instruction Specifications for the Simple Computer

Instruction	Opcode	Mnemonic	Format	Description	Status Bits
Move A	0000000	MOVA	RD, RA	R[DR] ← R[SA]*	N, Z
Increment	0000001	INC	RD, RA	R[DR] ← R[SA] + 1*	N, Z
Add	0000010	ADD	RD, RA, RB	R[DR] ← R[SA] + R[SB]*	N, Z
Subtract	0000101	SUB	RD, RA, RB	R[DR] ← R[SA] − R[SB]*	N, Z
Decrement	0000110	DEC	RD, RA	R[DR] ← R[SA] − 1*	N, Z
AND	0001000	AND	RD, RA, RB	R[DR] ← R[SA] ∧ R[SB]*	N, Z
OR	0001001	OR	RD, RA, RB	R[DR] ← R[SA] ∨ R[SB]*	N, Z
Exclusive OR	0001010	XOR	RD, RA, RB	R[DR] ← R[SA] ⊕ R[SB]*	N, Z
NOT	0001011	NOT	RD, RA	R[DR] ← $\overline{R[SA]}$*	N, Z
Move B	0001100	MOVB	RD, RB	R[DR] ← R[SB]*	
Shift Right	0001101	SHR	RD, RB	R[DR] ← sr R[SB]*	
Shift Left	0001110	SHL	RD, RB	R[DR] ← sl R[SB]*	
Load Immediate	1001100	LDI	RD, OP	R[DR] ← zf OP*	
Add Immediate	1000010	ADI	RD, RA, OP	R[DR] ← R[SA] + zf OP*	N, Z
Load	0010000	LD	RD, RA	R[DR] ← M[SA]*	
Store	0100000	ST	RA, RB	M[SA] ← R[SB]*	
Branch on Zero	1100000	BRZ	RA, AD	if (R[SA] = 0) PC ← PC + se AD, if (R[SA] ≠ 0) PC ← PC + 1	N, Z
Branch on Negative	1100001	BRN	RA, AD	if (R[SA] < 0) PC ← PC + se AD, if (R[SA] ≥ 0) PC ← PC + 1	N, Z
Jump	1110000	JMP	RA	PC ← R[SA]*	

* For all of these instructions, PC ← PC + 1 is also executed to prepare for the next cycle.

(a) Consider Table 8-8 containing instruction specification for a simple computer. Translate the following instructions into 16-bit binary machine codes. (**NB:** use 0 for don't care)

Instruction	Binary machine code			
	Opcode	RD/AD(left)	RA	RB/OP/AD(Right)
SUB R7, R3, R0	0000101	111	011	000
ST (R6), (R1)	0100000	000	110	001
ADI R0, R2, 5	1000010	000	010	101
BRZ R5 AD (AD = 10 011)	1100000	101	101	011

$R_6 \leftarrow M(R_1)$ ST (R_6), R_1 (AA, BA)

(b) Assume that the variable x is located at the address 105 in data memory containing 3, and the variable y is located at the address 106 containing 31. Write an assembly language program to evaluate the equation $z = (x*4) - (y - 1)$ where variable z is located at the address 110. (**NB:** use only register R0 as address register).

$R_0 \leftarrow 105$

$R_1 \leftarrow M[R_0] \Rightarrow 3$

$R_0 \leftarrow R_0+1 = 106$

$R_2 \leftarrow M(R_0) \Rightarrow 31$

SHL $R_1 \Rightarrow 6$

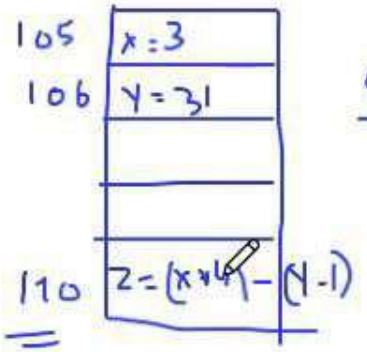
SHL $R_1 \Rightarrow 12$

$R_2 \leftarrow R_2 - 1 \Rightarrow 30$

$R_3 \leftarrow R_1 - R_2 \Rightarrow -18$

$R_0 \leftarrow R_0 + 4 \Rightarrow 110$

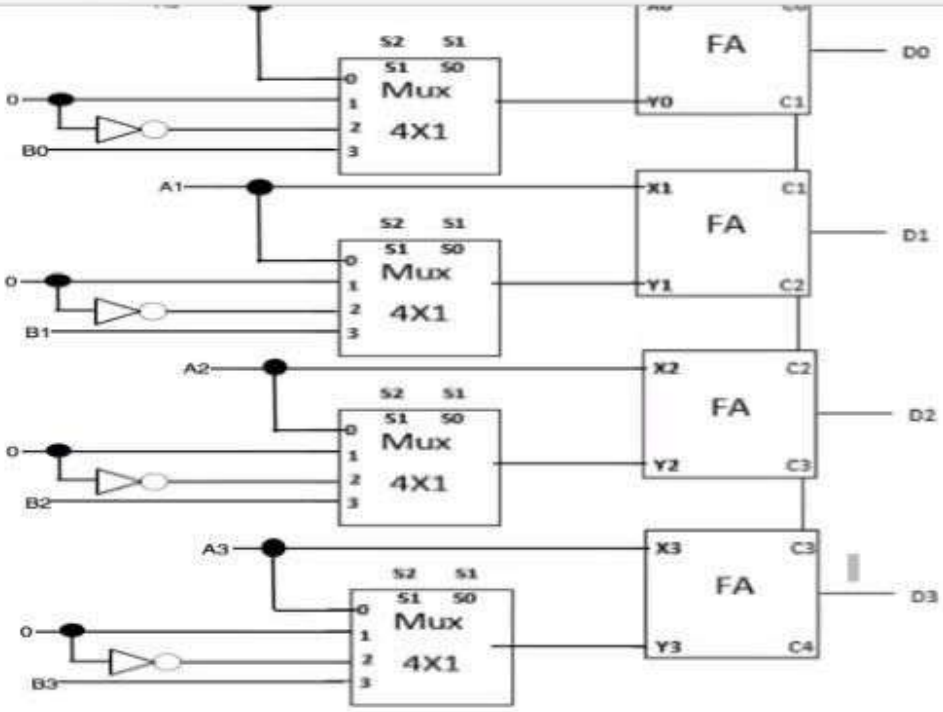
$M(R_0) \leftarrow R_3$



6 → 0101 = 5 → 1010 ↔ HL

10

```
LDI  R0, 105
LD   R1, (R0)
INC  R0, R0
LD   R2, (R0)
SHL  R1, R1
SHL  R1, R1
DEC  R2, R2
SUB  R3, R1, R2
ABI  R0, R0, 4
ST   (R0), R3
```



0 + 0 = 0
0 + 1 = 1

Selection code			Required adder inputs			Resulted arithmetic operation
S_2	S_1	S_0	X	y	Co	D (X + Y + Co)
0	0	0	A	A	0	A + A
0	0	1	A	A	1	A + A + 1
0	1	0	A	0	0	A
0	1	1	A	0	1	A + 1
1	0	0	A	1111 (-1)	0	A − 1
1	0	1	A	−1	1	A
1	1	0	A	B	0	A + B
1	1	1	A	B	1	A + B + 1