King Saud University
College of Computer and Information Sciences
Department of Computer Science

CSC 220: Computer Organization

Tutorial 7: Flip Flop

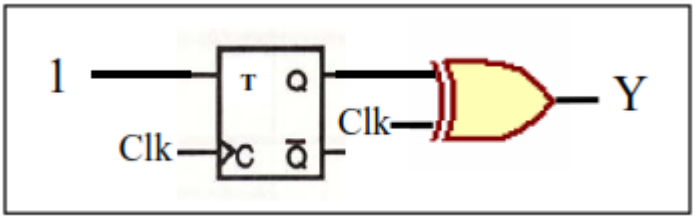
Q1:

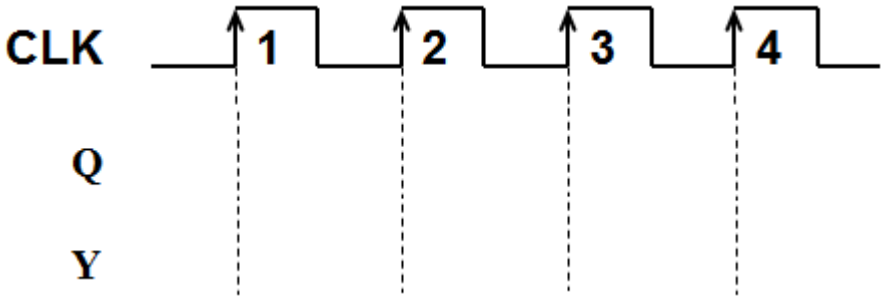
i. Give the transition table and Represent the synchronous SR Flip Flop with NAND gates.
ii. Explain the role of the control signal in the function of SR Flip Flop
iii. Explain how to obtain D Flip Flop from the SR structure.

Q2:

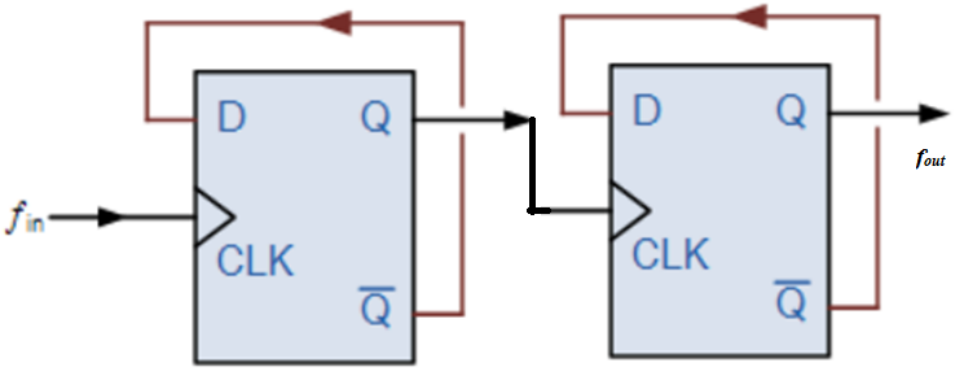
i. Give the transition table of JK Flip Flop.
ii. Show how to implement a JK flip-flop using NAND gates
iii. Explain how to obtain T Flip Flop from the JK structure.

Q3: For the given diagram below- what will be the output waveform at Q and Y (assuming that initially Q = 0)?

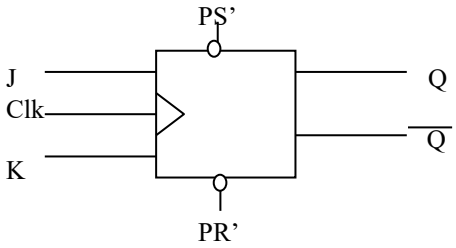




Q4: Determine the output frequency (f_{out}) for a frequency division circuit that contains 2 flip-flops with an input clock frequency of 20.48 MHz.

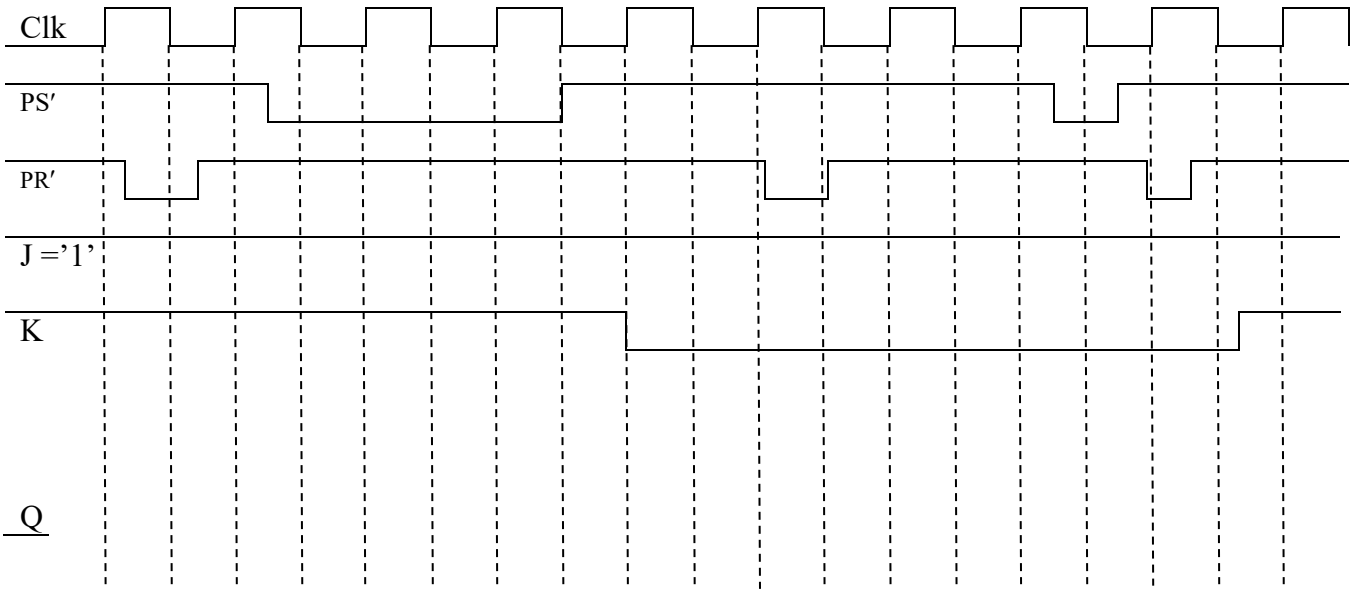


Q5: Consider the following JK Flip Flop.



i. Explain the role of the direct inputs (PS and PR) with characteristic table.

ii. Represent the outputs of the JK Flip flop (s) for the following input signal waves .



Home Works

Text book problems: 4-4, 4-5 (a-b), 4-6(a-b)

Additional Problems

1. Determine the output frequency for a frequency division circuit that contains 12 flip-flops with an input clock frequency of 20.48 MHz.
a. 10.24 kHz, b. 5 kHz, c. 30.24 kHz, d. 15 kHz

2. Clock speed is measured in
(a) bits per second (b) baud (c) bytes (d) Hertz

3. Explain how would draw the Y and Z activity in the following problem (if we ignore propagation delay and assume Y and Z start at 0)?