King Saud University
College of Computer and Information Sciences
Computer Science Department

Course Code: CSC 220
Course Title: Computer Organization

Final Exam
Semester: 1st (2016-2017)
Duration: 2 hours

Student's Name: _____

Student's ID: _____

Section No. _____

EVALUATION

Tick the Relevant	Computer Science B.Sc. Program: NCAAA: Intended Learning Outcomes (ILO) Student Outcomes ABET: Program Learning Outcomes (PLO) Student outcomes	Question No. Relevant Is Hyperlinked	Covering %	Full Mark	Obtained Mark
NCAAA	Knowledge (NCAAA) Suggested verbs (list, name, record, define, label, outline, state, describe, recall, memorize, reproduce, recognize, record, tell, write)	**Exercise 1**	$\sum$ ***ABET***%		
ABET	(a) Apply knowledge of computing and mathematics appropriate to the discipline;	Exercise 1	25 %	**10**	
NCAAA	Cognitive Skills (NCAAA) Suggested verbs (estimate, explain, summarize, write, compare, contrast, diagram, subdivide, differentiate, criticize, calculate, analyze, compose, develop, create, prepare, reconstruct, reorganize, summarize, explain, predict, justify, rate, evaluate, plan, design, measure, judge, justify, interpret, appraise)	**Exercise 2-4**	$\sum$ ***ABET***%		
ABET	(b) Ability to analyze a problem, and identify and define the computing requirements appropriate to its solution.	Exercise 2	15 %	**6**	
	(c) An ability to design, implement and evaluate a computer-based system, process, component, or program to meet desired needs.	Exercise 3	30 %	**12**	
		Exercise 4	30%	**12**	
		Total	**100%**	**40**	

Feedback and Remarks:

I certify that the work contained within this assignment is all my own work and referenced where required.

Student's Signature: **Date:**

Feedback Received:

Student's Signature: **Date:**

Question 1. (10 Marks)

MCQ (Put tick marks on answers)

1. Which is a read instruction from memory:

[A] R1 <--- MAR, [B] R1 <--- MDR, [C] R1 <--- M[MAR], [D] M[R1] <--- R1

Answer: [C]

2. If a register containing data (1100 1100) is subjected to arithmetic shift right operation, then the content of the register after the shift will be

(A) (1001 1001), (B) (0110 0110), (C) (1110 0110), (D) (1001 1000)

Answer: [C]

3. The content of a 4-bit register is initially 1101. The register is shifted 2 times to the right with the serial input being 1011101. What is the content of the register after each shift?

(A) 1110, 0111 (B) 0001, 1000 (C)1101, 1011 (D) 1001, 1001

Answer: (A)

4. The largest positive number that can be represented by 8 bit 2's complement signed number system is

[A] 256 [B] 255 [C] 128 [D] 127

Answer: [D]

5. The smallest negative number that can be represented by 8 bit 2's complement signed number system is

[A] -256 [B] -255 [C] -128 [D] -127

Answer: [C]

6. A digital computer has a common bus system for 8 registers of 32 bit each. The bus is constructed with multiplexers. How many multiplexers are there in the bus?

[A] 16, [B] 8, [C] 4, [D] 32

Answer: [D]

7. A digital computer has a common bus system for 8 registers of 16 bit each. The bus is constructed with multiplexers. How many selection inputs are there is each multiplexer?

[A] 8, [B] 4, [C] 2, [D] 16

Answer: [B]

8. Assuming registers are 8-bits width, and R1 = CF, R2 = 6F, R3 = 9F, R4 = FF, ""numbers are represented in HEX and in 2's complement" what is the contents of R1 in decimal, if the instruction ADD, R1, R1, R4 (in RTL: R1 <-- R1 + R4) is executed?

[A] -50 [B] 50 [C] 51 [D] -51

Answer: [A]

R1 = CF = 11001111 R4 = FF = 11111111								
R1	1	1	0	0	1	1	1	1
R4	1	1	1	1	1	1	1	1
Result = R1+R4	1	1	0	0	1	1	1	0
The 2's of the result is	0	0	1	1	0	0	1	0
	128	64	32	16	8	4	2	1
The 2's of the result is	50							
The result is	-50							

9. Assuming registers are 8-bits width, and R1 = CF, R2 = 6F, R3 = 9F, R4 = FF, ""numbers are represented in HEX and in 2's complement" what is the contents of overflow Flag "V" and Zero Flag "Z" and Sign "N" if the instruction SUB, R1, R1, R4 (in RTL: R1 <-- R1 - R4) is executed?
[A] V = 0, Z = 0, N = 1, **[B]** V = 1, Z = 0 , N = 0, **[C]** V = 0, Z = 1, N= 0, **[D]** V = 0, Z = 0, N=1

Answer: [D]

R1 = CF = 11001111 R4 = FF = 11111111								
R1	1	1	0	0	1	1	1	1
2s com. Of R4	0	0	0	0	0	0	0	1
Result = R1+(2s com. Of R4)	1	1	0	1	0	0	0	0
The result is	D				0			
V = Cn-1 XOR Cn	0 XOR 0 = 0							
V = 0, Z =0, N =1	Answer is D							

10. Assuming registers are 8-bits width, and R1 = CF, R2 = 6F, R3 = 9F, R4 = FF, numbers are represented in HEX and in 2's complement, what is the contents of R1, if the instruction SUB, R1, R1, R4 (in RTL: R1 <-- R1 - R4) is executed?
[A] R1= CF [B] R1= FC [C] R1= D0 [D] R1= FF

Answer: [C]

Question 2. (6 Marks: 2+4)

(a) Suppose we have a memory chip containing 128 words of 16-bit each. Compute and give how many bits (address line) do we need for selecting a single word? What is the size of that memory in Bytes.

(b) Using multiplexers 2-to-1, design a 4-bits register that performs a shift right (LD = 0) and parallel load (LD = 1) functions.

Answer of Question 2 (a)

Since $2^7 = 128$

No. of bits (address line) = 7

Memory = 2^7* 16 bits

$= 2^7 * 2^4 / 8$

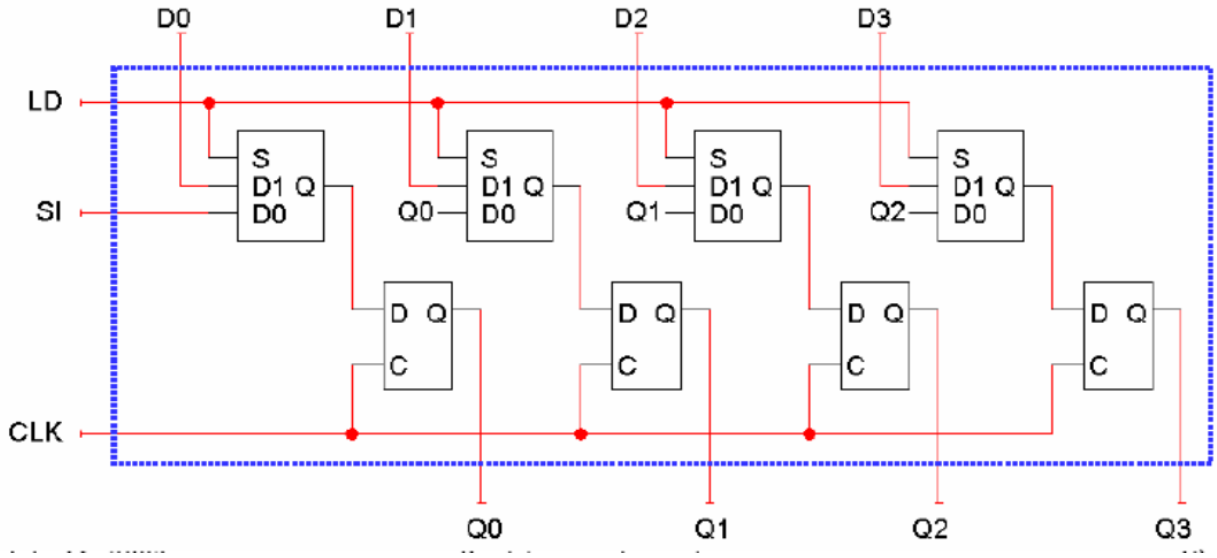
$= 2^{11}/2^3$

$= 2^8$

= 256 Bytes

2 kilo bits

Answer of Question 2 (b)



Question 3 (10 Marks: 3+6+3)

(a) Represent the following **decimal** numbers in 8 bit 2's complement signed number system

I. -10

II. + 64

III. -1

(b) Design a 4-bit arithmetic unit using full adders and multiplexers to perform following micro operations

S1	S0	Cin	Micro Operation
0	0	0	Addation (A+B)
0	0	1	Addition with carry (A+B+1)
0	1	0	Transfer A
0	1	1	Increment A
1	0	0	Decremnet A
1	0	1	Transfer A
1	1	0	Subtraction with barrow (A+B')
1	1	1	2's complement Subtraction (A+B'+1)

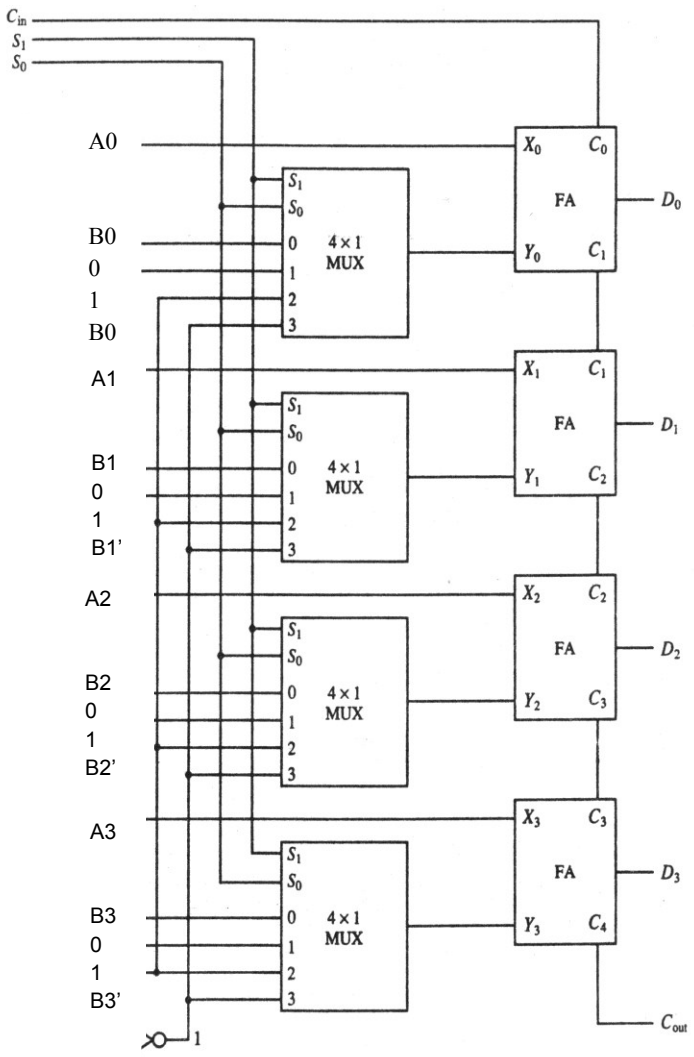
(c) Give the circuit diagram for 1bit logic unit to perform the following logic operations

S1	S0	Logic Operations
0	0	Bitwise AND
0	1	Bitwise OR
1	0	Bitwise XOR
1	1	Bitwise NOT

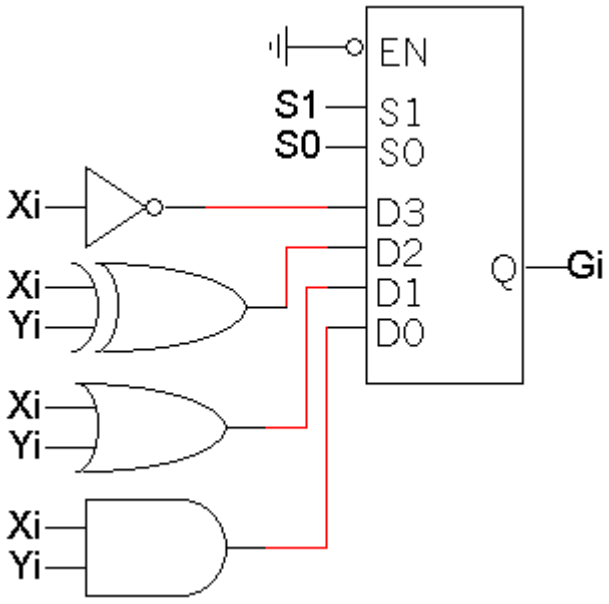
Answer of Question 3 (a)

I. -10 = 1111 0110
II. +24 = 0001 1000
III. -1 = 1111 1111

Answer of Question 3 (b)



Answer of Question 3 (c)

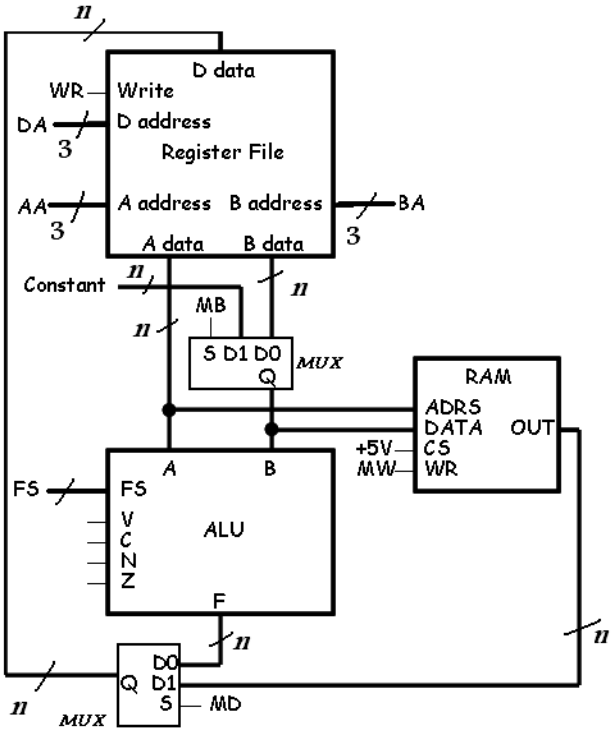


Question 4 (12 Marks: 6+6)

Here is the most basic datapath you have studied.

– The ALU's two data inputs.

– The ALU computes a result, which is saved back to the registers. AA, BA, DA, WR, MB, MD, MW, and FS are control signals. Their values determine the exact actions taken by the datapath, and which registers are used and for what operation.



FS	Operation
0000	F = A
0001	F = A + 1
0010	F = A + B
0011	F = A + B + 1
0100	F = A + B'
0101	F = A + B' + 1
0110	F = A - 1
0111	F = A
1000	F = A ∧ B (AND)
1001	F = A ∨ B (OR)
1010	F = A ⊕ B (XOR)
1100	F = B
1011	F = A'

Assume that the registers of 8 bits, and their initial signed 2's complement values were, R0= 0E, R1 = 0F, R2 = 09, R3 = 0B, data in memory as shown in the right-side figure, and the initial values of V, C, N, Z were 0's

a. **Fill in the given** table 3 with the generated control signals (**AA, BA, DA, WR, MB, MD, MW, FS**) on the diagram to perform the instructions below.

b. The **contents of memory and registers** after executing the 5 instructions.

```
LD R0, (R3)
LD R3, (R2)
ADD R1, R0, #0F
ST (R2), R1
ST (R1), R3
```

address	memory
09	AA
0A	A3
0B	21
0C	
2F	E4
1E	71

0.6 Mark each row

0.5 Mark

0.5 Mark each

Answer

[illegible]	BA	DA	WR	MB	MD	MW	FS	Instruction in RTL
….	….	….	….	….	….	….		LD R0, (R3)
								……
….	….	….	….	….	….	….		LD R3, (R2)
								……
….	….	….	….	….	….	….	….	ADD R1, R0, #F0
								……
….	….	….	….	….	….	….		ST (R2), R1
								……
….	….	….	….	….	….	….		ST (R1), R3
								……

Table 3

1 Mark each

MW and WR never takes x "don't car"

The contents of Registers and Memory are as shown: [6 MARKS]

[1 Mark] R0=

[1 Mark] R1 =

[1 Mark] R2 =

[1 Mark] R3 =

address	memory
09	……
0A	A3
0B	21
0C	
2F	E4
30	……

AA	BA	DA	WR	MB	MD	MW	FS	Instruction in RTL
011	XXX	000	1	X	1	0	XXXX	LD R0, (R3) R0 ← M[R3]
010	XXX	011	1	X	1	0	XXXX	LD R3, (R2) R3 ← M[R2]
001	XXX	000	1	1	0	0	0010	ADD R1, R0, #F0 R1 ← R0 + 0F
010	001	XXX	0	0	1	1	XXXX	ST (R2), R1 M[R2]← R1
001	011	XXX	0	0	1	x	XXXX	ST (R1), R3 M[R1]← R3

The contents of Registers and Memory are as shown:

R0= 21

R1 = 30

R2 = 09

R3 = AA

address	memory
09	30
0A	A3
0B	21
0C	
2F	E4
30	AA

THE END