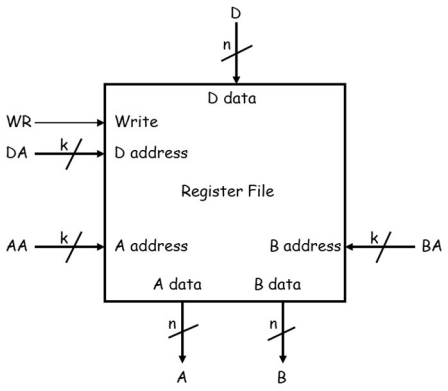
King Saud University
College of Computer and Information Sciences
Department of Computer Science

CSC 220: Computer Organization

Tutorial 11: Datapath Design

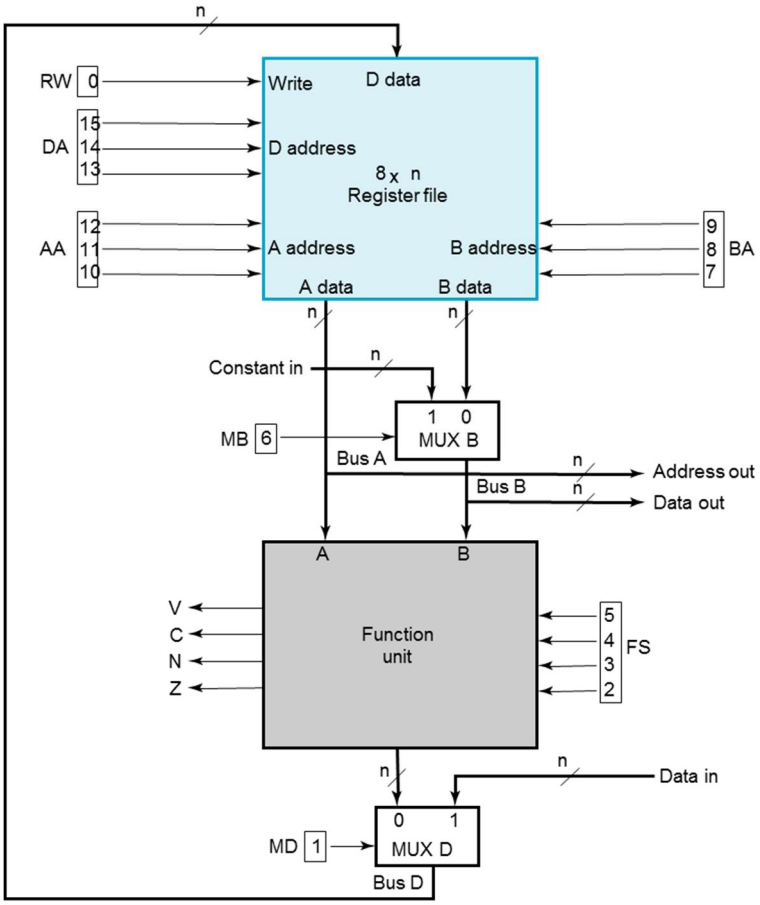
Q1: Show how to construct a 4 x n register file using necessary registers, MUX and decoder.



Q2: Show the representation of a general datapath using the block diagrams for a register file (2^m x n) and the function unit.

Q 3:

Consider the following datapath and function table.



FS	Operation
0000	F = A
0001	F = A + 1
0010	F = A + B
0011	F = A + B + 1
0100	F = A + B'
0101	F = A + B' + 1
0110	F = A - 1
0111	F = A
1000	F = A ∧ B (AND)
1001	F = A ∨ B (OR)
1010	F = A ⊕ B (XOR)
1011	F = A'
1100	F = B
1101	F = sr B (shift right)
1110	F = sl B (shift left)

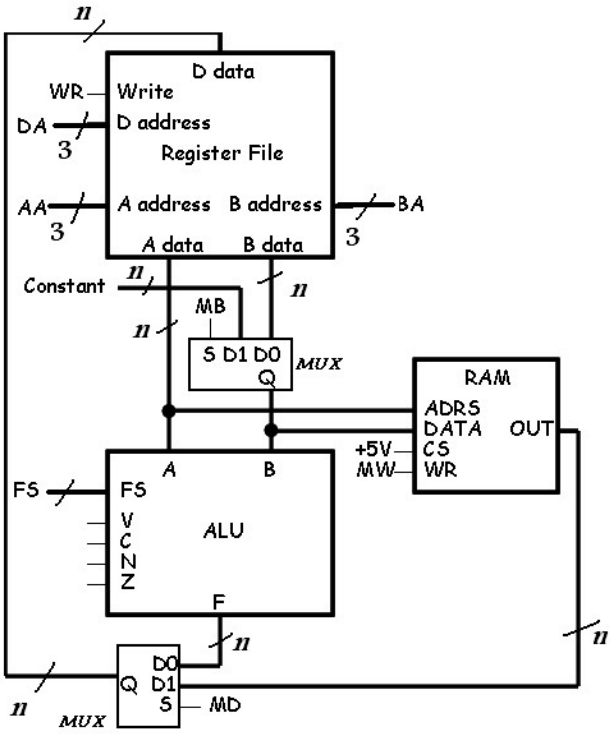
Show the 16-bit control words on the table below to perform the following microoperations assuming that the registers are 8 registers in the register file

Microoperations	DA (15-13)	AA (12-10)	BA (9-7)	MB (6)	FS (5-2)	MD (1)	RW (0)
R1←R1-5							
R0←R1+R5							
R7←R7+1							
R4←sl R6							
M[R3]←R1							

Q4: Here is the most basic datapath you have studied.

– The ALU's two data inputs.

– The ALU computes a result, which is saved back to the registers. AA, BA, DA, WR, MB, MD, MW, and FS are control signals. Their values determine the exact actions taken by the datapath, and which registers are used and for what operation.



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1011	F = A'

Fill in the required information in the answer table to perform the following instructions assuming that the registers of 8 bits, and their initial signed 2's complement values were, R0= 0E, R1 = 0F, R2 = 09, R3 = 0B, data in memory as shown, and the initial values of V, C, N, Z were 0's. The required information are:

a. The generated control signals (**AA, BA, DA, WR, MB, MD, MW, FS**) on the diagram to perform the instruction.

b. The values **of V, C, N, and Z status flags** after each instruction.

c. The **contents of memory and registers** after executing the 5 instructions.

R0 ← M[R3]
R3 ← M[R2]
R1 ← R0 + 0F
M[R2] ← R1
M[R1] ← R3

memory address	
09	**20**
0A	**A3**
0B	**21**
2E	**34**
2F	**E4**
30	**71**

Answer

AA	BA	DA	WR	MB	MD	MW	FS	V	C	N	Z	Microoprations
011	XXX	000	1	X	1	0	XXXX					R0 ← M[R3]
												R3 ← M[R2]

												R1 ← R0 + 0F
								[redacted]	[redacted]	[redacted]	[redacted]	M[R2] ← R1
								[redacted]	[redacted]	[redacted]	[redacted]	M[R1] ← R3

(6 points)

The contents of Registers and Memory are as shown:

R0=

R1 =

R2 =

R3 =

address	memory
09	
0A	A3
0B	21
2E	34
2F	E4
30	

Home Works

Text book problems: 8-9 to 8.10

Additional Problems:

1. A 32-bit processor has
(a) 32 registers (b) 32 I/O devices (c) 32 Mb of RAM (d) a 32bit bus or 32-bit registers