

CSC 220: Computer Organization

Unit 0 Introduction



Prepared by: Md Saiful Islam, PhD

Associate Professor

Department of Computer Science

College of Computer and Information Sciences

Office: G085 (Inside ALISR Laboratory)

Home Page: http://fac.ksu.edu.sa/saislam

Email: saislam@ksu.edu.sa

Main Component

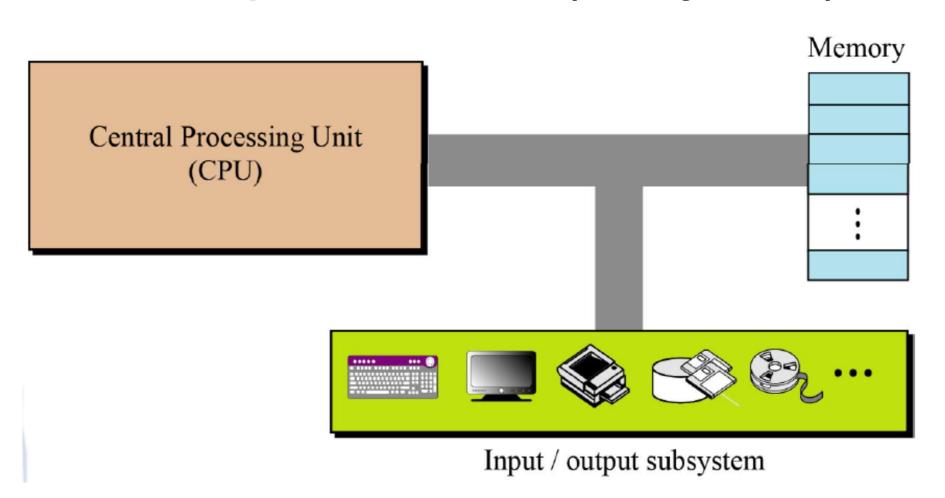
https://www.youtube.com/watch?v=yRmPTbGBqVI

Integrated Circuit (IC) Fabrication

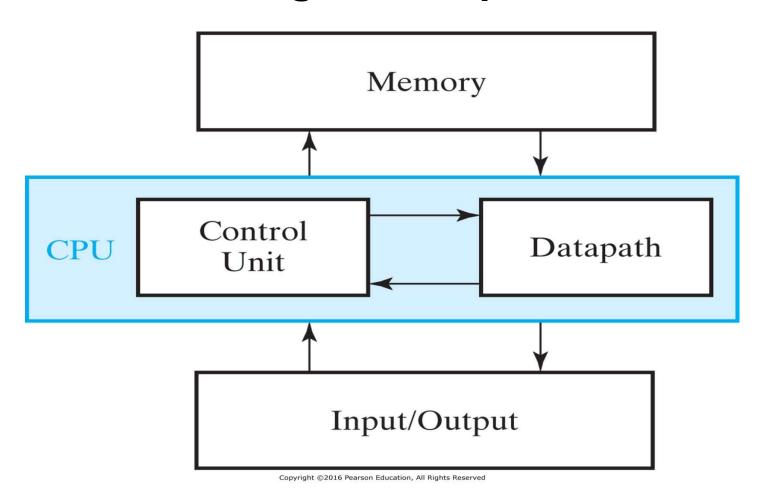
https://www.youtube.com/watch?v=aWVywhzuHnQ

https://www.youtube.com/watch?v=qm67wbB5Gml (new)

Computer Hardware (Subsystems)



A Digital Computer

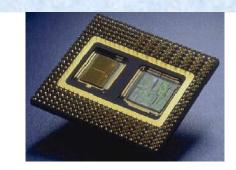


Central Processing Unit (CPU)

ALU	Registers R ₀ R ₁ R ₂ R _n
Control Unit	PC IR

History of Intel x86 processors

- 4004: 4-bit processor; 8-bit processors 8080, 8085.
- 8086: 16-bit processors, introduced in 1979: 20-bit address bus (AB), 16-bit data bus (DB), 5/8/10 MHz.
- 80186: a faster version of the 8086. Also 20-bit AB and 16-bit DB.
 Never widely used in computer systems.
- 80286: introduced in 1982, It has a 24-bit AB, which implies 16MB of memory address space.
- 80386: Intel introduced its first 32-bit processor in the 1985. It has 32-bit AB and 32-bit DB. It follows their 32-bit architecture known as IA-32.
- Pentium: was introduced in 1993 (20th anniversary). it uses a 64-bit wide DB, 60/66 MHz.
- Itanium: 64-bit processor, released in 2001; formerly called IA-64, the Itanium uses a 64-bit AB to provide substantially larger address space. Its DB is 128 bits wide.



CSC220 - Computer Organization (2-2-1) - Required Course

Pre-requisites: MATH 151 - Discrete Mathematics

Topics

- Data Representation: binary number systems, signed number systems, use of 1's and
 2's complements in addition and subtraction
- Digital Circuit Design: Logic gates, Logic function, K-Map simplification
- Combinational Circuits: Multiplexer, De-multiplexer, Decoder, Arithmetic circuits
- Sequential Circuits: register, binary counters, and memory organization
- Arithmetic and Logic Unit Design, Central Processing Unit design
- Register, Register Transfer Language, and micro-operations instruction set
- CPU Design and Programming

CSC 220: Course Learning Outcomes

	CLOs				
1	Knowledge and Understanding	"			
1.1	Data Representation	K2			
1.2	Digital circuit design and simplification	K2			
1.3	Instruction set and machine programming	K2			
1					
2	Skills:				
2.1	Combinational and sequential circuits design	S1			
2.2	Register, counter, and RAM design	S1			
2.3	Arithmetic and Logic Unit (ALU) design	S1			
2.4	Datapath and CPU design	S1			

Text Books

- 1. M. Morris Mano, Charles R. Kime and Tom Martin, **Logic and Computer Design Fundamentals**, 5th (Global) Edition, Pearson Education Limited, 2016. ISBN: 9781292096124
- 2. Morris Mano, Computer System Architecture 3rd Edition, Publisher: McGraw Hill

Class Note based on the main text (Available at the LMS)

Assessment Methods:

Final Exam: 40%

Quiz: --%

Midterm: 40%

Lab works: 15% (experiments 5%, test 10%, project 5%)

Home works: 5%

Important Information

Last Date to Drop Course:

Quiz: Unit- to be decided, Date to be decided

Midterm: Units- to be decided, Date decided by the college

Homework-1: to be decided Homework-2: to be decided

Final Exam: Unit 4-12.

Attendance Rules

- 1. Absent if you come after 15 minutes
- 2. Can't attend final exam if absence rate is more than 25%
- 3. No medical certificate will be considered for attendance

Schedule:

Week	Lecture 1	Lecture 2	Tutorial	Lab	Homerwork	Exam	
#01 (17 Jan, 21) Orientation	& Introduction					
#02 (Unit-1)	Number System	Number System	Tutorial-1				
#03 (Unit-2)	Digital Circuits	Digital Circuits	Tutorial-2	Lab-1			
#04 (Unit-3)	Simplification (K-map)	Simplification (K-map)	Tutorial-3	Lab-2			
#05 (Unit-4)	Signed Number Representation	Signed Number Representation	Tutorial-4	Lab-3	HW 1		
#06 (Unit-5)	Combinational circuit-1	Combinational circuit-1	Tutorial-5	Lab-4			
#07 (Unit-6)	Combinational circuit-2	Combinational circuit-2	Tutorial-6	Lab-5		Midterm (Unit)	
#08 (Unit-7)	Sequential Circuit	Sequential Circuit	Tutorial-7	Lab-6			
#09 (Unit-8)	Registers and RTL	Registers and RTL	Tutorial-8	Lab-7			
# 10		Revision					
#11 (Unit-9)	Counters-RAM	Counters-RAM	Tutorial-9	Lab-8	HW 2		
#12 (Unit-10)	ALU Design	ALU Design	Tutorial-10	Lab Test		Quiz (Unit)	
#13 (Unit-11)	Datapath Design	Datapath Design	Tutorial-11	Lab-9			
#14 (Unit-12)	CPU design & Programming	CPU design & Programming	Tutorial-12	Lab-10			
# 15		Revision		Lab Project			
#1 <i>C</i> /\		Droporatory Course	s Final Fyams				
#16 () #17 ()	Preparatory Courses Final Exams						
#18 ()	Final Exams (Unit 4-12)						