PARALLEL PROCESSING

Mohammed Alabdulkareem

kareem@ksu.edu.sa

Office 2247



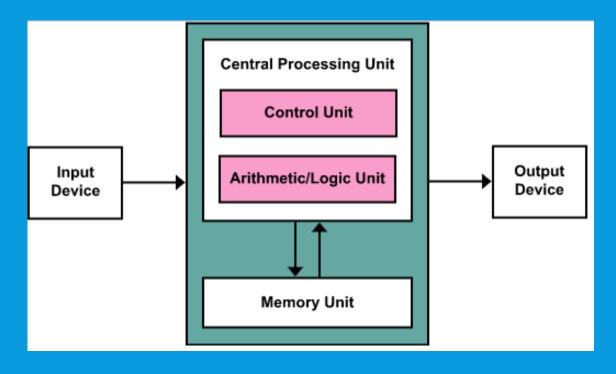
- Parallel computers can be divided into two main categories.
 - **Control flow** based on sequential machine architecture(von Neumann Machine).

• **Data flow** not based on sequential machine. No pointer to next instruction the control is distributed. The instruction triggered when the data is available.



John von Neumann





By Kapooht - Own work, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=25789639



• In 1966, Flynn proposed a four-way classification of computer systems based on instruction streams and data streams. Namely SISD, SIMD, MISD, MIMD.

	Single Data Stream	Multi Data Stream	
Single Instruction Stream	SISD	SIMD	
Multi Instruction Stream	MISD	MIMD	



- SISD: represents ordinary "uniprocessor" machines.
- SIMD : several processors directed by instructions issued from a central control unit, with array of data "array or vector processors."
- MISD : Not widely used.
- MIMD : includes a wide class of computers: shared memory, distributed memory, message passing, etc.



• Johnson 1988, proposed a further classification of MIMD machines based memory structure.

	Shared Variables Message Passing	
Global Memory	GMSV	GMMP
Distributed Memory	DMSV	DMMP



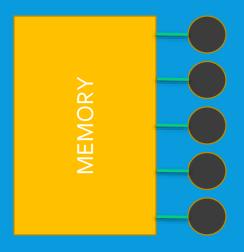
Visit the Top 500 website:

https://www.top5oo.org/

What the term GFlop/s or TFlop/s mean?



GMSV: Shared Memory Multiprocessor.

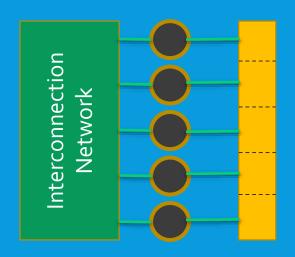




- **GMMP**:?

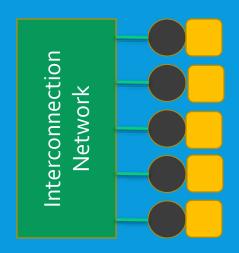


DMSV: Distributed Shared Memory (single address space).



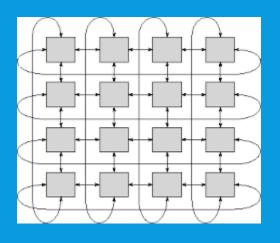


DMMP: Distributed Memory Multicomputer.

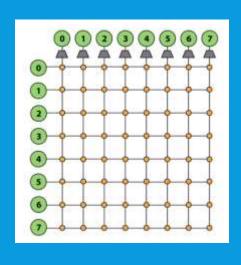


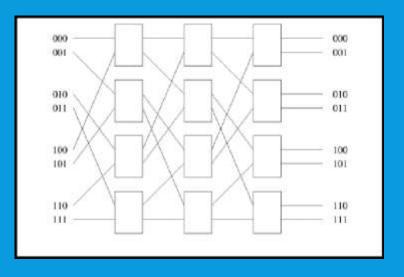


Interconnection Networks Example:



2D Mesh





Crossbar

Multistage



- PRAM : Parallel Random Access Machine.
 - Shared memory abstract machine.
 - Used to model parallel algorithmic performance.
 - EREW
 - ERCW
 - CREW
 - CRCW



- NUMA: Non-Uniform Memory Access Machine.
 - A design of a distributed memory machine.

The access time to memory depends on the location of the memory.

UMA: Uniform Memory Access Machine. (cross bar, multistage switching)



- How to measure the benefit of parallel computing?
- It is measured by the time it takes to complete a task on a single processor versus the time it takes to complete the same task on *P* parallel processors.



Speedup:

T1: Serial time (time to complete the task on single processor).

Tp: parallel time(time to complete the task on p processors).

n: problem size.

$$Sp = \frac{T1(n)}{Tp(n)}$$



• Efficincey:

T1: Serial time.

Tp: parallel time.

p : Number of processors.

$$Ep = \frac{T1(n)}{p Tp(n)} \text{ or } Ep = \frac{Sp}{p}$$



Limits of speedup & efficiency:

$$1 \le Sp \le p$$

$$0 \le Ep \le 1$$



Р	T1	Тр	Sp	Ер
2	20	10	2	1
2	20	16	1.25	0.625
4	20	10	2	0.5
8	20	5	4	0.5



What causes communication overhead:

Interconnection network delay. Transmitting data across the interconnection network suffers from bit propagation delay, message/data transmission delay, and queuing delay within the network. These factors depend on the network topology, the size of the data being sent, the speed of operation of the network, etc.



What causes communication overhead:

Memory bandwidth. No matter how large the memory capacity is, access to memory contents is done using a single port that moves one word in or out of the memory at any given memory access cycle.



What causes communication overhead:

Memory collisions, when two or more processors attempt to access the same memory module. Arbitration must be provided to allow one processor to access the memory at any given time.



What causes communication overhead:

Memory wall. The speed of data transfer to and from the memory is much slower than processing speed. This problem is being solved using memory Hierarchy or cache.