King Saud University
Department of Computer Science
CSC227: Operating Systems
Tutorial – Chapter 8: Main Memory

Exercise 1)

Assume that we have the following jobs to be scheduled using FCFS algorithm with variable partition memory scheme:

Job	Size	CPU
1	50k	13
2	120k	3
3	70k	9
4	20k	3
5	105k	8
6	55k	13

Memory size is 256k. Jobs are initially loaded in memory as follows:

J1	50k
J2	120k
J3	70k
16k	

Show how the memory will look after scheduling job 6 (assume no memory compaction is allowed) using both FCFS and Best Fit strategies.

J1	50K
J2	120K
J3	70K
16K	

50K	
J2	120K
J3	70K
16K	

J4	20K
30K	
J2	120K
J3	70K
16K	

J4	20K
150K	
J3	70K
16K	

J4	20K
J5	105K
45K	
J3	70K
16K	

J4	20k
J5	105k
131k	

J4	20k
J5	105k
J6	55k
76k	

Exercise 2)

Given memory partitions of 100K, 500K, 200K, 300K, and 600K (in order), how would each of the First-fit, Best-fit, and Worst-fit algorithms place processes of 212K, 417K, 112K, and 426K (in order)? Which algorithm makes the most efficient use of memory?

First Fit:

- 212k takes 500k, remaining 288k.
- 417k takes 600k, remaining 183k.
- 112k takes 288k, remaining 176k *288k from step 1.
- 426k waits as not enough memroy available.

Best Fit:

- 212k takes 300k, remaining 88k.
- 417k takes 500k, remaining 83k.
- 112k takes 288k, remaining 200k.
- 426k takes 600k, remaining 174k.

Worst Fit:

- 212k takes 600k, remaining 388k.
- 417k takes 500k, remaining 83k.
- 112k takes 388k, remaining 276k *288k from step 1.
- 426k waits as not enough memroy available.

Exercise 3)

Consider a paged memory of 64 pages of 256 bytes each.

a) What is the size of the virtual space and the number of bits of a virtual address?
Virtual space size is $2^6 \times 2^8 = 2^{14}$
Number of bits of a virtual address is 14.

b) Assume that the free frame list is {29,4,18,5,22,15,7,2} and two programs P1(4 pages), P2(2 pages) are waiting to be loaded. Perform the memory allocation of P1 and P2 and show the their PMT's.
P1's PMT:

0	29
1	4
2	18
3	5

P2's PMT:

0	22
1	15

c) Assume that PMT is kept in memory and two register associative memory. The access time to the memory is 480ns and the access to associative memory is 50ns, what is the effictive access time to the memory if the hit ratio in the associative memory is 50% ? 90%?

Effective access time (EAT)= (acacess time for associative memory + access time for memory) × hit ratio + (access time for associative memory + 2 × access time for memory) × miss ratio

If hit ration is 50%:

EAT = (50 + 480) × 0.50 + (50 + 2 × 480) × 0.50 = 265 + 505 = 770ns

If hit ration is 90%:

EAT = (50 + 480) × 0.90 + (50 + 2 × 480) × 0.10 = 477 + 101 = 578ns

Exercise 4)

Given a logical address filed with the following format:

Page #	**Page Offset**
16-bits	8-bits

a) What is the size of a page?

2^8 bytes = 256 byte.

b) What is the maximum number of pages?

2^{16} pages.

c) What is the maximum size of page table (PT)? assume each page entry requires 4 bytes.

PT size = number of pages (each page has one entry in the PT) × size of each entry

= $2^{16} \times 4 = 2^{16} \times 2^2 =$ **2^{18} bytes**

= $(2^{18} \div 2^{10})$ KB = 2^8 KB = **256 KB**.

d) Consider that PT is stored in physical memory, the memory access time is 100ns and the access time to associateve memory is 10ns. If th hit ratio is 80%, what is the effective access time (EAT)?

EAT = (access time for associative memory for page# + access time for memory) × hit ratio + (access time for associative memory for page# + access time for memory for PT + access time for memory) × (1 - hit ratio)

= (110 × 0.80) + (10 + 100 + 100) × (0.20) = 135ns

e) Under what condition is an associtive memory effective?

High hit ratio

Exercise 5)

Consider a paging system with the page table stored in memory.

a) If a memory reference takes 200 nanoseconds, how long does a paged memory reference take?

Two memory accesses are required to resolve the address which implies that the access time would be 2 ×200 = 400ns

b) If we add associative registers, and 75 percent of all page-table references are found in the associative registers, what is the effective memory reference time? (Assume that finding a page-table entry in the associative registers takes zero time, if the entry is there.)

EAT = (0 + 200) × 0 .75 + (0 + 200 + 200) × 0.25 = 250 ns.

Exercise 6)

Consider the following segment table:

Segment	Base	Length	Last Addrress
0	219	600	819
1	2300	14	2314
2	90	100	190
3	1327	580	1907
4	1952	96	2048

What are the physical addresses for the following logical addresses:

a) 0,430

A logical address in segmentation is in the form (segment#, offset), therefore the physical address would be: the base of the segment + offset

219 + 430 = 649

b) 1,10

2300 + 10 = 2310

c) 2,500

90 + 500 = 590 (illegal reference, trap to operating system)

d) 3,400

1327 + 400 = 1727

e) 4,112

1952 + 112 = 2064

Exercise 7)

Consider a segmentation system where virtual space can have up to 2^{14} segments of 2^{18} bytes

a) How many bits represent the address field?

14 (for segment number) + 18 (for offset) = 32 bits

b) Assume a program P1 is loaded into memory with the following SMT:

Limit	Base
4000	1000
8000	2000

Translate the address (1,50) to an absolute address.

2000+50 = 2050

c) If the access time to the memory is 200 ns and associative memory access time is 4 ns, what is the effective access time if hit ratio is 80%,

EAT = (4 + 200) × 0 .8 + (4 + 200 + 200) × 0.2 = 244 ns.

Exercise 8)

Consider a logical address space of 256 pages with a 4-KB page size, mapped onto a physical memory of 64 frames.

a) How many bits are required in the logical address?

256 pages = 2^8 pages → we need 8 bits to represent the page number.

4KB = $2^2 \times 2^{10}$ bytes = 2^{12} bytes → we need 12 bits to represent the offset.

Hence, we need 8 + 12 = 20 bits for the logical address.

b) How many bits are required in the physical address?
64 frames = 26 frames → We need 6 bits to represent the frame number.
From (a), we concluded that we need 12 bits for the offset.
Hence, we need 6 + 12 = 18 bits for the physical address.

Exercise 9)

Consider a computer system with a 32-bit logical address and 4-KB page size. The system supports up to 512 MB of physical memory. How many entries are there in each of the following?

a) A conventional, single-level page table.
4-KB page size means the offset will require 12 bits, leaving 20 bits to represent the page number. Therefore, the PT will have 2^{20} entries.

b) An inverted page table.
The IPT contains one entry for each frame in the physical memory.
Number of frames = Size of physical memory ÷ Frame size
Size of physical memory = 512 MB = ($2^9 \times 2^{20}$) bytes = 2^{29} bytes.
Frame size = page size = 4 KB = $2^2 \times 2^{10}$ bytes = 2^{12} bytes.
Number of frames = $2^{29} \div 2^{12} = 2^{17}$
Hence, number of entries in the IPT is 2^{17} entries.

Exercise 10)

Assuming a 1-KB page size, what are the page numbers and offsets for the following address references (provided as decimal numbers):

a) 3085
Each page contains 1024 bytes.
3085 ÷ 1024 = 3.01 →
page = 3; offset = 3085 – (1024 × 3) = 13

b) 42095
page = 41; offset = 111

c) 2000001
page = 1953; offset = 129