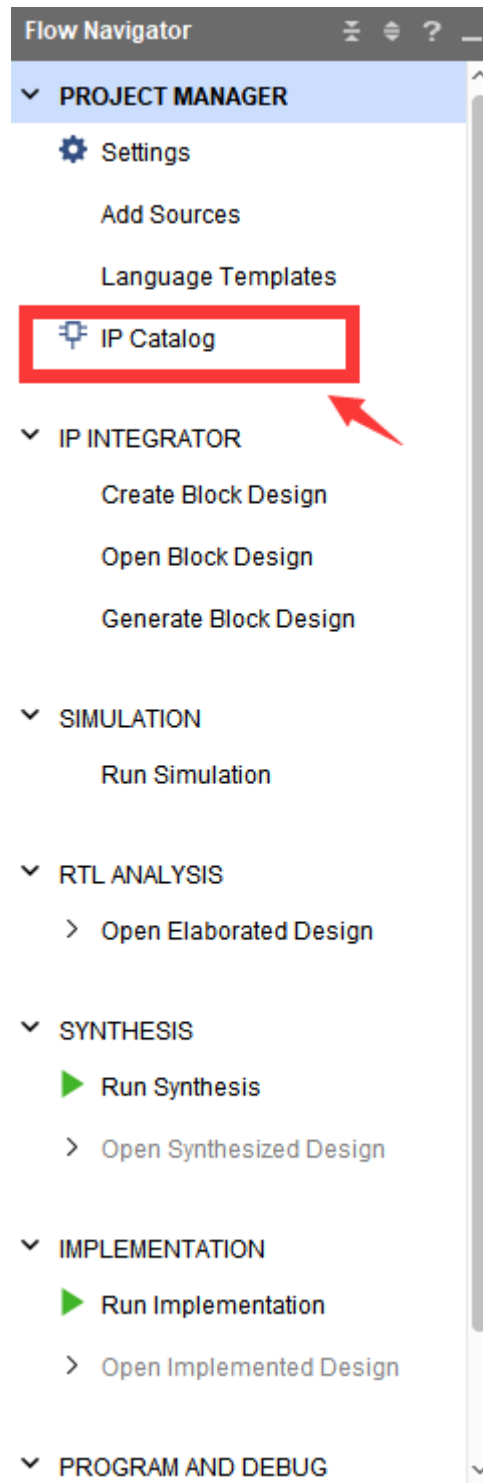


How to use IP Core

(1)Select IP Catalog



(2)Search ROM IP Core

The screenshot shows the IP Catalog interface with a search filter 'rom' applied. The results are organized into a table with columns: Name, AXI4, Status, License, and VLN. The 'Block Memory Generator' is highlighted with a red box and a red arrow pointing to its VLN value 'xilinx.com:ip:blk_mem_gen:8.4'.

Name	AXI4	Status	License	VLN
Vivado Repository				
Alliance Partners				
OmniTek				
Chroma Down-Sampler	AXI4, AXI4-Stream	Production	Purchase	omnitek.tv/ip:omni_chroma_down.0.0
Chroma Up-Sampler	AXI4, AXI4-Stream	Production	Purchase	omnitek.tv/ip:omni_chroma.0.0
Chroma Up-Sampler 420 to 422	AXI4, AXI4-Stream	Production	Purchase	omnitek.tv/ip:omni_chroma_420_to_422.0.0
Memories & Storage Elements				
RAMs & ROMs				
Distributed Memory Generator		Production	Included	xilinx.com:ip:dist_mem_gen:8.0
RAMs & ROMs & BRAM				
Block Memory Generator	AXI4	Production	Included	xilinx.com:ip:blk_mem_gen:8.4
Video & Image Processing				

(3)Select Signal Port Rom

The screenshot shows the 'Block Memory Generator (8.4)' configuration window. The 'Component Name' is 'blk_mem_gen_0'. The 'Memory Type' is set to 'Single Port ROM', which is highlighted with a red box. The 'Interface Type' is 'Native'. The 'ECC Options' section shows 'ECC Type' as 'No ECC' and 'Error Injection Pins' as 'Single Bit Error Injection'. The 'Write Enable' section shows 'Byte Write Enable' as 'No' and 'Byte Size (bits)' as '9'. The 'Algorithm Options' section shows 'Algorithm' as 'Minimum Area' and 'Primitive' as '8kx2'.

Block Memory Generator (8.4)

Documentation IP Location Switch to Defaults

IP Symbol Power Estimation

Show disabled ports

Component Name: blk_mem_gen_0

Basic Port A Options Other Options Summary

Interface Type: Native ☐ Generate address interface with 32 bits

Memory Type: **Single Port ROM** ☐ Common Clock

ECC Options

ECC Type: No ECC

☐ Error Injection Pins: Single Bit Error Injection

Write Enable

☐ Byte Write Enable

Byte Size (bits): 9

Algorithm Options

Defines the algorithm used to concatenate the block RAM primitives. Refer datasheet for more information.

Algorithm: Minimum Area

Primitive: 8kx2

OK Cancel

(4) Select Rom Width and Depth

Customize IP

Block Memory Generator (8.4)

Documentation IP Location Switch to Defaults

IP Symbol Power Estimation

☐ Show disabled ports

Component Name: blk_mem_gen_0

Basic Port A Options Other Options Summary

Memory Size

Port A Width: 16 Range: 1 to 4608 (bits)

Port A Depth: 40000 Range: 2 to 1048576

The Width and Depth values are used for Read Operation in Port A

Operating Mode: Write First Enable Port Type: Always Enabled

Port A Optional Output Registers

☒ Primitives Output Register ☐ Core Output Register

☐ SoftECC Input Register ☐ REGCEA Pin

Port A Output Reset Options

☐ RSTA Pin (setreset pin) Output Reset Value (Hex): 0

☐ Reset Memory Latch Reset Priority: CE (Latch or Register Enable)

READ Address Change A

☐ Read Address Change A

OK Cancel

BRAM_PORTA

- addra[15:0]
- clka
- douta[15:0]

(5) Select .coe file

Customize IP

Block Memory Generator (8.4)

Documentation IP Location Switch to Defaults

IP Symbol Power Estimation

☐ Show disabled ports

Component Name: blk_mem_gen_0

Basic Port A Options Other Options Summary

Pipeline Stages within Mux: 0 Mux Size: 10x1

Memory Initialization

☒ Load Init File

Coe File: /ers/p500/Desktop/rom/Image_process/lena_RGB565.coe Browse Edit

☐ Fill Remaining Memory Locations

Remaining Memory Locations (Hex): 0

Structural/UniSim Simulation Model Options

Defines the type of warnings and outputs are generated when a read-write or write-write collision occurs.

Collision Warnings: All

Behavioral Simulation Model Options

☐ Disable Collision Warnings ☐ Disable Out of Range Warnings

OK Cancel

BRAM_PORTA

- addra[15:0]
- clka
- douta[15:0]

(6)Generate Output Products

