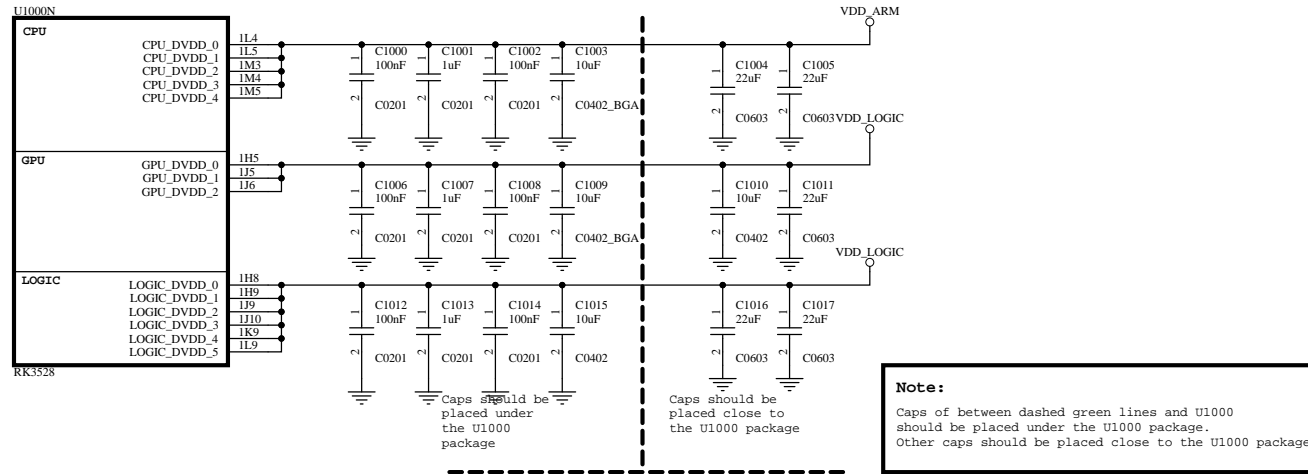
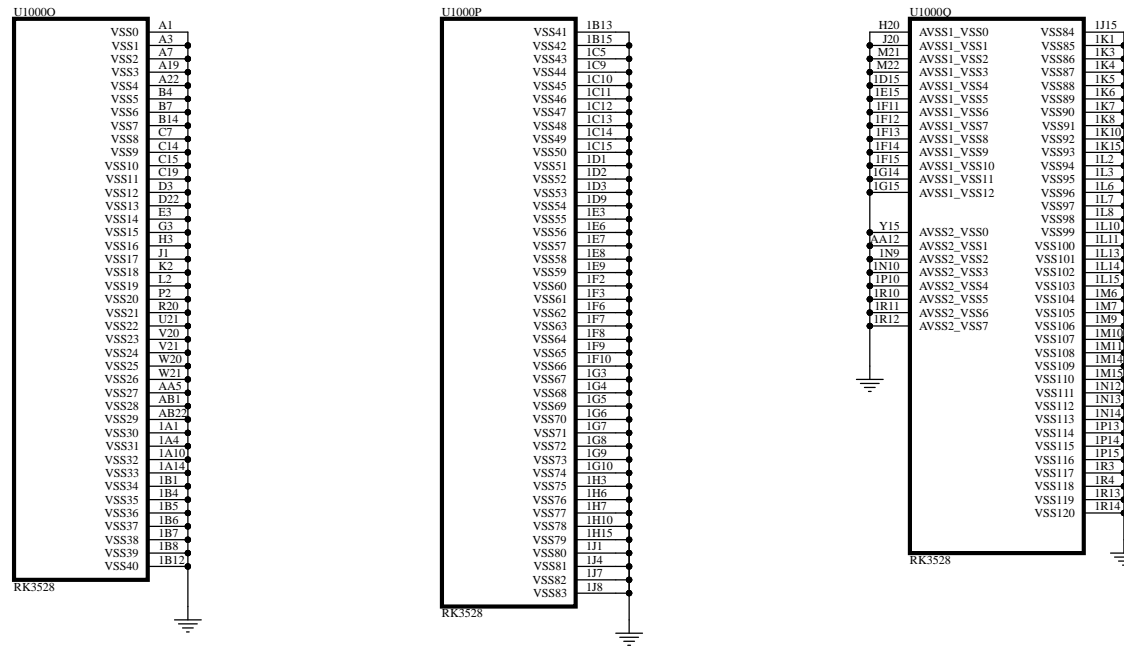


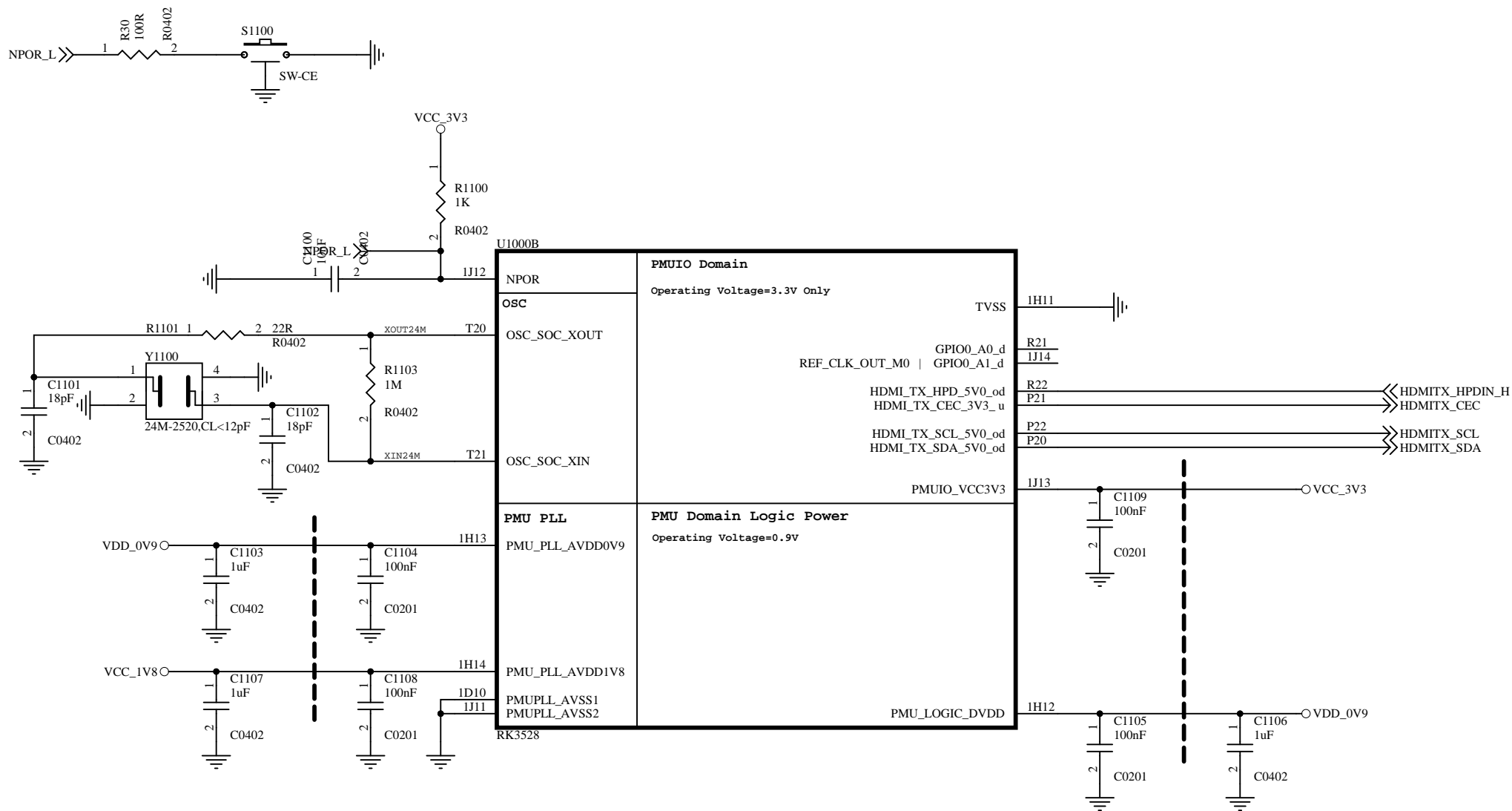
## RK3528\_N(POWER)



## RK3528\_O/P/Q(GND)



# RK3528\_B(OSC/PLL/PMUIO Domain)



## Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

# RK3528\_A(DDR PHY)

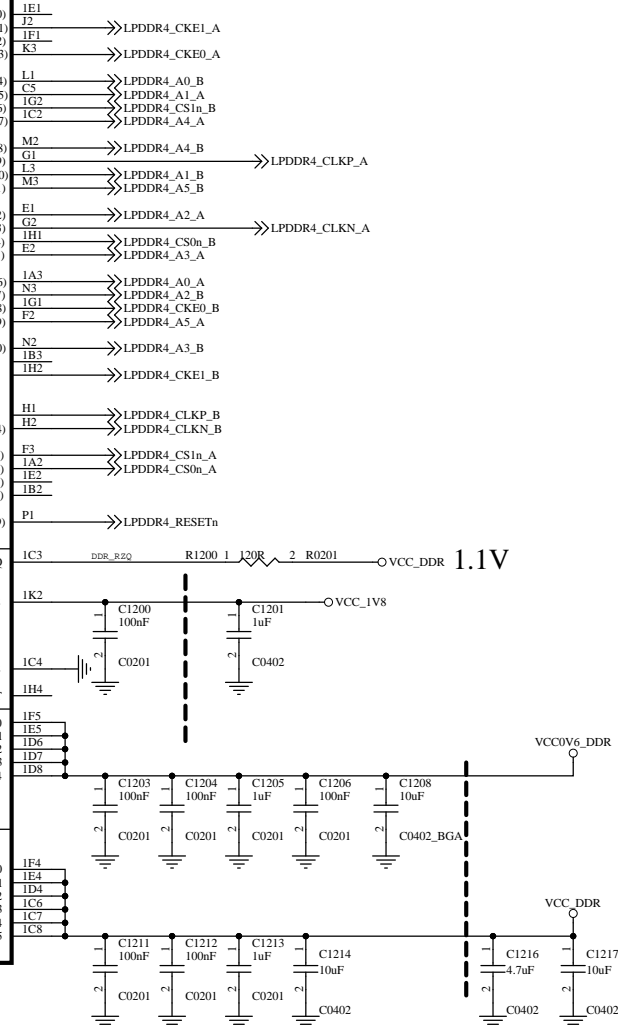
U1000A

		DDR4	LPDDR4	DDR3	LPDDR3
LPDDR4_DQ0_A << C4	DDRRPHY_A_DQ0	DDR4_DQ0_6_A	LPDDR4_DQ0_A	DDR3_D4	LPDDR3_D0
LPDDR4_DQ1_A << B5	DDRRPHY_A_DQ1	DDR4_DQ1_2_A	LPDDR4_DQ1_A	DDR3_D0	LPDDR3_D1
LPDDR4_DQ2_A << B8	DDRRPHY_A_DQ2	DDR4_DQ1_0_A	LPDDR4_DQ2_A	DDR3_D2	LPDDR3_D2
LPDDR4_DQ3_A << A8	DDRRPHY_A_DQ3	DDR4_DQ1_1_A	LPDDR4_DQ3_A	DDR3_D1	LPDDR3_D3
LPDDR4_DQ4_A << B9	DDRRPHY_A_DQ4	DDR4_DQ1_4_A	LPDDR4_DQ4_A	DDR3_D6	LPDDR3_D4
LPDDR4_DQ5_A << C13	DDRRPHY_A_DQ5	DDR4_DQ1_5_A	LPDDR4_DQ5_A	DDR3_D7	LPDDR3_D5
LPDDR4_DQ6_A << A8	DDRRPHY_A_DQ6	DDR4_DQ1_7_A	LPDDR4_DQ6_A	DDR3_D5	LPDDR3_D6
LPDDR4_DQ7_A << A8	DDRRPHY_A_DQ7	DDR4_DQ1_3_A	LPDDR4_DQ7_A	DDR3_D3	LPDDR3_D7
LPDDR4_DM0_A << C3	DDRRPHY_A_DM0	DDR4_DML_A	LPDDR4_DM0_A	DDR3_DM0	LPDDR3_DM0
LPDDR4_DQS0P_A << A6	DDRRPHY_A_DQS0P	DDR4_DQSL_P_A	LPDDR4_DQS0P_A	DDR3_DQS0P	LPDDR3_DQS0P
LPDDR4_DQS0N_A << B6	DDRRPHY_A_DQS0N	DDR4_DQSL_N_A	LPDDR4_DQS0N_A	DDR3_DQS0N	LPDDR3_DQS0N
LPDDR4_DQ8_A << C1	DDRRPHY_A_DQ8	DDR4_DQ1_1_A	LPDDR4_DQ8_A	DDR3_D12	LPDDR3_D19
LPDDR4_DQ9_A << C2	DDRRPHY_A_DQ9	DDR4_DQ1_5_A	LPDDR4_DQ9_A	DDR3_D14	LPDDR3_D16
LPDDR4_DQ10_A << B9	DDRRPHY_A_DQ10	DDR4_DQ1_0_A	LPDDR4_DQ10_A	DDR3_D15	LPDDR3_D21
LPDDR4_DQ11_A << D2	DDRRPHY_A_DQ11	DDR4_DQ1_2_A	LPDDR4_DQ11_A	DDR3_D9	LPDDR3_D17
LPDDR4_DQ12_A << B3	DDRRPHY_A_DQ12	DDR4_DQ1_7_A	LPDDR4_DQ12_A	DDR3_D10	LPDDR3_D20
LPDDR4_DQ13_A << B3	DDRRPHY_A_DQ13	DDR4_DQ1_5_A	LPDDR4_DQ13_A	DDR3_D8	LPDDR3_D23
LPDDR4_DQ14_A << A7	DDRRPHY_A_DQ14	DDR4_DQ1_4_A	LPDDR4_DQ14_A	DDR3_D13	LPDDR3_D22
LPDDR4_DQ15_A << C11	DDRRPHY_A_DQ15	DDR4_DQ1_6_A	LPDDR4_DQ15_A	DDR3_D11	LPDDR3_D18
LPDDR4_DM1_A << B1	DDRRPHY_A_DM1	DDR4_DMU_A	LPDDR4_DM1_A	DDR3_DM1	LPDDR3_DM2
LPDDR4_DQS1P_A << B2	DDRRPHY_A_DQS1P	DDR4_DQSL_P_A	LPDDR4_DQS1P_A	DDR3_DQS1P	LPDDR3_DQS1P
LPDDR4_DQS1N_A << A2	DDRRPHY_A_DQS1N	DDR4_DQSL_N_A	LPDDR4_DQS1N_A	DDR3_DQS1N	LPDDR3_DQS2N
LPDDR4_DQ0_B << A14	DDRRPHY_B_DQ0	DDR4_DQ1_4_B	LPDDR4_DQ0_B	DDR3_D29	LPDDR3_D14
LPDDR4_DQ1_B << B13	DDRRPHY_B_DQ1	DDR4_DQ1_0_B	LPDDR4_DQ1_B	DDR3_D31	LPDDR3_D12
LPDDR4_DQ2_B << B11	DDRRPHY_B_DQ2	DDR4_DQ1_1_B	LPDDR4_DQ2_B	DDR3_D28	LPDDR3_D13
LPDDR4_DQ3_B << A10	DDRRPHY_B_DQ3	DDR4_DQ1_5_B	LPDDR4_DQ3_B	DDR3_D30	LPDDR3_D8
LPDDR4_DQ4_B << B11	DDRRPHY_B_DQ4	DDR4_DQ1_7_B	LPDDR4_DQ4_B	DDR3_D26	LPDDR3_D9
LPDDR4_DQ5_B << B15	DDRRPHY_B_DQ5	DDR4_DQ1_3_B	LPDDR4_DQ5_B	DDR3_D24	LPDDR3_D15
LPDDR4_DQ6_B << B10	DDRRPHY_B_DQ6	DDR4_DQ1_6_B	LPDDR4_DQ6_B	DDR3_D27	LPDDR3_D10
LPDDR4_DQ7_B << B10	DDRRPHY_B_DQ7	DDR4_DQ1_2_B	LPDDR4_DQ7_B	DDR3_D25	LPDDR3_D11
LPDDR4_DM0_B << A15	DDRRPHY_B_DM0	DDR4_DMU_B	LPDDR4_DM0_B	DDR3_DM3	LPDDR3_DM1
LPDDR4_DQS0P_B << B12	DDRRPHY_B_DQS0P	DDR4_DQSL_P_B	LPDDR4_DQS0P_B	DDR3_DQS3P	LPDDR3_DQS1P
LPDDR4_DQS0N_B << A12	DDRRPHY_B_DQS0N	DDR4_DQSL_N_B	LPDDR4_DQS0N_B	DDR3_DQS3N	LPDDR3_DQS1N
LPDDR4_DQ8_B << B18	DDRRPHY_B_DQ8	DDR4_DQ1_1_B	LPDDR4_DQ8_B	DDR3_D17	LPDDR3_D27
LPDDR4_DQ9_B << A13	DDRRPHY_B_DQ9	DDR4_DQ1_3_B	LPDDR4_DQ9_B	DDR3_D19	LPDDR3_D26
LPDDR4_DQ10_B << B20	DDRRPHY_B_DQ10	DDR4_DQ1_4_B	LPDDR4_DQ10_B	DDR3_D18	LPDDR3_D30
LPDDR4_DQ11_B << A20	DDRRPHY_B_DQ11	DDR4_DQ1_6_B	LPDDR4_DQ11_B	DDR3_D22	LPDDR3_D31
LPDDR4_DQ12_B << B19	DDRRPHY_B_DQ12	DDR4_DQ1_0_B	LPDDR4_DQ12_B	DDR3_D16	LPDDR3_D28
LPDDR4_DQ13_B << B16	DDRRPHY_B_DQ13	DDR4_DQ1_2_B	LPDDR4_DQ13_B	DDR3_D20	LPDDR3_D24
LPDDR4_DQ14_B << A11	DDRRPHY_B_DQ14	DDR4_DQ1_7_B	LPDDR4_DQ14_B	DDR3_D21	LPDDR3_D25
LPDDR4_DQ15_B << C16	DDRRPHY_B_DQ15	DDR4_DQ1_5_B	LPDDR4_DQ15_B	DDR3_D23	LPDDR3_D29
LPDDR4_DM1_B << C18	DDRRPHY_B_DM1	DDR4_DML_B	LPDDR4_DM1_B	DDR3_DM2	LPDDR3_DM3
LPDDR4_DQS1P_B << B17	DDRRPHY_B_DQS1P	DDR4_DQSL_P_B	LPDDR4_DQS1P_B	DDR3_DQS2P	LPDDR3_DQS3P
LPDDR4_DQS1N_B << A17	DDRRPHY_B_DQS1N	DDR4_DQSL_N_B	LPDDR4_DQS1N_B	DDR3_DQS2N	LPDDR3_DQS3N

RK3528  
000001-000001000000

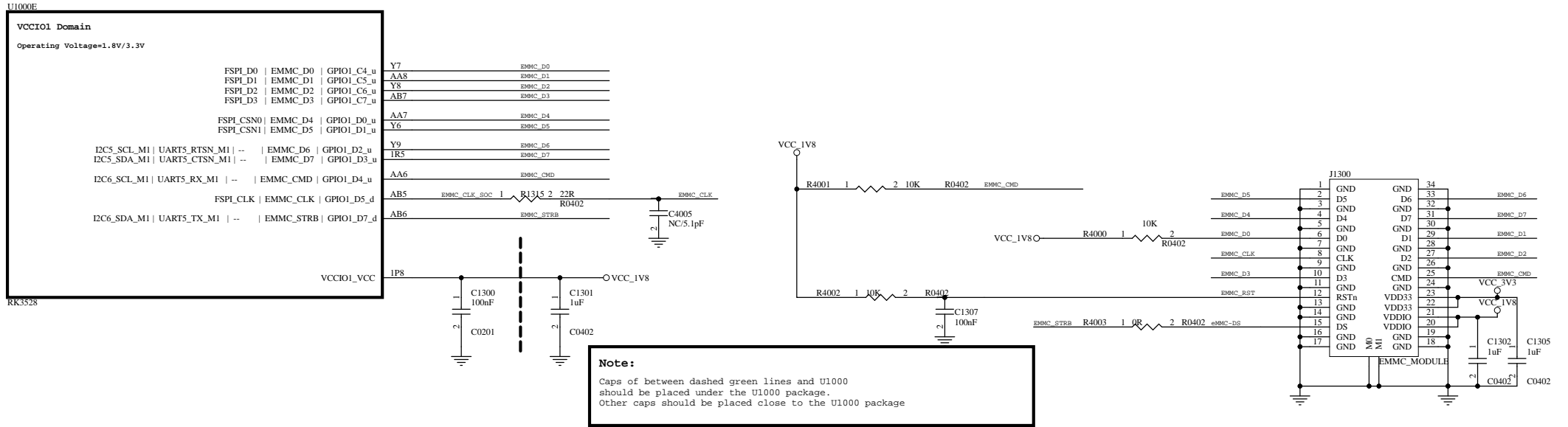
DDR4	LPDDR4	DDR3	LPDDR3	
DDR4_A0	LPDDR4_ODT1_B	DDR3_A9	LPDDR3_ODT2	DDRPHY_A0 (A
DDR4_A1	LPDDR4_CKE1_A	DDR3_A14	--	DDRPHY_A1 (A
DDR4_A2	LPDDR4_ODT0_B	DDR3_A13	LPDDR3_ODT3	DDRPHY_A2 (A
DDR4_A3	LPDDR4_CKE0_A	DDR3_A1	--	DDRPHY_A3 (A
DDR4_A4	LPDDR4_A0_B	DDR3_A2	LPDDR3_A5	DDRPHY_A4 (A
DDR4_A5	LPDDR4_A1_A	DDR3_A4	--	DDRPHY_A5 (A
DDR4_A6	LPDDR4_CS1_B	DDR3_A3	LPDDR3_CS2	DDRPHY_A6 (A
DDR4_A7	LPDDR4_A4_A	DDR3_A6	--	DDRPHY_A7 (A
DDR4_A8	LPDDR4_A4_B	DDR3_A5	LPDDR3_A6	DDRPHY_A8 (A
DDR4_A9	LPDDR4_CLKP_A	DDR3_A11	LPDDR3_A2	DDRPHY_A9 (A
DDR4_A10	LPDDR4_A1_B	DDR3_A0	--	DDRPHY_A10 (A
DDR4_A11	LPDDR4_A5_B	DDR3_A7	LPDDR3_A7	DDRPHY_A11 (A
DDR4_A12	LPDDR4_A2_A	DDR3_A10	LPDDR3_A4	DDRPHY_A12 (A
DDR4_A13	LPDDR4_CLKN_A	DDR3_A8	LPDDR3_A3	DDRPHY_A13 (A
DDR4_WEN/A14	LPDDR4_CS0_B	DDR3_ODT0	LPDDR3_CS3	DDRPHY_A14 (A
DDR4_CASN/A15	LPDDR4_A3_A	DDR3_BA1	LPDDR3_A0	DDRPHY_A15 (A
DDR4_RASN/A16	LPDDR4_A0_A	DDR3_CKE0	--	DDRPHY_A16 (A
DDR4_ACTN	LPDDR4_A2_B	DDR3_CS0	LPDDR3_A9	DDRPHY_ACTN (A
DDR4_BA0	LPDDR4_CKE0_B	DDR3_BA2	LPDDR3_CKE0	DDRPHY_BA0 (A
DDR4_BA1	LPDDR4_A5_A	DDR3_A12	LPDDR3_A1	DDRPHY_BA1 (A
DDR4_BG0	LPDDR4_A3_B	DDR3_BA0	LPDDR3_A8	DDRPHY_BG0 (A
DDR4_BG1	--	DDR3_A15	--	DDRPHY_BG1 (AC21
DDR4_CKE	LPDDR4_CKE1_B	DDR3_RASN	--	DDRPHY_CKE (AC22
DDR4_CLKP	LPDDR4_CLKP_B	DDR3_CLKP	LPDDR3_CLKP	DDRPHY_CLKP (AC23
DDR4_CLKN	LPDDR4_CLKN_B	DDR3_CLKN	LPDDR3_CLKN	DDRPHY_CLKN (AC24
DDR4_CS0	LPDDR4_CS1_A	DDR3_CASN	LPDDR3_CS1	DDRPHY_CS0 (AC
DDR4_CS1	LPDDR4_CS0_A	DDR3_CS1	LPDDR3_CS0	DDRPHY_CS1 (AC
DDR4_ODT0	LPDDR4_ODT1_A	DDR3_WEN	LPDDR3_ODT0	DDRPHY_ODT0 (AC
DDR4_ODT1	LPDDR4_ODT0_A	DDR3_ODT1	LPDDR3_ODT1	DDRPHY_ODT1 (AC
DDR4_RESETN	LPDDR4_RESETN	DDR3_RESETN	--	DDRPHY_RESETN (AC
Note: Sequences can not be swap				
DDR_R3				
DDR_PLL_AVDD1				
DDR_PLL_AV				
DDR_VREF0				
DDR3L	+1.35V	DDR_VDDQ		
DDR3	+1.5V	DDR_VDDQ		
DDR4	+1.2V	DDR_VDDQ		
LPDDR3	+1.2V	DDR_VDDQ		
LPDDR4	+1.1V	DDR_VDDQ		
LPDDR4x	+0.6V	DDR_VDDQ		
DDR3L	+1.35V	DDR_VDDQ		
DDR3	+1.5V	DDR_VDDQ		
DDR4	+1.2V	DDR_VDDQ		
LPDDR3	+1.2V	DDR_VDDQ		
LPDDR4	+1.1V	DDR_VDDQ		
LPDDR4x	+1.1V	DDR_VDDQ		

Note: Sequences can not be swap

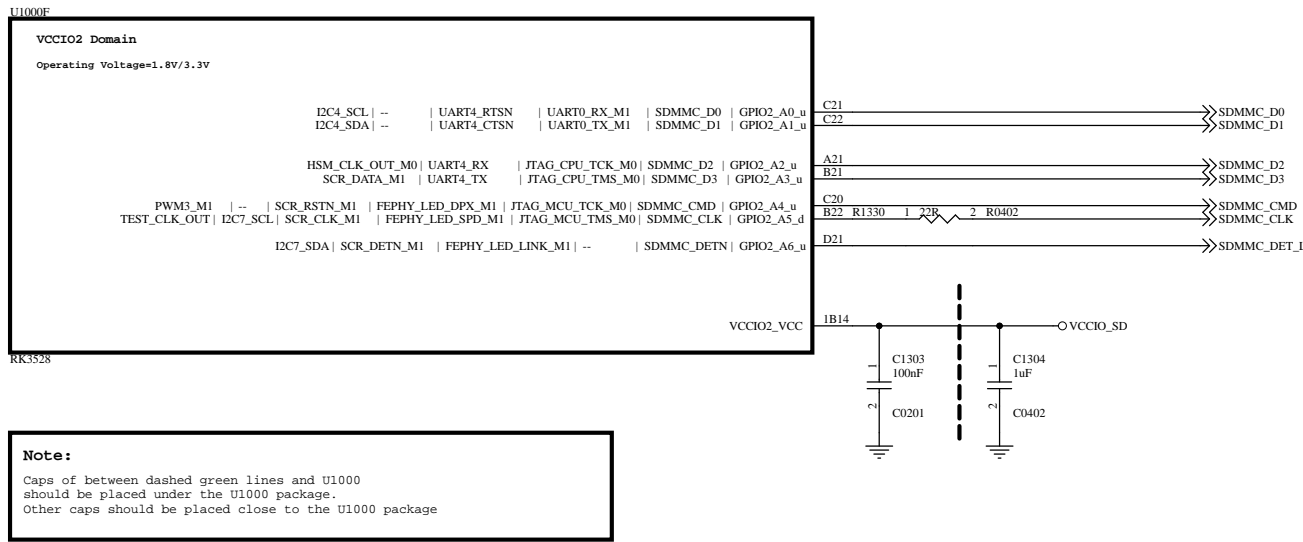


**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

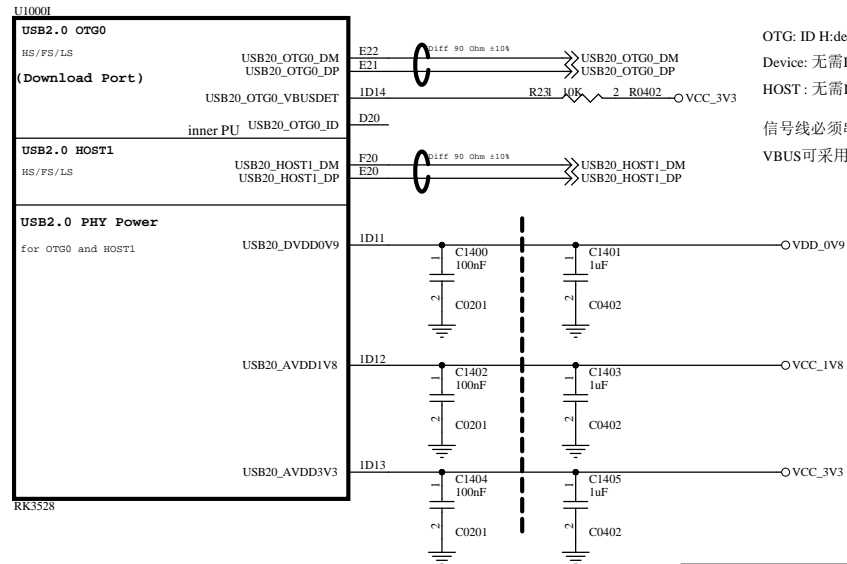
## RK3528\_E(VCCIO1 Domain)



## RK3528\_F(VCCIO2 Domain)



## RK3528\_I(USB2.0 OTG/HOST)



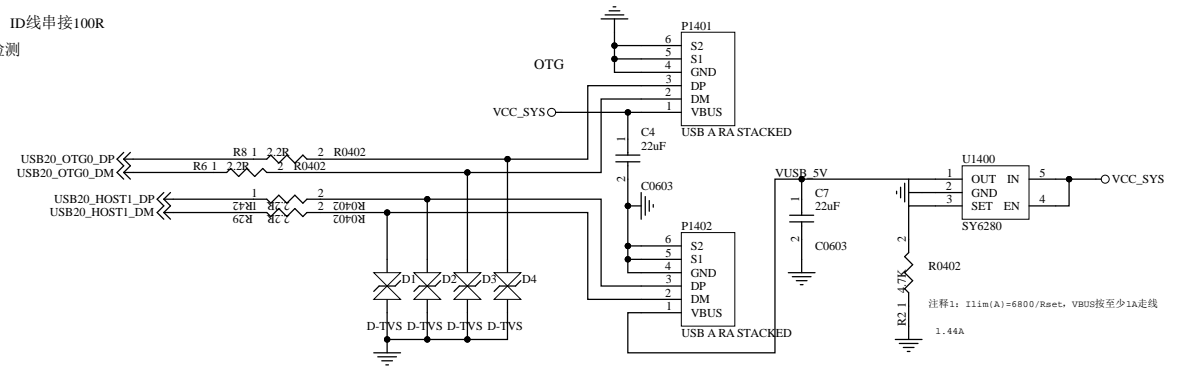
OTG: ID H:device, L:HOST. VBUS>2.3V 枚举

Device: 无需ID, 判断VBUS>2.3V, 枚举

HOST: 无需ID, 判断VBUS>2.3V, 枚举

信号线必须串接2.2ohm, ID线串接100R

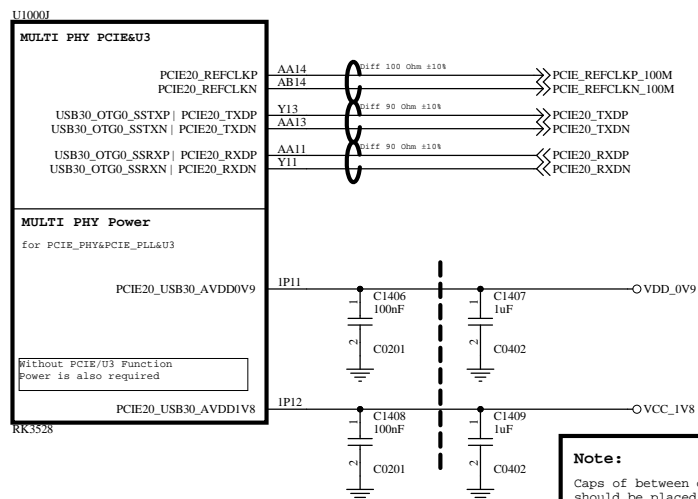
VBUS可采用电阻分压检测



### Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

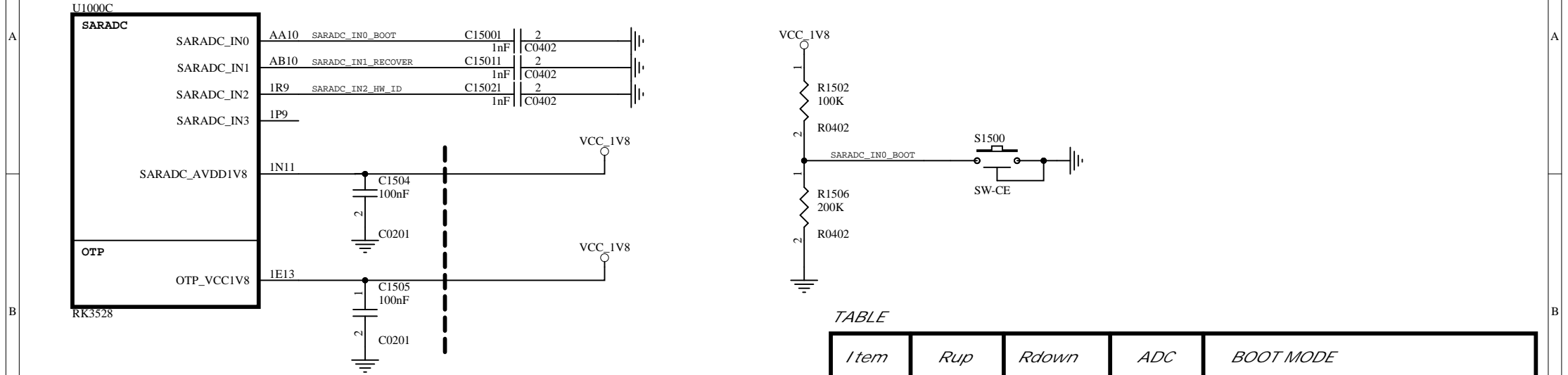
## RK3528\_J(PCIE2.0/U3 PHY)



### Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

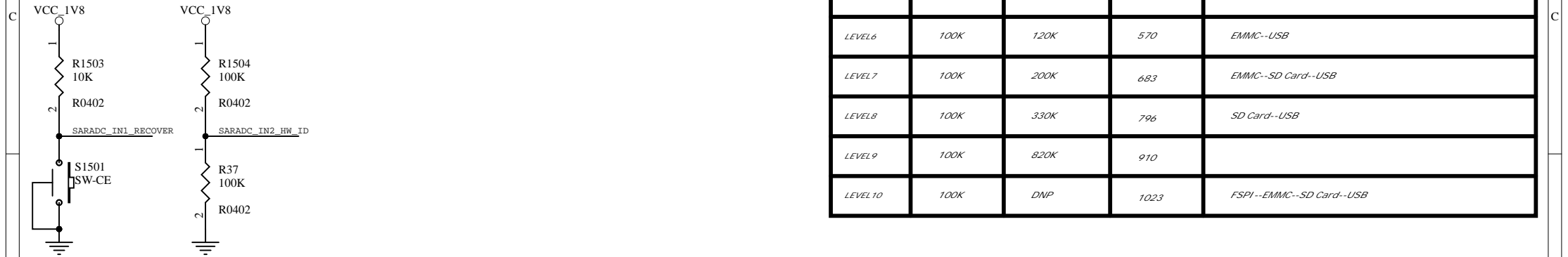
# RK3528\_C (Saradc/OTP)



**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

TABLE

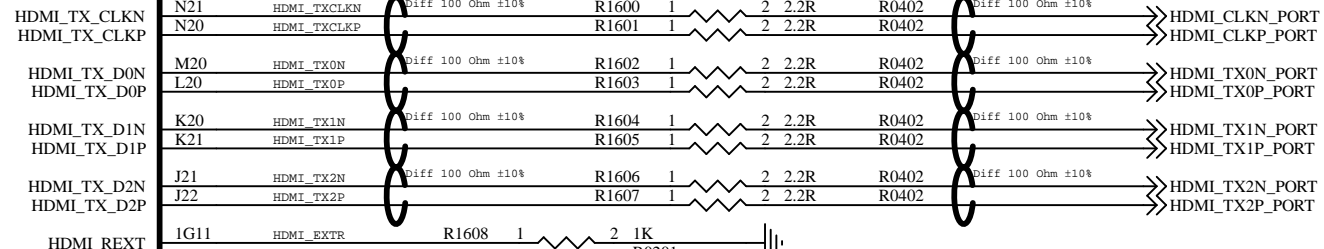
Item	Rup	Rdown	ADC	BOOT MODE
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	12K	114	
LEVEL3	100K	27K	228	FSPI--USB
LEVEL4	100K	51K	342	
LEVEL5	100K	82K	456	
LEVEL6	100K	120K	570	EMMC--USB
LEVEL7	100K	200K	683	EMMC--SD Card--USB
LEVEL8	100K	330K	796	SD Card--USB
LEVEL9	100K	820K	910	
LEVEL10	100K	DNP	1023	FSPI--EMMC--SD Card--USB



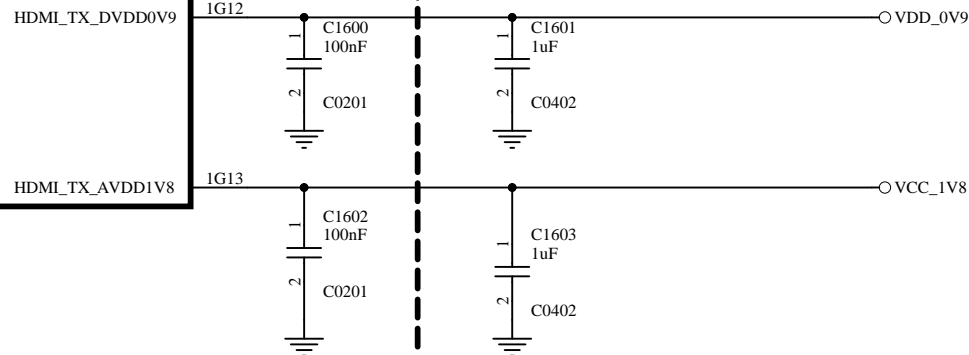
# RK3528\_L(HDMI PHY)

U1000L

## HDMI2.1 TMDS



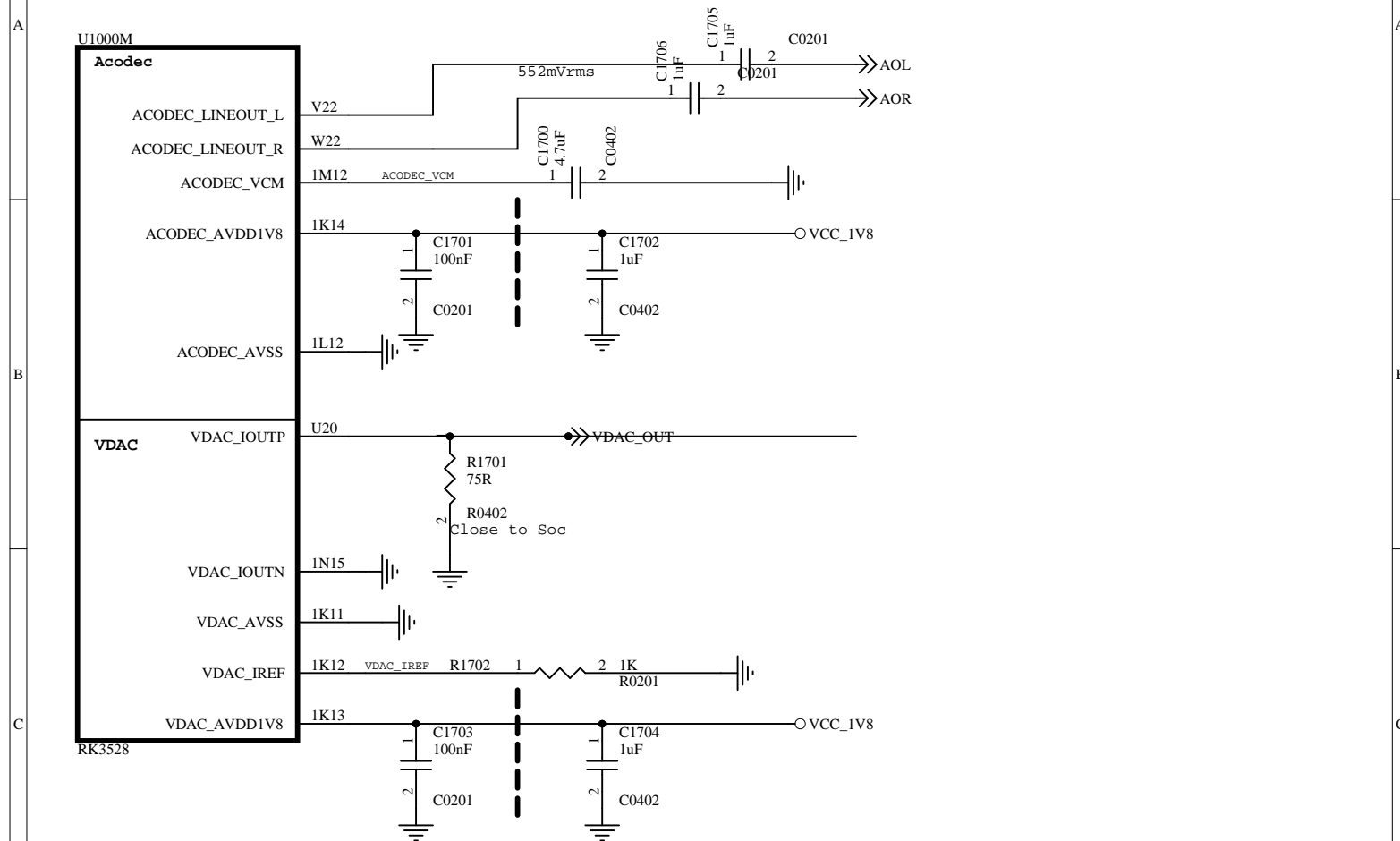
## HDMI PHY Power



## Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

# RK3528\_M(Acodec/VDAC)

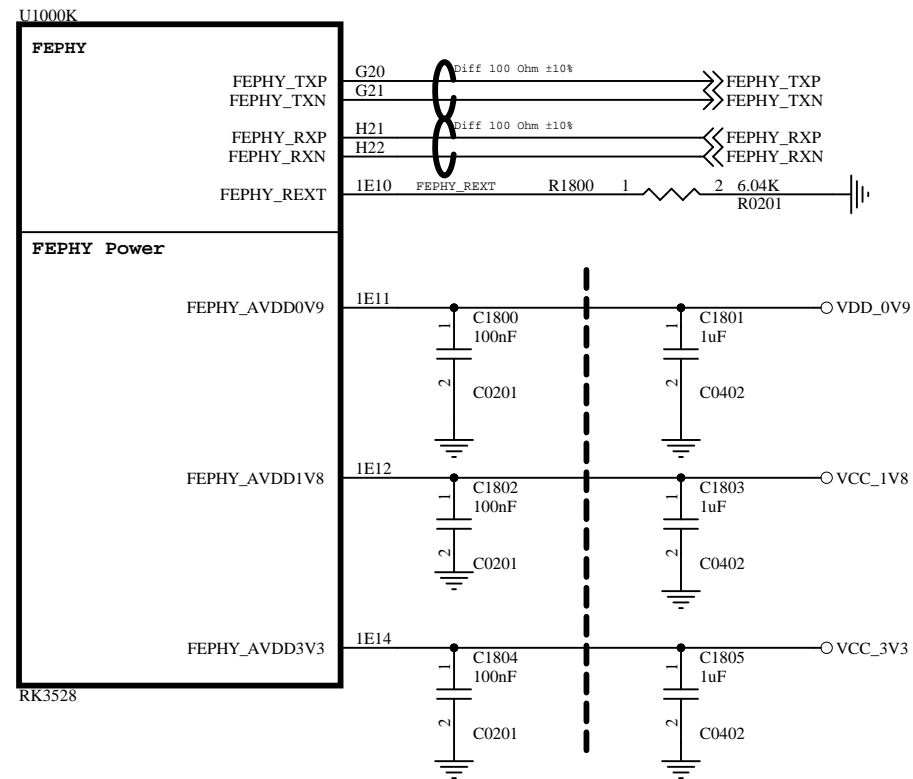


## Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package



# RK3528\_K(Embed FEPHY)



## Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

**Note:**

Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

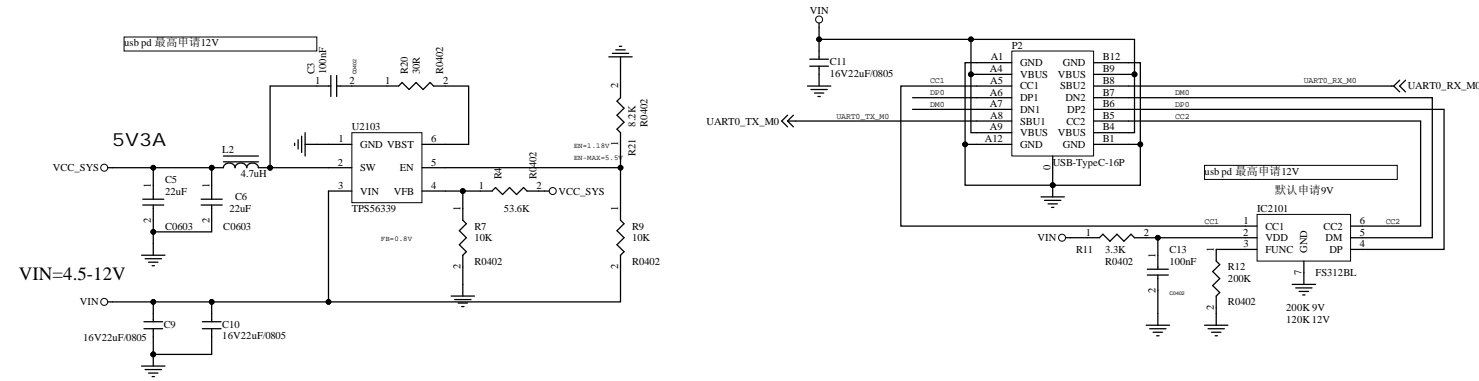
**Note:**  
Caps of between dashed green lines and U1000  
should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

**Note:**

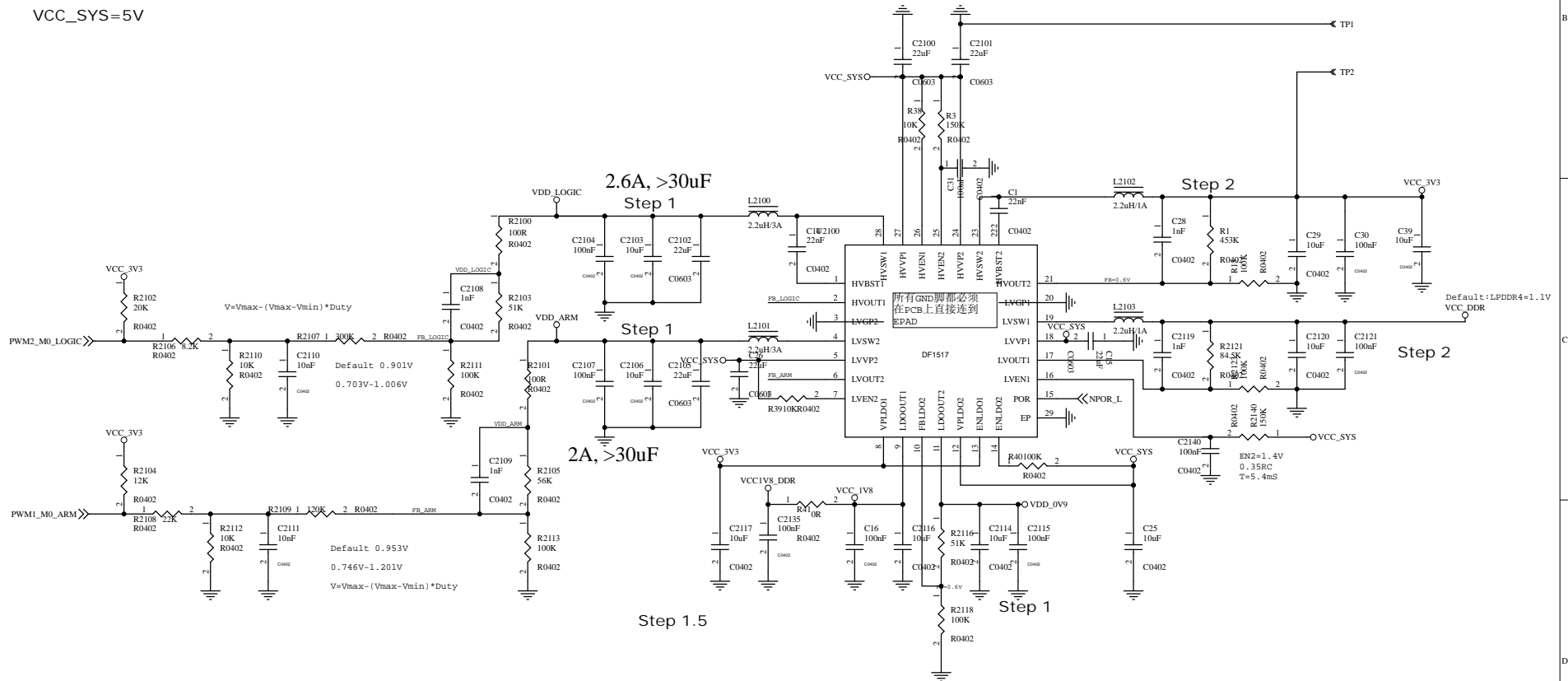
Caps of between dashed green lines and U1000 should be placed under the U1000 package.

Other caps should be placed close to the U1000 package

V\_USB-->VCC\_SYS (3.3V)

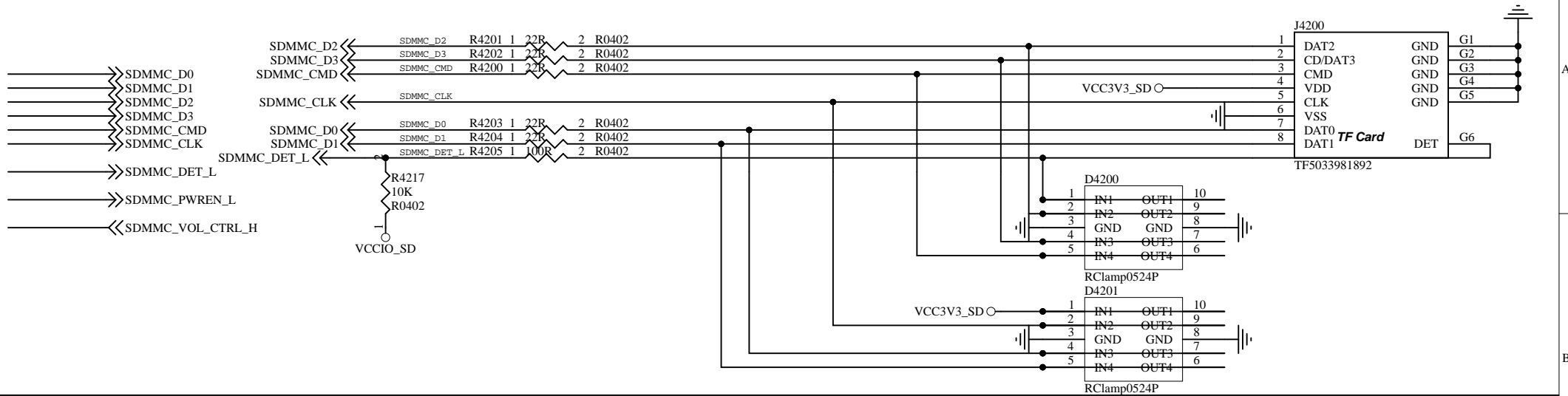


VCC\_SYS=5V

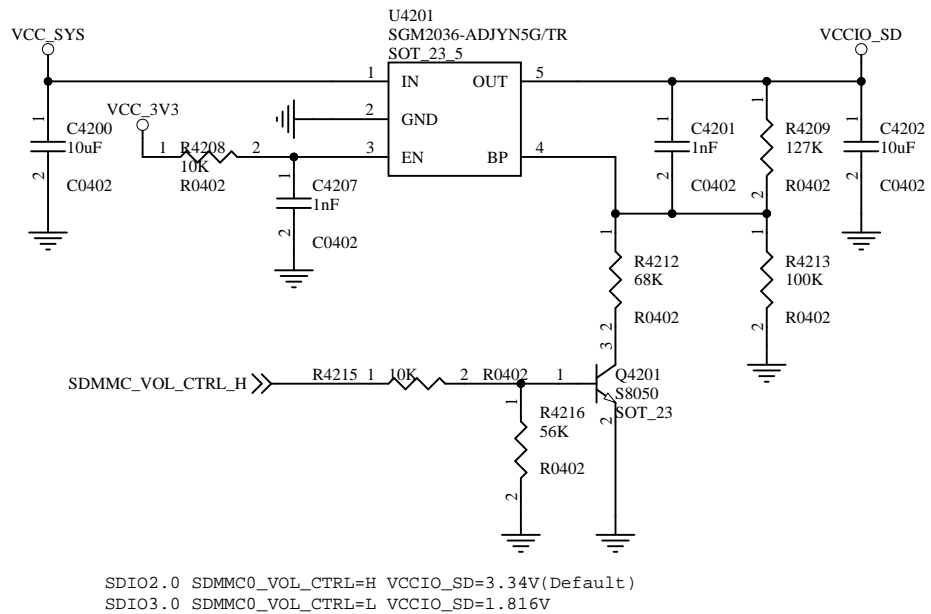




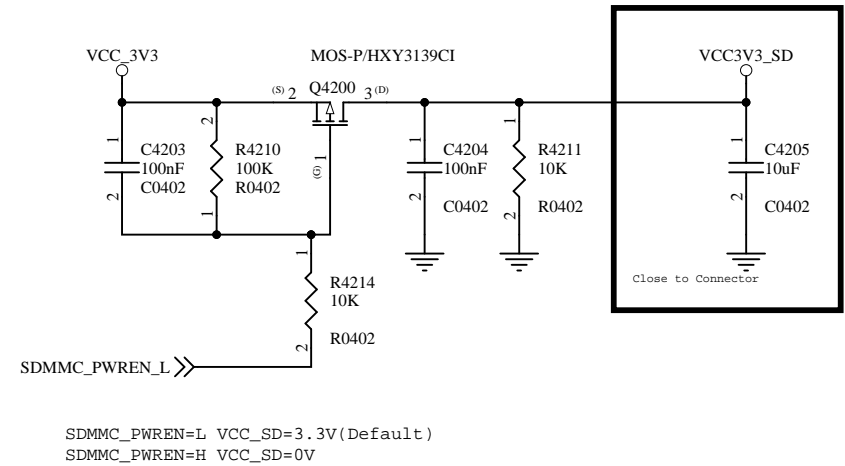
# TF Card



## VCCIO\_SD



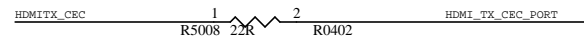
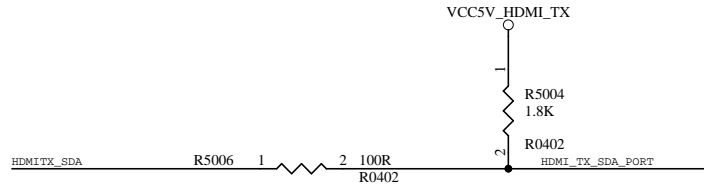
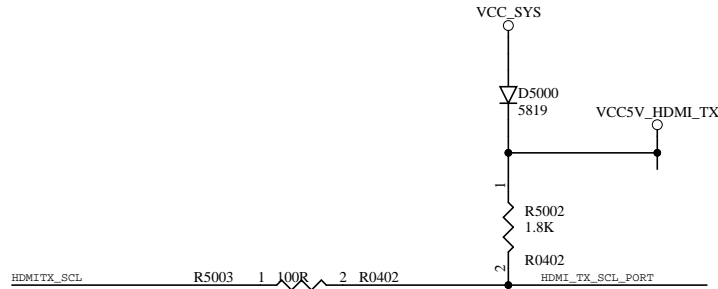
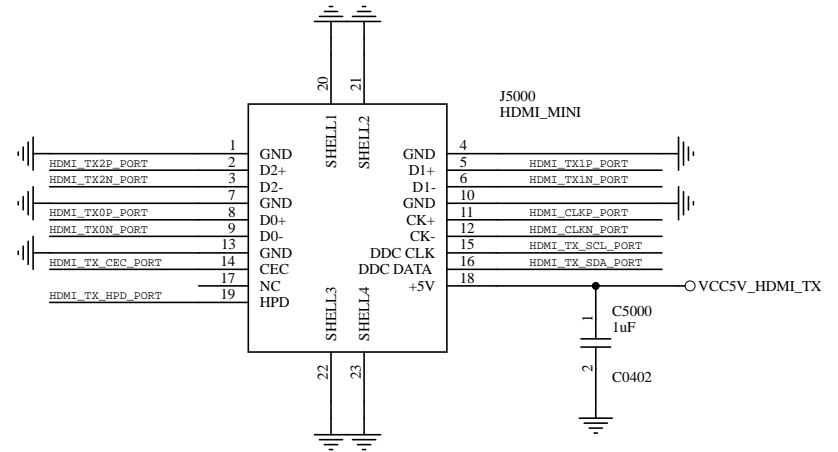
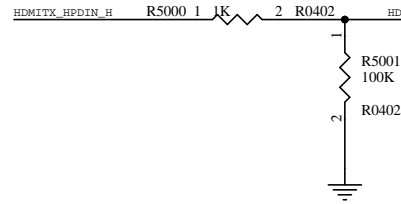
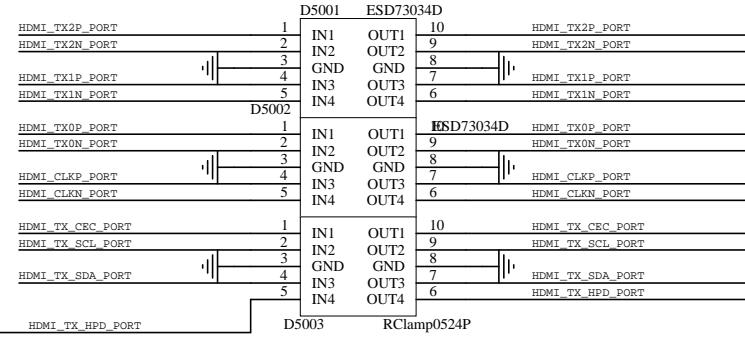
## VCC3V3\_SD



# HDMI2.0 TX

Cj<=0.2pF

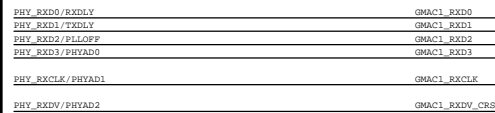
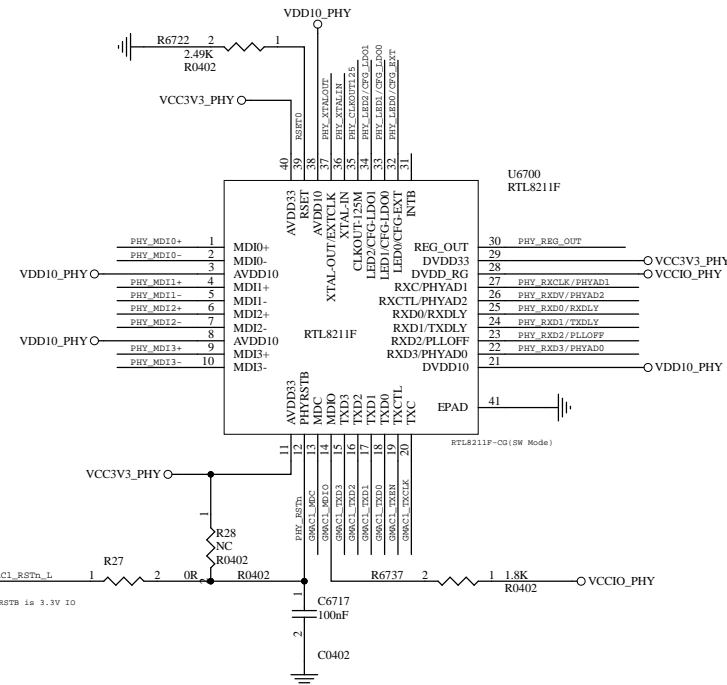
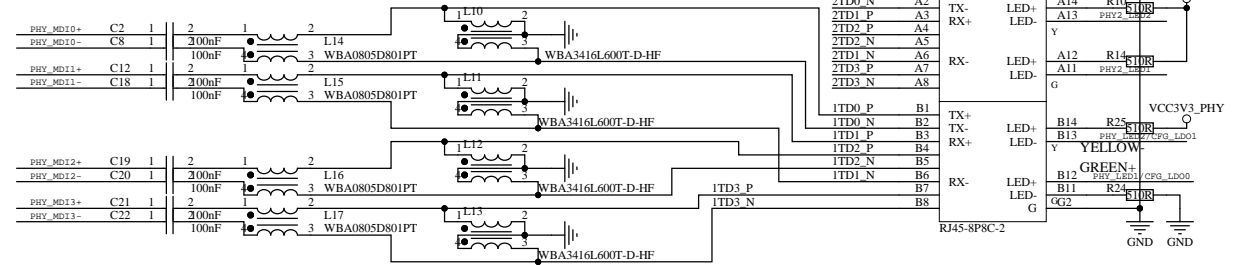
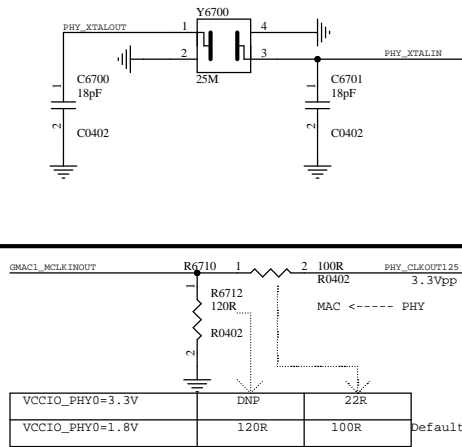
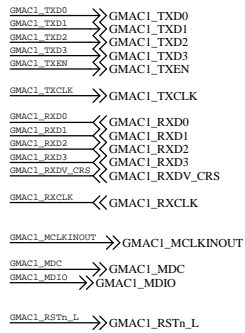
HDMI\_TX0P\_PORT >> HDMI\_TX0P\_PORT  
 HDMI\_TX0N\_PORT >> HDMI\_TX0N\_PORT  
 HDMI\_TX1P\_PORT >> HDMI\_TX1P\_PORT  
 HDMI\_TX1N\_PORT >> HDMI\_TX1N\_PORT  
 HDMI\_TX2P\_PORT >> HDMI\_TX2P\_PORT  
 HDMI\_TX2N\_PORT >> HDMI\_TX2N\_PORT  
  
 HDMI\_CLKP\_PORT >> HDMI\_CLKP\_PORT  
 HDMI\_CLKN\_PORT >> HDMI\_CLKN\_PORT  
  
 HDMI\_TX\_HPDIN\_H >> HDMI\_TX\_HPDIN\_H  
 HDMI\_TX\_CEC >> HDMI\_TX\_CEC  
  
 HDMI\_TX\_SDA >> HDMI\_TX\_SDA  
 HDMI\_TX\_SCL >> HDMI\_TX\_SCL



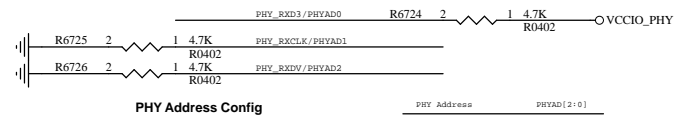
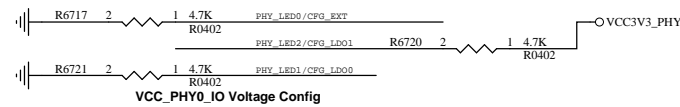
## HDMI0 TX CEC

## HDMI0 TX DDC

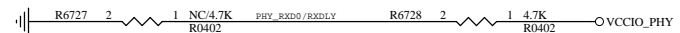
## RGMI I



## Close to PHY



### PHY Address Config



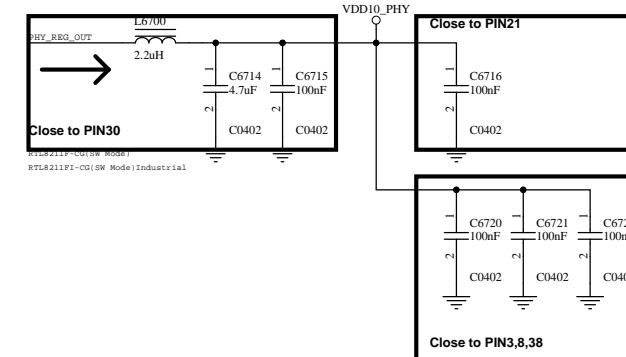
**Pull-up for additional 2ns delay to RXC for data latching**



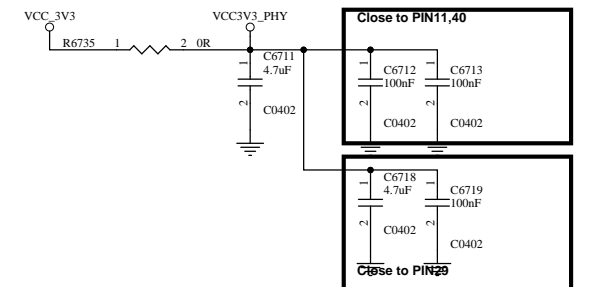
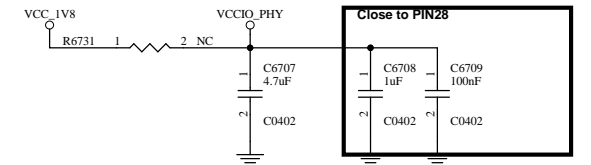
**Pull-up for additional 2ns delay to TXC for data latching**



### Pull-up to disable PLL @ ALDPS mode(Low power mode)

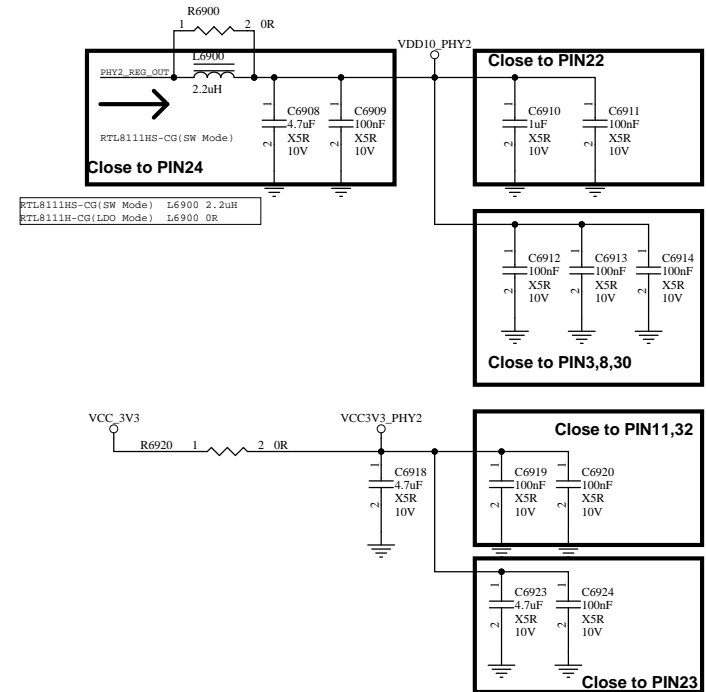
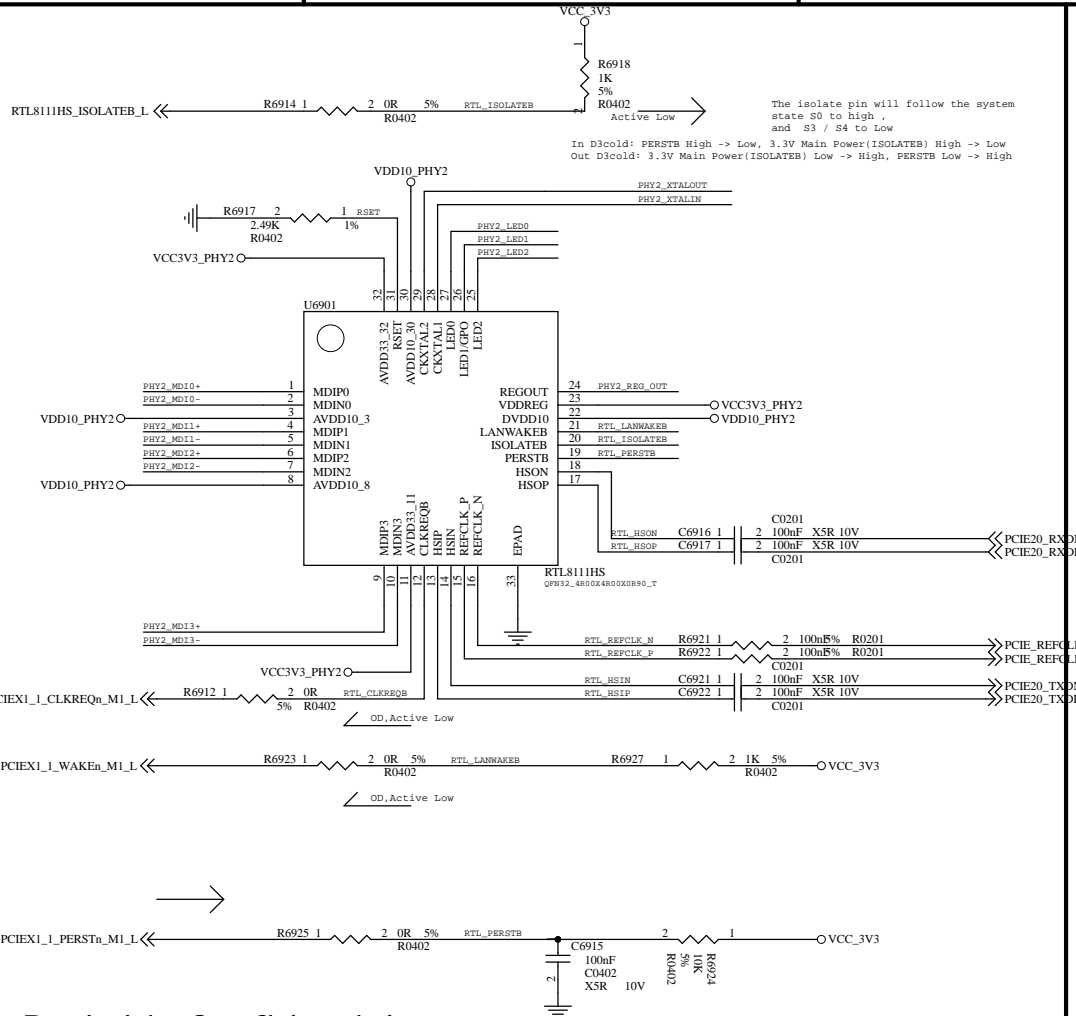
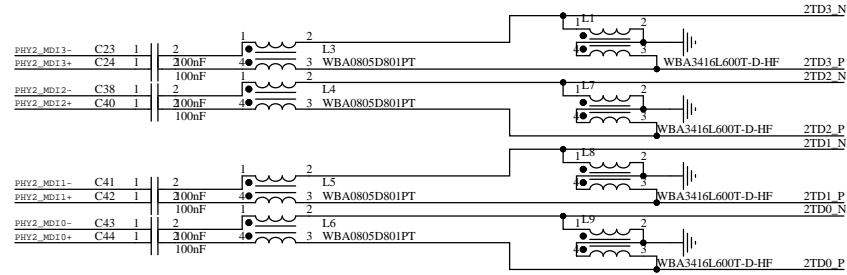
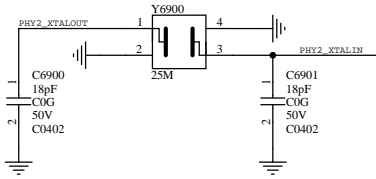


SGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V(default)	1'b0	2'b10	

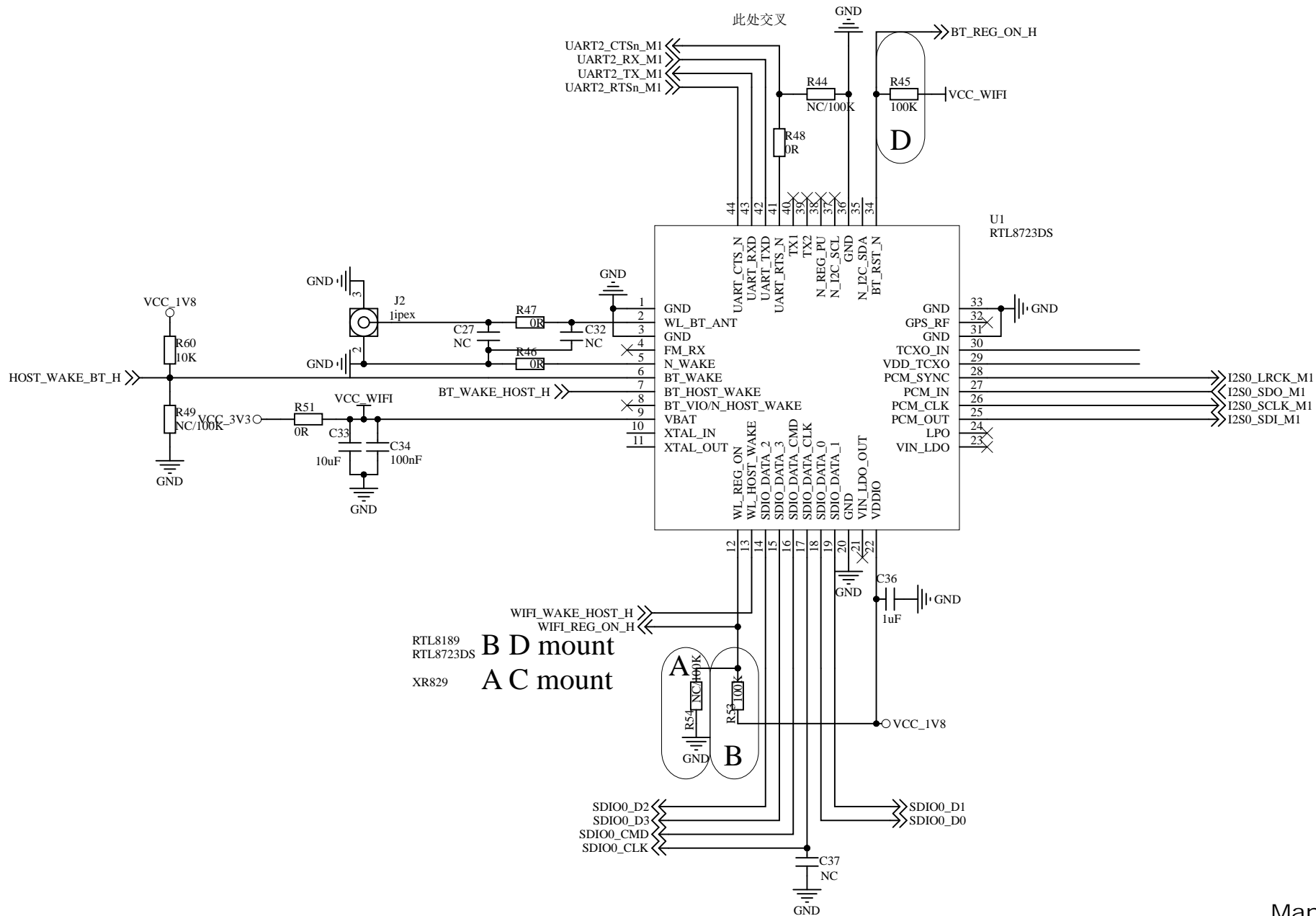


# PCIE Ethernet

PCIE20\_TXP  
PCIE20\_TXN  
PCIE20\_RXP  
PCIE20\_RXN  
PCIE20\_REFCLKP  
PCIE20\_REFCLKN







RTL8189 B D mount  
 RTL8723DS  
 XR829 A C mount