ONLINE SUMMER VLSI INTERNSHIP PROGRAMME

VLSI BASED SYNTHESIS OF IMAGE PROCESSING ALGORITHMS

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III Year - Electronics & Communication Engineering

INTRODUCTION

The Online Summer VLSI Internship Programme at Tessolve Semiconductor Pvt. Ltd., commenced on January 24, 2024, under the guidance of Mr. Nepolean M. The training period extended until June 20, 2024.

Our initial sessions focused on the basics of Digital Electronics, followed by Verilog, and subsequent assessments.

Over the course of three months, we delved into sessions on System Verilog to deepen our understanding.

As we approached the conclusion of our training, we were tasked with building our own project, leading to our exploration into VLSI-Based Synthesis of Image Processing Algorithms.

ABOUT COMPANY :

Tessolve Semiconductor Pvt. Ltd.

Location : India, USA, Germany, UK, Singapore, Malaysia, Japan, Taiwan, Philippines, Canada

Type : Private Entity

Field : Semiconductor, Chip design, and Embedded solutions.

Date of creation : Established in 2004

Founder : V. Raja Manickam

CEO : Srini Chinamilli

Headquarters : Bengaluru, Karnataka, India.

Employees : 3000 +

Turn over : $100 million revenue

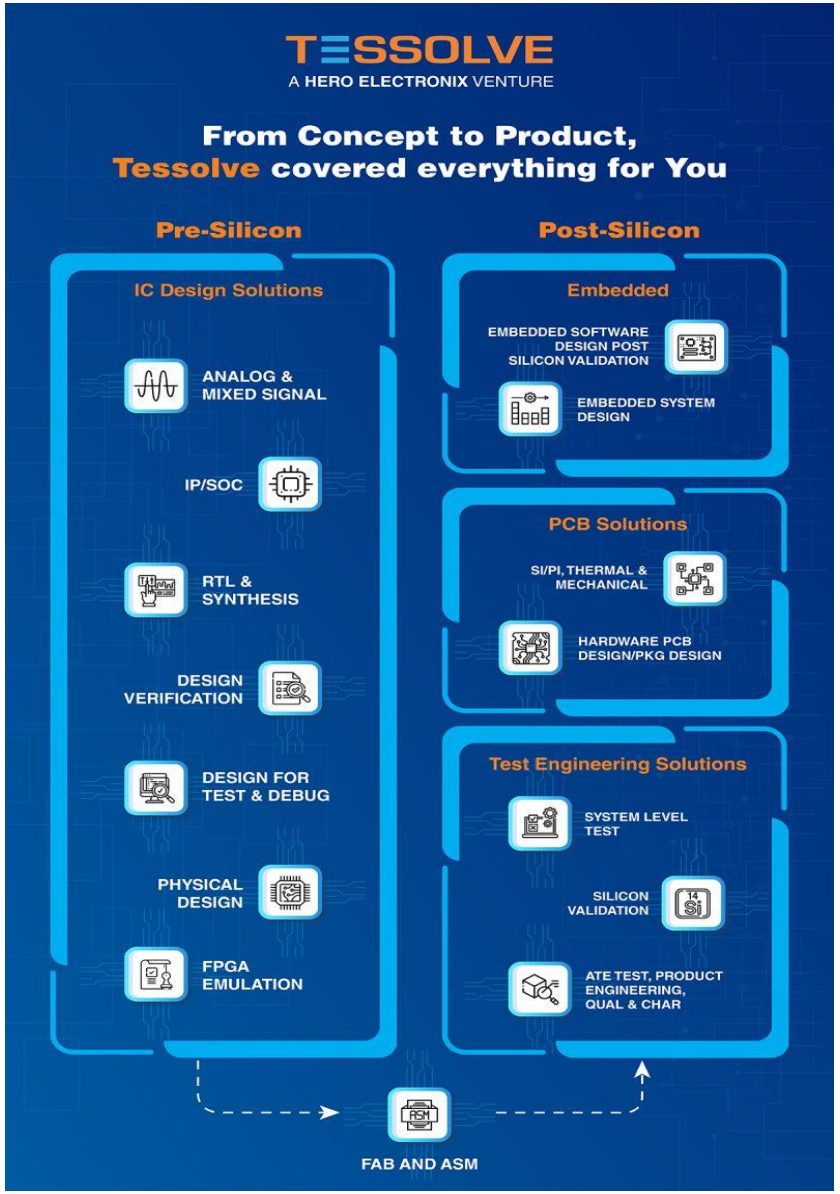
ABOUT COMPANY :

Tessolve Semiconductor Pvt. Ltd.

Description of the products: Productization of next-gen Semiconductor products, from Design to Silicon and Systems, by constant innovation and technical competence.

Strengths of the company :

Addressing disruptions in the sector of Silicon engineering – complex IC development, increasing failures, and inadequate facilities for design, development, and testingby partnering with OEMs and semiconductor companies for end-to-end innovation and productization of silicon and systems solutions.



ABOUT THE INTERNSHIP

(i) CONTEXT OF THE PROJECT

- **Overview:** Our six-month internship focused on VLSI concepts, Verilog, and SystemVerilog and complete a project by designing Verilog and System Verilog code.

- **Training Period:** First three months dedicated to theoretical learning and Last three months involved hands-on application of knowledge

- **Project Focus:** Our project is VLSI based Synthesis of Image Processing algorithm where we used to arithmetic mean filter to reduce the noise of an image

ABOUT THE INTERNSHIP

(ii) DEVELOPMENT PHASE OF OUR PROJECT

1. **Objective:**
   Implement an arithmetic mean filter for removing salt and pepper noise.

2. **Specific Tasks:**

- Selecting and preparing an image with salt and pepper noise.
- Converting the image into a hex file suitable for Verilog processing.
- Implementing the arithmetic mean filter in Verilog using Quartus Prime Lite.
- Developing SystemVerilog code for verification and testbench development.
- Synthesizing the filtered output into a hex file and visualizing results using MATLAB.

ABOUT THE INTERNSHIP

(iii) SCHEDULE OF OUR PROJECT

- Phase 1 (Weeks 1-4):Selection of the project topic, literature review, and image selection with salt and pepper noise.
- Phase 2 (Weeks 5-8): Conversion of the noisy image into a hex file and development of the arithmetic mean filter algorithm in Verilog.
- Phase 3 (Weeks 9-12): Implementation of the algorithm in SystemVerilog and development of the testbench code.
- Phase 4 (Weeks 13-14):Synthesis of the output into a hex file and visualization of the filtered image using MATLAB.
- Phase 5 (Weeks 15-16): Final testing, validation, and project documentation.

ABOUT THE INTERNSHIP

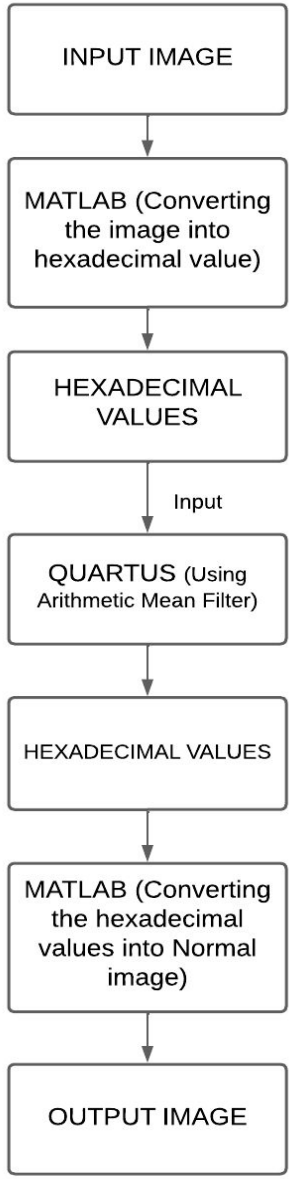
(iii) RESULT

The obtained output would be an image with reduced noise using Arithmetic Mean Filter

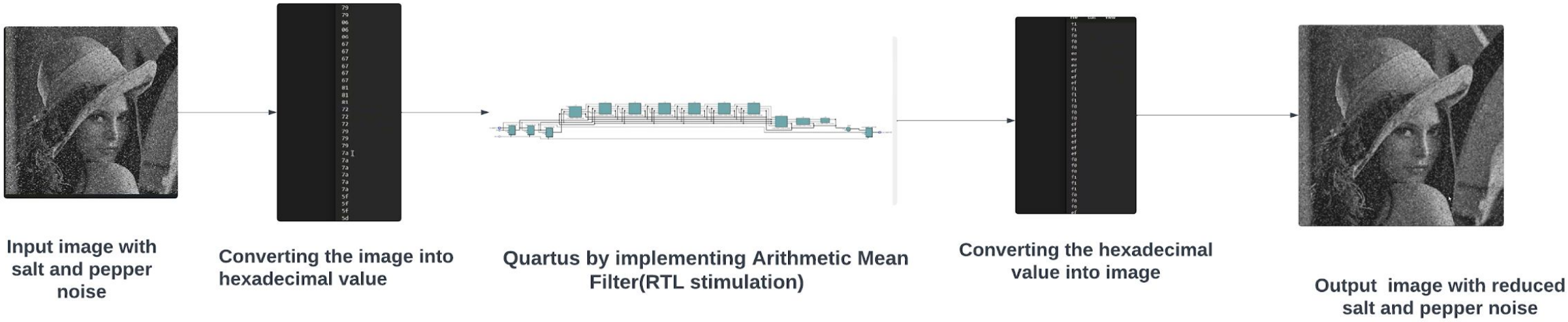
(iv) OBSERVATION OF RESULTS

1. Effective Noise Reduction:The arithmetic mean filter significantly reduced salt and pepper noise in the images.
2. Accurate Algorithm Implementation:Verilog and SystemVerilog code accurately performed the filtering, verified by testbench scenarios.
3. Seamless Integration: Quartus Prime Lite and MATLAB facilitated efficient image processing and analysis.
4. Enhanced Image Quality: The final output showed a marked improvement in image quality with minimized noise.

WORKFLOW / SYSTEM FLOW



DIAGRAMATIC REPRESENTATION OF THE PROJECT



Input image with salt and pepper noise

Converting the image into hexadecimal value

Quartus by implementing Arithmetic Mean Filter(RTL stimulation)

Converting the hexadecimal value into image

Output image with reduced salt and pepper noise

FEED-BACK OF THE EXPERIENCE

To complete the project, the team conducted a detailed analysis of image processing algorithms for restoration, thresholding, and noise filtering, gaining a solid understanding of image processing fundamentals.

The Tessolve Internship sessions provided deep insights into VLSI design. Starting from scratch, the team learned to code in both Matlab and Verilog, exploring various execution methods.

Presentations, corrections, and Q&A sessions were crucial for improvement.
By resolving errors, the team fully grasped the design and testbench code, completing the VLSI project and gaining confidence in coding with Verilog and SystemVerilog.

CONCLUSION

The internship at Tessolve Semiconductors was highly enriching, bridging theoretical knowledge and practical application. We gained expertise in Verilog and SystemVerilog, and hands-on experience with MATLAB and Quartus Prime through a VLSI-based image processing project. Implementing an arithmetic mean filter to reduce image noise highlighted the practical benefits of hardware-level processing. This experience underscored the importance of simulation and verification, preparing us for future engineering challenges and broadening our perspective on VLSI design applications in medical imaging and digital photography.