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A prototype of a new generation readout ASIC in 65nm CMOS for pixel detectors at HL-LHC

E.Monteil,[a,b,1] **L. Pacher,**[a,b] **A. Paternò,**[b,c] **F. Loddo,**[d] **N. Demaria,**[b] **L. Gaioni,**[e,f] **F. De Canio,**[e,g] **G. Traversi,**[e,f] **V. Re,**[e,f] **L. Ratti,**[e,g] **A. Rivetti,**[b] **M. Da Rocha Rolo,**[b] **G. Dellacasa,**[b] **G. Mazza,**[b] **C. Marzocca,**[d,h] **F. Licciulli,**[d] **F. Ciciriello,**[d,h] **S. Marconi,**[i,j] **P. Placidi,**[i,j] **G. Magazzù,**[k] **A. Stabile,**[l] **S. Mattiazzo**[m] **and C. Veri**[n]

[a] *Dipartimento di Fisica, Università di Torino, Via Pietro Giuria 1, Torino, Italy*
[b] *INFN — Sezione di Torino, Via Pietro Giuria 1, Torino, Italy*
[c] *Dipartimento di Elettronica e Telecomunicazioni, Politecnico di Torino, Torino, Italy*
[d] *INFN — Sezione di Bari, Via Orabona 4, Bari, Italy*
[e] *INFN — Sezione di Pavia, Via Agostino Bassi 6, Pavia, Italy*
[f] *Dipartimento di Ingegneria e scienze applicate, Università di Bergamo, Viale Marconi 5, Dalmine BG, Italy*
[g] *Dipartimento di Ingegneria Industriale e dell'Informazione, Università di Pavia, Pavia, Italy*
[h] *Dipartimento di Ingegneria Elettrica e dell'Informazione, Politecnico di Bari, Via Orabona 4, Bari, Italy*
[i] *INFN — Sezione di Perugia, Via Alessandro Pascoli, Perugia, Italy*
[j] *Dipartimento di Ingegneria, Università di Perugia, Via G. Duranti 93, Perugia, Italy*
[k] *INFN — Sezione di Pisa, Largo Bruno Pontecorvo 3, Pisa, Italy*
[l] *INFN — Sezione di Milano, Via Celoria 16, Milano, Italy*
[m] *Dipartimento di Ingegneria dell'Informazione, Università di Padova, Via Gradenigo 6B, Padova, Italy*
[n] *Dipartimento di Ingegneria dell'Innovazione, Università del Salento, Via per Monteroni, Lecce, Italy*

E-mail: ennio.monteil@cern.ch

Abstract: This paper describes a readout ASIC prototype designed by CHIPIX65 project, part of RD53, for a pixel detector at HL-LHC. A 64×64 matrix of 50×50 μm^2 pixels is realised. A digital architecture has been developed, with particle efficiency above 99.9% at 3 GHz/cm^2 pixel rate, 1 MHz trigger rate with 12.5 μs latency. Two analog front end designs, one synchronous and one asynchronous, are implemented. Charge is measured with 5-bit precision and the analog dead-time is below 1%. IP-blocks (DAC, ADC, BandGap, SER, sLVS-TX/RX) and very front ends are silicon proven, irradiated to 600-800Mrad.

Keywords: Analogue electronic circuits; Digital electronic circuits; Front-end electronics for detector readout; Radiation-hard electronics

[1] Corresponding author.

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1 Introduction

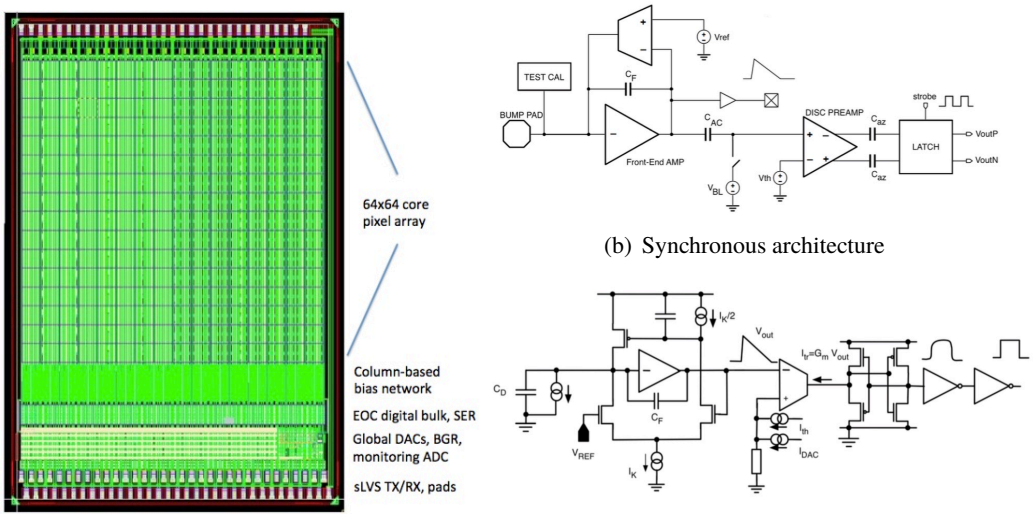
The High Luminosity Large Hadron Collider (HL-LHC) will start its operation in 2026. The machine will establish new benchmarks for the experiments, such as a pile-up per event between 140 and 200 and for the innermost layer an expected level of radiation of 1 Grad in 10 years and an event rate for the innermost layer around 3 GHz/cm^2.

The readout chip currently used in LHC experiments can not tolerate these extreme requirements, therefore a new design is required. For this purpose the RD53 collaboration at CERN has been established. INFN is part of this collaboration through the CHIPIX65 project. A 65nm CMOS technology has been chosen to for the production of the chip, since the detector granularity will be increased (the pixel area is 2500 μm^2) and the total amount of data will be significantly higher than in current LHC runs, requiring the introduction of more digital logic, especially buffer cells, per pixel.

In this paper the design of a small and complex pixel array, called CHIPIX65 demonstrator [1], is described. The layout of the chip submitted to the foundry is shown in figure 1a. It has a size of 3.5×5.1mm^2 and consists of a 64×64 pixel matrix which contains two flavors of analog front-ends and a digital architecture organized in 4×4 pixel regions. The periphery contains all the blocks required for the bias, the readout and the configuration of the chip.

2 Analog front-ends

The pixel matrix contains a synchronous and an asynchronous front-end, each of them occupying half of the matrix. For both architectures two small prototypes have been submitted and tested, also after irradiation. Both architectures feature a single stage preamplifier to minimize the power dissipation and a Krummenacher feedback to provide both leakage current compensation and constant current feedback capacitor discharge, along with a calibration circuit to inject an input



(a) CHIPIX demonstrator.

(b) Synchronous architecture

(c) Asynchronous architecture

Figure 1. CHIPIX demonstrator overview and analog front-end chains.

charge. The front-ends satisfy the requirements of being compact, low power, low noise (< 100 e^-) in order to achieve high efficiency with the foreseen silicon detectors.

The synchronous architecture [2, 3], presented in figure 1b, features a telescopic cascode preamplifier AC coupled to a synchronous discriminator composed of a Differential Amplifier (DA) and a positive feedback latch. The offset compensation of the DA is performed using capacitors (auto-zeroing) without need of local Digital-to-Analogue Converters (DACs). The latch can be turned into a local oscillator up to 800 MHz using an asynchronous logic feedback loop, in order to accomplish the ToT counting in a very short time avoiding to distribute a fast clock in the chip. The average current consumption is around 5 μA. Measurements show very promising results, in particular: the preamplifier gain shows a very good uniformity over the pixel matrix with a 2.2% RMS in the gain distribution, the ENC is equal to 80 e^- at C_{input} 50 fF, the offset compensation mechanism and the local oscillation both work consistently with simulation results. Irradiation measurements show that the front-end is fully working at 600 Mrad, with negligible degradation of the analog parameters [4].

The asynchronous architecture [5], shown in figure 1c, features a folded cascode amplifier, followed by a fast comparator composed of a transconductor stage and a transimpedance amplifier. A 4-bit DAC is included for local threshold trimming. The average current consumption is 4 μA. Measurements show that the noise response is fully compliant with the specifications, and that leakage currents up to 15 nA do not affect the preamplifier performance. Total Ionizing Dose (TID) irradiation has been performed up to 800 Mrad, showing no significant degradation in the preamplifier signal shape and a 20% increase in noise with a C_{det} = 50 fF at 800 Mrad [5].

3 Digital architecture and chip configuration

The CHIPIX65 demonstrator features a novel digital architecture. It is based on the concept of pixel region with local trigger matching as in FEI4 [6]: (2x2) pixels with distributed latency buffers.

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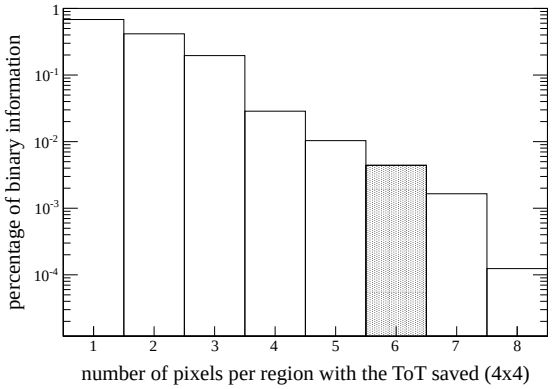

Figure 2. Inefficiency vs. saved ToTs per event.

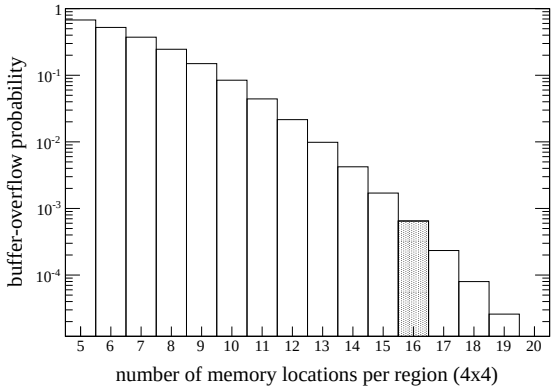

Figure 3. Inefficiency vs. buffer depth.

Nevertheless, it extends the grouping to (4x4) pixels and centralised latency buffer, obtaining an optimised sharing of the digital circuitry. The Pixel Regions contain 16 pixel analog front-ends, themselves grouped in (2x2) pixel analog islands in the layout, and a shared digital architecture which stores the pixels' data, handles the configuration, performs trigger matching, and communicates with the readout block at the chip periphery.

The advantage on choosing a 4×4 approach lies in the possibility to achieve an efficient sharing of buffer resources, without compromising the inefficiency. Targeting an inefficiency lower than 0.1%, such a Pixel Region would, in fact, only need 16 buffer locations, as shown in figure 3. Together with a Time-over-Threshold (ToT) compression algorithm, the advantage of this approach is clear: an efficient way to reduce the memory size inside the digital architecture, and, with it, the overall power consumption and area. ToT compression is performed by saving only a fixed number of ToTs per event but preserving the binary information for all the 16 pixels of the region: the graph in figure 2 shows the percentage of binary hits versus the number of 5-bit ToT saved in the central buffer. In order to quantify hit losses, detailed simulations have been performed using the SystemVerilog-UVM simulation framework developed within RD53 [7], which has also been used for chip verification. Simulations have been run including Montecarlo data from physics input hits, provided from detailed sensor simulations. In order to reach the target (ToT information for

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more than 99.5% of hits), the design choice was to arrange the priority queue so that only the six first ToTs per event are saved in the shared buffer. This allows to an overall saving of about 60% in the number of latches in the shared memory (6 instead of 16). Working on event-based data implies another requirement for the design: the need for pixels synchronization. Every pixel, in fact, processes its ToT independently via dedicated counters in the pixels' digital interfaces, but the writing operation, which accounts for the ToT compression too, has to happen when all the pixel hits belonging to the same event are ready. To overcome this hurdle, a deadtime counter has been implemented to every interface. When the fixed deadtime elapses for a pixel (the deadtime can be set to either 5 or 15 clock cycles), the pixel interface raises a ready flag. The shared logic checks at each clock cycle whether any pixel has raised this flag, and, if so, follows the priority queue and drives the memory latches.

Other important features are the trigger matching algorithm, performed via a set of comparators, and a debugging mode which can be used in both triggered and triggerless operations.

4 Bias network and monitoring

The bias to the analog FEs is provided in the chip periphery and is monitored by an internal ADC (see figure 4). Sixteen 10-bit current DACs, nine for the synchronous FE, six for the asynchronous FE and one for the calibration circuit, are used to provide bias currents and voltages to the front-ends. Current mirrors have been designed in order to provide the different currents with the requested resolution and to guarantee linearity in the full operating range. These mirrors are connected to the column bias cells, designed to drive 64 pixels.

The DAC [8] has been implemented using a segmented architecture. It is then split into 2 sub-DACs: a 8 bit thermometric DAC and 2 bit binary DAC. This configuration has been preferred since it is the best compromise between performance and area. Irradiation tests with both X-rays and protons up to 1 Grad show that this block still works properly with an increase of Differential Non-Linearity (DNL) from 0.4 LSB to 1 LSB, while the Integral Non-Linearity (INL) rises from 0.9 LSB to 1.5 LSB.

During operation the DAC needs a reference current, I_{ref}, which is provided by a bandgap reference circuit (BGR) [9]. It provides a DC voltage independent of Process, supply Voltage and Temperature (PVT) variations. In high-energy physics (HEP) applications it has to fulfill an additional requirement given by the harsh radiation environment. For this reason this bandgap has been designed using MOSFET biased in weak inversion region instead of Bipolar Transistors. It has been characterized with X-rays up to 580 Mrad (SiO_2). The circuit implements a 5-bit trimming resistor for the compensation of the mismatch and process variations.

In addition, a 12-bit ADC has been integrated on-chip for monitoring DC voltage levels and slow varying signals. A dual-slope integrating architecture has been chosen, since high accuracy is required at low conversion rate, i.e. about 5 kSample/s. A linear transconductor converts the input voltage, in the dynamic range from 0 to 900 mV, into a current, which is integrated onto a 70pF Met al.-Oxide-Metal (MOM) capacitor for 2^{12} clock cycles. The output code is obtained by counting the clock cycles needed to discharge the integration capacitor at a constant current. An automated calibration procedure has been implemented to finely adjust the gain and the discharge current.

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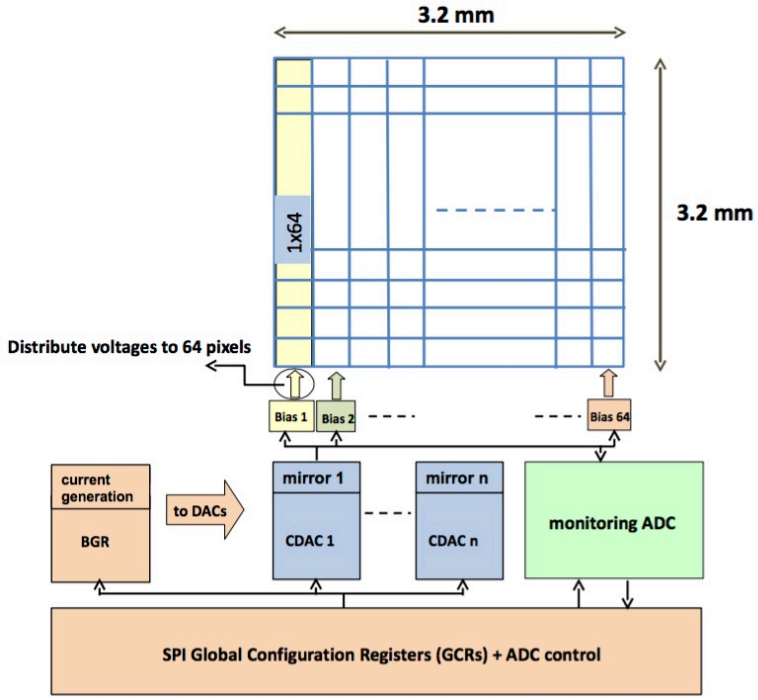

Figure 4. Bias network scheme (n = 16).

5 End of column, readout and configuration interface

For the purpose of this demonstrator, it was decided to employ a simple readout architecture. Communication with each macro-column is performed via ad-hoc modules called Macro Column Drainers. As the name suggests, these modules implement the receiver end of the column-drain protocol, in addition to buffering both the triggers to be sent to the Pixel Regions and the output data sent by them. The data FIFOs are polled and read by a centralized data buffer, namely Dispatcher, designed to withstand the expected data rates. Another Finite State Machine, working at the serializer frequency, reads the Dispatcher FIFO, encodes the data using 8b10b encoding, and feeds the 20-bit packets to the serializer. Serialized data are then sent to the Scalable Low Voltage Signaling Transceiver (SLVS-Tx) [10].

6 Conclusions

The CHIPIX65 demonstrator, a $3.5 \times 5.1 \text{mm}^2$ chip composed of a matrix of 64×64 pixels, has been designed and submitted for fabrication in July 2016. Beforehand, the analog front-ends and the building blocks have been characterized through small prototypes, showing promising results also after irradiation levels above 500 Mrad. In addition, the chip contains a novel digital architecture featuring a digital inefficiency $< 0.1\%$ at the HL-LHC rate (3 GHz/cm^2) and providing 5-bit ToT information for 99.6% of hits. The chip has been received at the end of September 2016. Early results show that it works correctly and the bare devices show 85 e$^-$ ENC and 500 e$^-$ minimum threshold. Bump bonding to silicon detectors is foreseen and irradiation tests of the bare chip will be performed in early 2017.

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