Pixel front-end with synchronous discriminator and fast charge measurement for the upgrades of HL-LHC experiments

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Pixel front-end with synchronous discriminator and fast charge measurement for the upgrades of HL-LHC experiments

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Abstract: The upgrade of the silicon pixel sensors for the HL-LHC experiments requires the development of new readout integrated circuits due to unprecedented radiation levels, very high hit rates and increased pixel granularity. The design of a very compact, low power, low threshold analog very front-end in CMOS 65 nm technology is described. It contains a synchronous comparator which uses an offset compensation technique based on storing the offset in output. The latch can be turned into a local oscillator using an asynchronous logic feedback loop to implement a fast time-over-threshold counting. This design has been submitted and the measurement results are presented.

Keywords: VLSI circuits; Radiation-hard electronics; Front-end electronics for detector readout

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1 Introduction

The High Luminosity Large Hadron Collider (HL-LHC) [1] is an upgrade of the present LHC machine which is planned for the years 2024-2025, targeting an increase of the average luminosity to $5 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$ in order to achieve a $3000\,\mathrm{fb^{-1}}$ integrated luminosity in ten years. The physics program of HL-LHC includes a precise measurement of the Higgs coupling, study of rare decays and extending the search for new physics.

Unprecedented levels of radiation (a Total Ionizing Dose (TID) of 1 Grad in 10 years) and very high particle rates (around $2\,\mathrm{GHz/cm^2}$) will be reached in the innermost tracking elements of the experiments. The current silicon pixel detectors were not designed to cope with these requirements, leading to the necessity of using new technologies for both the sensors and electronics. In this context the RD53 Collaboration [2] has been established at CERN to explore new technologies and architectures for future front-end chips. INFN contributes to this effort through the CHIPIX65 project [3]. A CMOS 65 nm technology has been chosen for the new chip, since the pixel detector granularity will be increased (the pixel size is expected to be $50 \times 50\,\mu\mathrm{m^2}$ or $25 \times 100\,\mu\mathrm{m^2}$) and the total amount of data will increase (the L1 trigger rate will be 750 kHz). Therefore, the 65 nm technology allows to accommodate the needed digital intelligence inside the pixel, while keeping under control the overall power consumption.

In this paper the design of a pixel analog front-end is reported. In section 2 the architecture is presented in detail. The first two submitted prototypes are detailed in section 3, along with a description of the test board. In section 4 the performance results obtained from the measurements on the prototypes are presented.

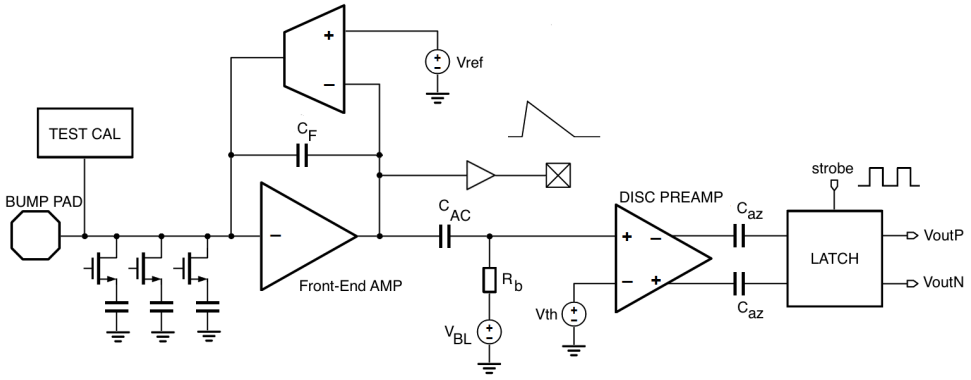

Figure 1. Overview of the analog front-end.

2 Overview of the design

The pixel analog chain is shown in figure 1. A single stage Charge Sensitive Amplifier (CSA) has been used, with a Krummenacher feedback network [4] providing both the feedback capacitor constant current discharge and the sensor leakage current compensation. The first stage is AC coupled to a synchronous discriminator, which is composed of a Differential Amplifier (DA) and a latch. The DA uses the output offset storage technique, which allows to compensate the offset using capacitors connected to the two preamplifier outputs during dedicated and periodic time windows. The overall current consumption of this architecture is around 4.5 μA. The supply voltage is 1.2 V. In addition, three different capacitors (with values of 21.5 fF, 43 fF and 86 fF, to which some parasitic capacitance has to be added) can be connected via configuration switches at the input of the first stage in order to emulate a sensor load. A calibration circuit is included to provide input pulses: it requires a voltage DC level from outside and a configuration bit to enable the injection of the signal. The size of the analog front-end is $26 \times 40\ \mu m^2$, less than half of the area of the pixel. It increases to $26 \times 50\ \mu m^2$ considering also an analog buffer and the sensor emulating capacitors, which are inserted only for testing purposes and will not be present in the final version of the chip.

2.1 Preamplifier

The schematic of the CSA is presented in figure 2. The purpose of this architecture is to achieve a high voltage gain and a low-noise performance at the same time. For this reason, a telescopic cascode (M1-M4) with PMOS current splitting (M5-M6) has been chosen. In this way an open-loop gain around 1000 is obtained. The input transistor, M1, works in the weak inversion region. Sizing of this device has been studied to minimize the noise contribution, based on simulations and theoretical MOS descriptions like the EKV model [5]. A low noise design is a key point, since the minimum detectable signal is required to be 1 ke^- or lower. This part is followed by a NMOS source follower (M7-M8) to ensure impedance matching and proper driving strength. Two switches (M9-M10) have been added to be able to operate with different feedback capacitance configurations (2.5, 4 and 6.5 fF) during the testing phase of the chip.

The input signal is provided by a calibration circuit. A DC voltage level, V_{cal}, drives a C_{cal} capacitor connected in series to the input node. A configuration bit, named *TEST_EN*, is required to

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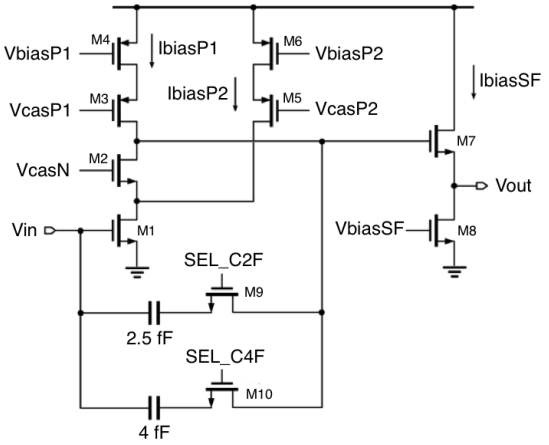

Figure 2. Schematic of the CSA.

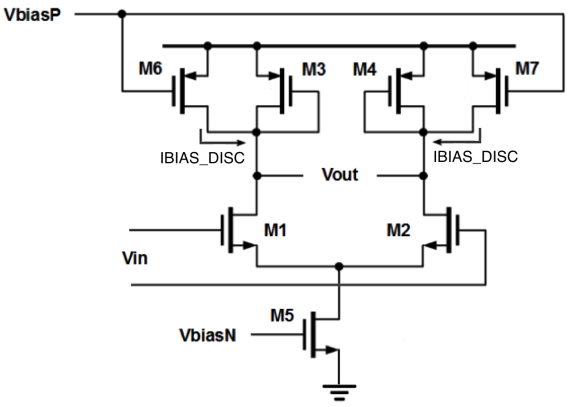

Figure 3. Differential amplifier scheme.

enable the injection of the test charge. The absolute value of the injected charge is $Q_{\mathrm{cal}} = C_{\mathrm{cal}}\, V_{\mathrm{cal}}$, with $C_{\mathrm{cal}} = 8$ fF.

The Krummenacher scheme has been adopted to implement the DC feedback network. It allows to do both the sensor leakage current compensation and the constant current discharge of the feedback capacitor using the same current source. For the former aspect, the maximum expected leakage is around 20 nA according to the RD53 specifications. The latter determines instead how fast the signal returns to the baseline after having reached the peak.

2.2 Discriminator and offset compensation

The first part of the discrimination stage consists of a low-gain fully-differential amplifier, whose inputs are the signal coming from the preamplifier and a discrimination threshold voltage. The schematic is shown in figure 3. The choice of a fully-differential architecture is driven by the necessity of getting rid of common mode noise and voltage supply variations. In principle, if the two inputs of a DA are shorted, the difference of the outputs should be zero. However, in a real implementation, this is not true due to mismatch effects, which produce an offset which therefore has to be compensated. For this purpose the output offset storage scheme [7], presented in figure 4, has been adopted. It requires a control sequence which is described in figure 6. All these logic signals are provided by a circuit in the periphery of the chip. At the beginning the signal ϕ_2 goes low, disconnecting the first stage and the threshold voltage from the discriminator. At the same time $\phi_{1\mathrm{A}}$ and $\phi_{1\mathrm{B}}$ go high, connecting both the inputs and the outputs of the second stage to a reference baseline voltage named *V_BL*. In this way the offset is stored into the two capacitors. At the end of the compensation window $\phi_{1\mathrm{B}}$ goes down before $\phi_{1\mathrm{A}}$ in order to take into account also some residual offset due to the opening of the switches. Then ϕ_2, which in practice is $\phi_{1\mathrm{A}}$ inverted, goes high and the front-end is ready again to receive and discriminate input signals.

The outputs of the DA are fed into the latch, whose schematic is shown in figure 5. The discrimination takes place for each rising edge of the strobe signal connected to the 40 MHz clock. In this way it generates a binary HIT output, whose length is a multiple of the strobe period. It can be also turned into a local oscillator by means of an asynchronous logic feedback loop in

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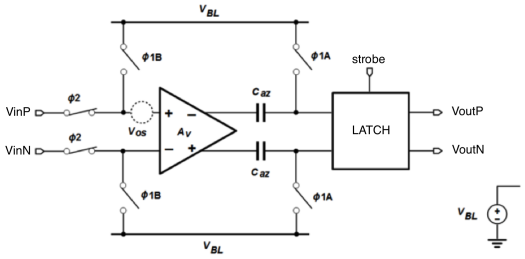

Figure 4. Second stage offset compensation scheme.

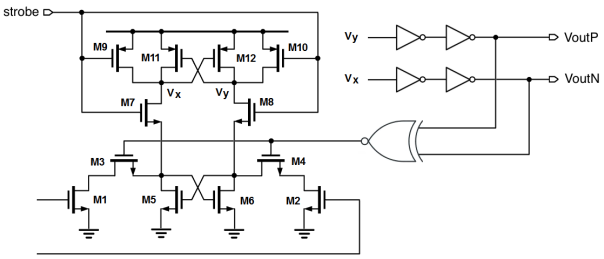

Figure 5. Schematic of the latch.

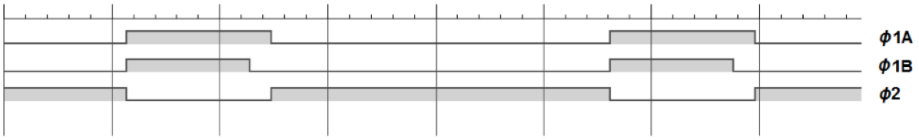

Figure 6. Offset compensation control sequence.

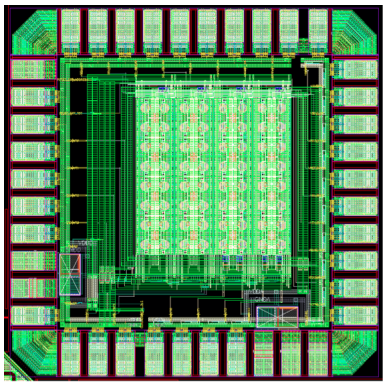

Figure 7. *CHIPIX_VFE_1/TO* layout.

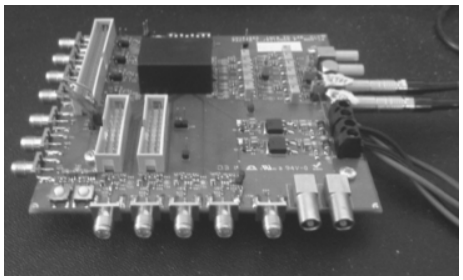

Figure 8. *CHIPIX_VFE_1/TO* test board.

order to internally generate a clock that can be used for high-speed ToT digitization. This is a technique frequently used in modern high-speed Successive Approximation Registers (SAR) A/D converters [6]. The oscillation frequency can be modulated in the range 100–900 MHz by changing the current flowing in a voltage-controlled delay line contained into the loop.

3 Chip submissions

A first small test prototype of the front-end has been submitted inside a common CHIPIX65 submission, under the name *CHIPIX_VFE_1/TO*. It has a 1×1 mm^2 size and contains a matrix of 8×8 pixels organized in a double column scheme. The layout of the chip is presented in figure 7. Some bias cells are also included in order to provide the current inside the pixels, along with analog and digital buffers for each double column which are used to bring out signals.

Subsequently a test board has been designed to characterize the prototype. It provides mechanical sustain, wire-bonding landing pads, power and necessary input/output access points. In addition it contains some control switches, which allow to modulate the value of the sensor-emulating ca-

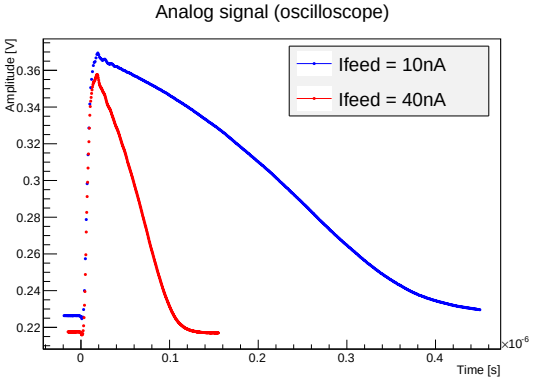

Figure 9. Analog signal shapes.

pacitors, to set the value of the feedback capacitor and to enable the oscillating configuration of the latch. The board provides current and voltage biases to the pixels, with values tunable via trimmers. The testing phase has been started after the chip has been wire bonded to the setup. A picture of the board with the chip lying under a protective box is shown in figure 8.

A second prototype, named *CHIPIX_VFE_2/TO*, has been submitted. It contains the same front-end architecture presented in section 2, with optimizations in some key points, as it will be explained in the following paragraphs.

4 Test results

The test setup contains, in addition to the board, some other instruments:

- A pattern generator which provides the needed logic signals for the calibration circuit and offset compensation, along with the 40 MHz clock
- Two generators to provide the threshold and baseline voltages in addition to analog and digital power
- A 2-GHz bandwidth 4-channels oscilloscope
- 4 oscilloscope probes, one of them differential to look at high frequency signals

In all the measurements shown in this paper, unless differently indicated, the current and voltage values are: *IBIAS_1* = 0.5 μA, *IBIAS_2* = 1.5 μA, *IBIAS_SF* = 0.5 μA, *IBIAS_FEED* = 40 nA, *IBIAS_DISC* = 0.38 μA.

4.1 Analog signal and voltage gain

Figure 9 shows the CSA output after a two stage analog buffer. A calibration signal of 10 ke$^-$ has been sent, with an input capacitance of 100 fF. The time needed for the signal to return to the baseline is dependent on the value of the feedback current. A 40 nA current determines a "fast" recovery, which allows to perform a Time-over-Threshold measurement in around 100 ns for a 10 ke$^-$ input charge. A 10 nA current leads, instead, to a "slow" configuration in which the ToT time

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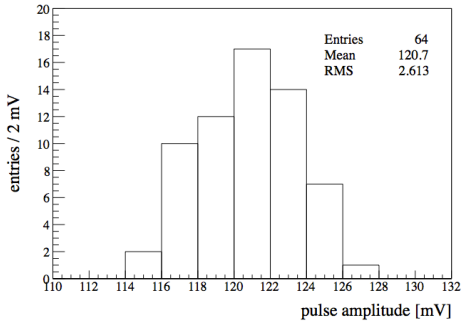

Figure 10. Gain distribution for the 64 pixels.

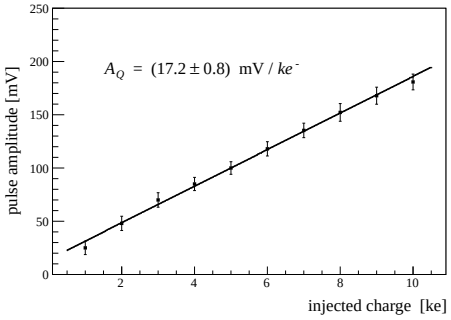

Figure 11. Gain linearity up to $10 ke^-$.

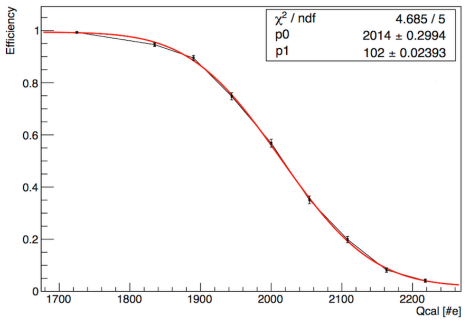

Figure 12. S-curve for a single pixel.

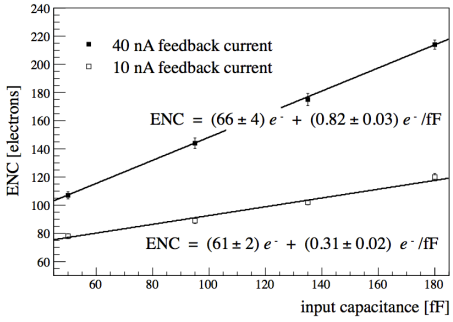

Figure 13. Noise vs input capacitance.

is around 400 ns for the same input charge. This choice has therefore an influence on the dead time of the readout, but also on the noise performance, as it will be explained in section 4.2. The gain variation among 64 pixels has been measured sending a 6 ke^- calibration signal and the amplitude of the signal has been computed on the oscilloscope. The histogram relative to this measurement is reported in figure 10. It shows that the spread in gain between channels is small, since the RMS of the distribution is equal to the 2.2% of the mean value.

In addition, a plot of the amplitude as a function of the input signal has been performed for a single pixel and is presented in figure 11. It can be seen that the CSA has a linear behavior up to an input charge of 10 ke^-.

4.2 Noise performance

Noise has been measured using the S-curves method. One of them is shown as an example in figure 12. Firstly a value of feedback current and input capacitance has been fixed. Then, for an input charge of 2 ke^-, an efficiency scan has been performed by changing the threshold voltage for 16 different pixels. This procedure has been repeated for two different feedback currents and, for each of them, four values of input capacitances. Figure 13 shows that the Equivalent Noise Charge (ENC) increases linearly with the input capacitance for both the values of feedback current as expected. However, the fast configuration leads to a significant increase of the noise compared to the slower one. However, for an input capacitance equal to 100 fF, which is expected to be quite an upper limit for the sensor that will be used for the HL-LHC upgrade, both configurations are compatible with a 1000 e^- or even smaller threshold.

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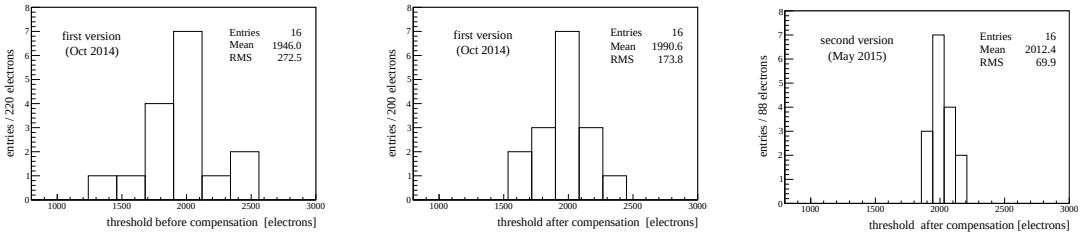

(a) Uncompensated. (b) Compensated - First prototype. (c) Compensated - Second prototype.

Figure 14. Threshold distributions.

4.3 Threshold dispersion

The same S-curves have been used to determine the threshold dispersion, which has been measured for 16 pixels. Figure 14 shows a comparison between a situation in which the offset compensation is not performed with a case in which the scheme presented in section 2.2 is applied. In the first prototype the threshold dispersion decreases by applying the offset compensation, but not as much as expected.

Further simulations have shown that it has been understood that there were two main issues that had substantially worsened the offset compensation performance:

- A fluctuation of the gain in the differential amplifier
- An initial underestimation of the dynamic offset contribution in the latch

This is the main reason that lead to the need of the second submission of the architecture, the *CHIPIX_VFE_2/TO* chip. The structure of the amplifier has been partially changed to reduce the gain spread. The two mirror transistor (M6-M7) shown in figure 3 have been eliminated and the loss in gain has been in part recovered by cascoding the input transistors (M1-M2). In addition, the size of some transistors of the latch has been increased since the dynamic offset was due to the mismatch effects. This second version of the front-end has been wire-bonded to the same type of board used for the testing of the first one.

Measurements on the second prototype, shown in figure 14(c), confirm the reduction of the threshold dispersion from 174 e^- to 70 e^-.

4.4 Time-over-Threshold

Figure 15 shows a oscilloscope screenshot taken with the latch in oscillator mode. The frequency in this case is limited to 100 MHz by the set-up, but simulations show that the oscillator can work properly up to 500 MHz. The figure shows that the oscillation starts when the analog signal goes beyond the threshold and stops when it returns below.

Figure 16 shows instead the ToT is linear on a wide range of input charges.

5 Summary

Two prototypes of a pixel analog front-end in CMOS 65 nm technology have been submitted and tested. It has a size of $26 \times 40\ \mu m^2$ and the current consumption is 4.5 μA per pixel. The spread

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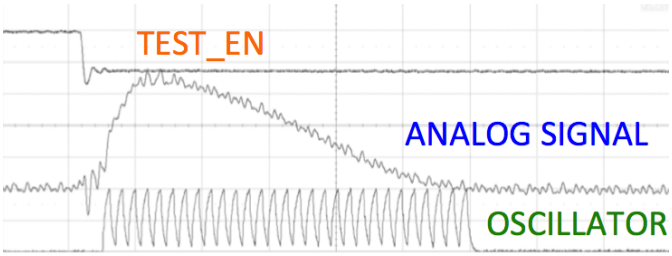

Figure 15. 100 MHz oscillating ToT output.

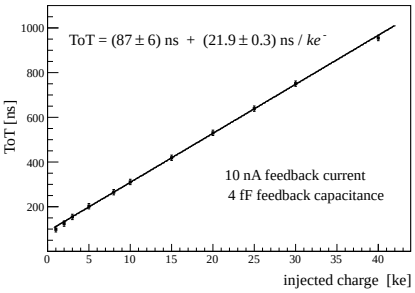

Figure 16. ToT linearity.

in gain between different channels is equal to the 2.2% of the mean value. The ENC is 78 e^- with an input capacitance of 50 fF and a feedback current of 10 nA and rises to 107 e^- with a feedback current equal to 40 nA. It allows to choose a threshold lower than 1000 e^- with a very low fake hit rate. The idea of the self-oscillating comparator for fast ToT measurements works properly. In the offset compensation, from the testing of the first prototype some issues were detected. These were reproduced in simulation, and subsequent circuit modifications lead to a reduction of the threshold dispersion in the second chip from 174 e^- to 70 e^-.

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