A Low-Power Low-Noise Synchronous Pixel Front-End Chain in 65 nm CMOS Technology with Local Fast ToT Encoding and Autozeroing for Extreme Rate and Radiation at HL-LHC

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***Abstract*—A low-power and low-noise synchronous front-end chain in a commercial 65 nm CMOS technology suitable for the future pixel upgrades at the CERN Large Hadron Collider (LHC) is presented. A shaper-less Charge-Sensitive Amplifier (CSA) with constant current feedback provides triangular pulse shaping for linear Time-over-Threshold (ToT) charge measurement. The sensor leakage current is compensated by the same feedback network. A track-and-latch voltage comparator is adopted for the hit discrimination. The hit generation is synchronized with a 40 MHz clock, minimizing time-walk issues in the time-stamp assignment. Fast ToT charge encoding up to 8-bit resolution can be retrieved at the pixel level exploiting a high-frequency self-generated clock signal. This is obtained by turning the latch into a voltage-controlled oscillator (VCO) using asynchronous logic. Pixel-to-pixel threshold variations are compensated by means of an autozeroed scheme, thus avoiding the need of a on-pixel D/A converter. An array of 8 $\times$ 8 cells with 50 μm $\times$ 50 μm pixel size has been prototyped. Design specifications, implementation and test results are discussed.**

I. Introduction

The foreseen High-Luminosity (HL) LHC upgrade [1] will impose the installation of new silicon pixel detectors in the inner tracking systems of general-purpose experiments.

With increased performance the machine will deliver proton collisions with an instantaneous luminosity up to 10^{35} cm^{-2}s^{-1}, one order of magnitude higher with respect to the current design value, targeting to reach an integrated luminosity of 3000 fb^{-1} in 10 years. With such a luminosity and a centre-of-mass energy of 14 TeV the nominal collision rate of 40 MHz will lead to unprecedented track densities, introducing extreme rates and radiation levels. More layers equipped with sensors featuring high granularity, speed and radiation hardness will be required close to the interaction regions. Thus hybrid silicon pixel detectors will continue to play a fundamental role.

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The innermost pixelated layer will have to cope with an expected Total Ionizing Dose (TID) of 10 MGy in 10 years, corresponding to 10^{16} (1 MeV) n_{eq}/cm^2. Smaller pixels of the order of 50 μm $\times$ 50 μm will be required to maintain high spatial resolution and two-tracks separation. The particle flux will increase to 500 MHz/cm^2, leading to hit rates of the order of 2 GHz/cm^2 and an estimated average rate per pixel of 50 kHz. The foreseen usage of thinner sensors of 100-150 μm thickness to increase the radiation tolerance will determine reduced signals, needing low-threshold (as low as 1 ke^- minimum detectable charge) and low-noise performance for the analogue front-end (below 150 e^- RMS at nominal 100 fF input capacitance including strays). Moreover a time response below 25 ns is required in order to cope with the nominal LHC bunch crossing rate, while keeping bias currents to acceptable values and targeting to a total maximum power dissipation of 10 μW per pixel. More on-chip intelligence and much higher readout bandwidth will be required to accommodate unprecedented data rates.

Research and development activities devoted to the design of new pixel Application Specific Integrated Circuits (ASIC) suitable for HL-LHC upgrades have started. A commercial 65 nm CMOS process has been identified by the pixel ASIC community as a promising fabrication technology for the implementation of new generation pixel readout chips. Such a 65 nm was already demonstrated to be radiation tolerant up to 3 MGy [2]. Technology qualification and radiation hardness studies using 65 nm CMOS are now part of the international RD53 collaboration research program officially supported by CERN [3] and of the Italian INFN CHIPIX65 project [4].

Preliminary pixel front-end test structures, small pixel arrays and other analogue, digital and mixed-signal building blocks have been submitted and tested by the CHIPIX65 collaboration. A small pixel array of 8 $\times$ 8 cells with 50 μm $\times$ 50 μm pixel size has been prototyped as part of the first CHIPIX65 submission. In order to gain from increased speed offered by a 65 nm CMOS technology node and meet the low-threshold and low-power requirements, a synchronous front-end architecture has been implemented.

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Section II of the paper summarizes the front-end design, while test results are presented in Section III and conclusions are drawn in Section IV.

II. Front-end architecture

A schematic block diagram of the front-end chain is reported in Fig. 1. The input stage is a charge-sensitive amplifier implemented as a single-ended, 60 dB open-loop gain inverting amplifier with two selectable feedback capacitors. In order to save power and area a shaper-less solution is chosen. Hence the CSA output directly drives the front-end discriminator.

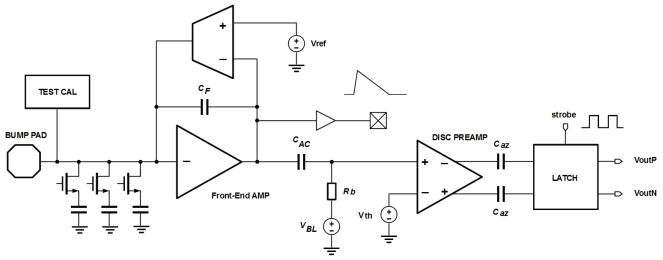

Fig. 1: Schematic block diagram of the front-end channel. Selectable shunt capacitors at the input node allows to mimic different values of sensor capacitance.

Linear charge measurements up to 40 ke^- are performed using the ToT technique, therefore triangular pulse shaping is adopted. A time-invariant feedback network based on an auxiliary transconductance amplifier discharges the feedback capacitance with a selectable constant current in the 5-50 nA range after a charge signal has been detected [5]. The same feedback circuit compensates also the sensor leakage currents up to 50 nA. A calibration circuit is used to inject a test charge at the CSA input node. Selectable test capacitors have been added to mimic different values of pixel sensor capacitance.

The front-end amplifier is AC coupled to a discrete-time hit discriminator. In this way, any offset caused by the feedback transconductor can not propagate to the discriminator. A track-and-latch voltage comparator is employed. It is implemented as a low-gain high-bandwidth differential preamplifier coupled to a regenerative latch stage. Thanks to positive feedback, precise and fast voltage comparison can be obtained with low-power dissipation, allowing to discriminate very low charge-induced signals above the nominal threshold. The generation of a CMOS digital hit pulse is synchronized with a 40 MHz master clock, sampling the CSA analogue output. This provides a reliable solution that greatly relaxes time-walk issues in the time-stamp assignment.

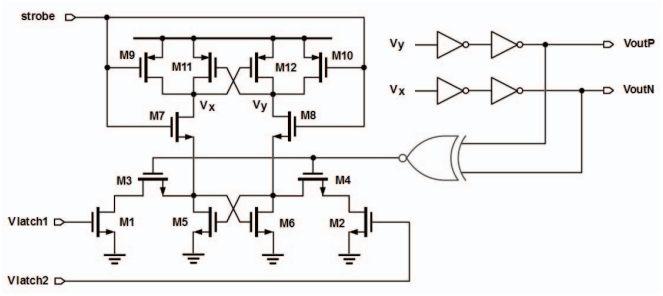

Fig. 2: Regenerative stage of the synchronous comparator. Transistors M_3 and M_4 are introduced to ensure class B operations and to mitigate the kickback noise.

A schematic of the latch stage is shown in Fig. 2. In order to reduce the power consumption a dynamic architecture is used, thus avoiding any DC path between power and ground rails both in the reset state and after positive feedback transients have occurred. In addition, transistors M_3 and M_4 isolate the latch from its driving preamplifier (not shown in the figure) before the full output swing is attained. This significantly reduces the propagation of kickback noise towards the charge-sensitive amplifier.

The latch can be turned into a fast voltage-controlled oscillator (VCO) by means of a dedicated asynchronous logic. Similar techniques are employed in the design of modern charge redistribution Successive Approximation Register (SAR) A/D converters which internally generate the necessary clock signals for SAR operations [6]. As derived from transient simulations, flexible and high-speed ToT digitizations up to 8-bit resolution can be performed in less than 400 ns using selectable on-pixel self-generated clock waveforms in the 100-900 MHz range.

Pixel-to-pixel threshold variations are compensated without the need of a local D/A converter for digital trimming. The offset voltage is periodically sampled and stored on capacitors using Output-Offset Storage (OOS) between the preamplifier and the latch [7]. The lack of a on-pixel D/A converter introduces fundamental advantages in perspective of pixel operations in a harsh radiation environment, avoiding the necessity of dedicated Single Event Upset (SEU) tolerant registers to store the configuration bits for digital trimming. The available area for local temporary data storage (buffering) and signal processing in the digital part can significantly increase. Furthermore efficient calibration schedules can be defined according to online machine operations.

The final layout of the chip, referred to as CHIPIX/TO, is presented in Fig. 3. The analogue part occupies about 50% of the total pixel size.

III. Test results

A picture of the prototype wire-bondend on the test board is presented in Fig. 4. In the measurements all digital control signals are provided by a data pattern generator and the outputs

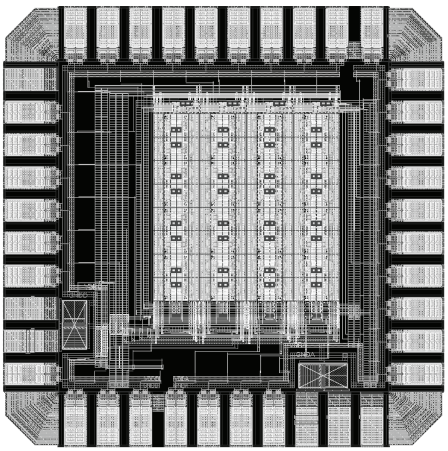

Fig. 3: Complete layout of the CHIPIX/TO chip, 945 μm × 945 μm. The prototype contains 8 × 8 pixels with synchronous front-end and full-analogue readout of all channels.

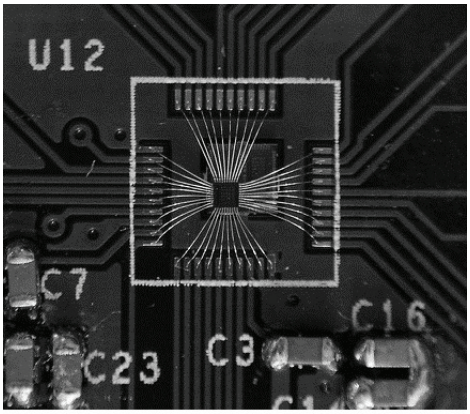

Fig. 4: Prototype chip wire-bondend on the test board.

are acquired with a fast, large bandwidth digital storage oscilloscope. Both the CSA and the discriminator outputs can be inspected independently. Sample oscilloscope waveforms are presented in Fig. 5. In the upper figure, the CSA response to a test input charge of 10 ke^- is shown together with the synchronous hit signal. In the lower one, the fast clock generated internally to the pixel is reported. This clock can be used to drive a fast counter that encodes the signal duration. The on-chip output CMOS driver limits the maximum measurable frequency to about 150 MHz.

In the system, a trade-off exists between signal-to-noise ratio and dead time due to the choice of the bias current in the feedback transconductor. In fact, a higher current determines a faster return to the baseline, but induces also an additional ballistic deficit that affects the SNR.

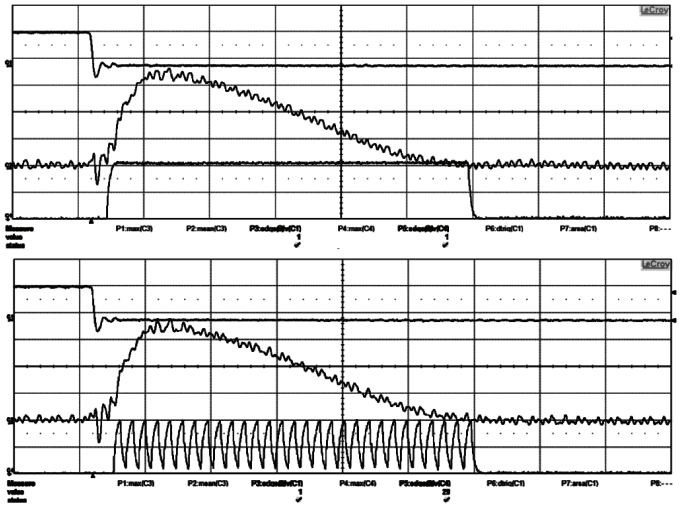

Fig. 5: Sample waveforms at the oscilloscope for 10 ke^- injected charge and 40 nA feedback current. The CSA output pulse with triangular shaping is sampled at 40 MHz. The width of the hit pulse is an integer number of clock cycles (top). Latch operations when turned into a local oscillator for fast ToT counting (bottom). The time base is 50 ns/div.

This aspect can be appreciated in Fig. 6 that reports the ENC versus input capacitance for 10 nA and 40 nA feedback currents. For a typical input capacitance of 100 fF, the noise is respectively 90 and 140 e^- RMS. Due to the differential nature of the transconductor, only half of the feedback current is actually available to discharge the CSA feedback capacitor. The dead time for an expected average signal of 2 fC is therefore 125 ns for 40 nA and 500 ns for 10 nA. The first value is already adequate for operating at the maximum expected rate of 75 kHz per pixel with an efficiency better than 99%.

Before trimming the measured discriminator offset is about 270 e^- RMS, as presented in Fig. 7. The autozeroing is performed by shorting both discriminator inputs to a common voltage and storing the offset in coupling capacitors that connect the low-gain differential amplifier to the latch. For maximum accuracy, the offset compensation cycle should be repeated every 100 μs. A few issues in the autozeroing mechanism were detected in the first version of the prototype and fixed in a second revision.

The threshold dispersion after trimming, measured in the improved prototype, is shown in Fig. 8. The residual offset after calibration is 69.9 e^- RMS and agrees extremely well with the value (70 e^-) predicted with computer simulations to evaluate the latch dynamic offset, which represents the most prominent contribution. A minimum threshold of 600 e^- can therefore be used once the system is calibrated. The overall analogue front-end dissipates 5.4 μW at 1.2 V supply voltage.

First irradiation tests were performed by exposing chip prototypes to 10 keV photons. No significant degradation in the analogue front-end performance were observed after a total ionizing dose of 600 Mrad.

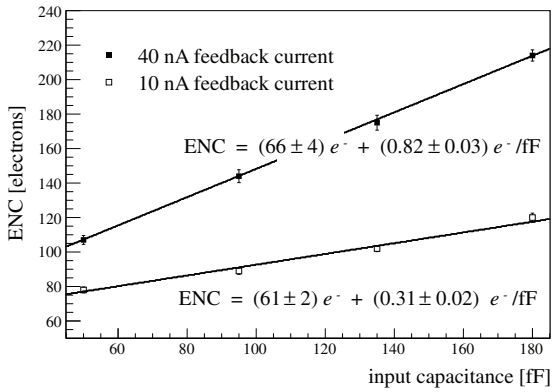

Fig. 6: Equivalent Noise Charge (ENC) versus total input capacitance for two different values of feedback current.

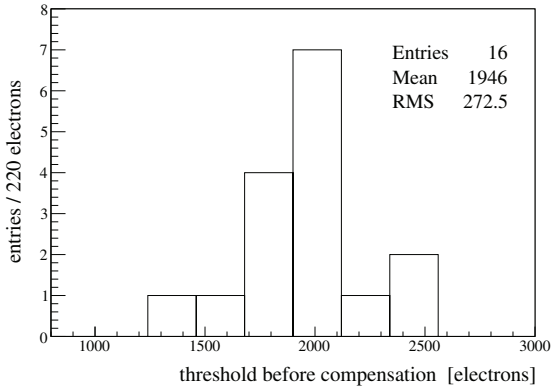

Fig. 7: Threshold distribution before autozeroing.

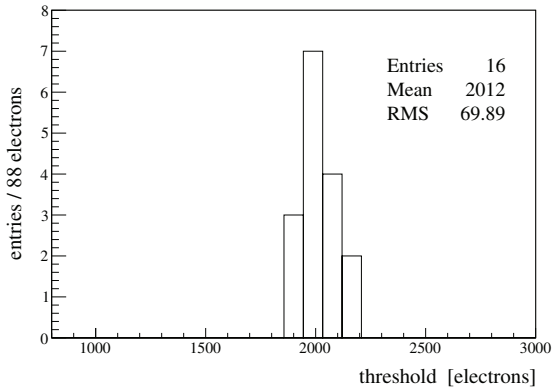

Fig. 8: Threshold distribution after autozeroing. After trimming the measured offset reduces to about 70 e^- RMS.

IV. Conclusions

A pixel front-end chain in 65 nm CMOS has been designed and tested. The key feature of the system is the usage of a clocked comparator with embedded offset calibration. When a signal is detected, the discriminator is automatically turned into a high-speed oscillator that allows fast, multi-bit charge encoding with time-over-threshold measurement. The noise is primarily dictated by the current chosen to discharged the CSA feedback capacitor, while no significant contribution induced by the digital signals present in the pixel cell has been observed. The design satisfies in term of rate capability, sensitivity and power consumption the stringent requirements envisaged for the Phase-II upgrades of the main LHC detectors.

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