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A synchronous analog very front-end in 65 nm CMOS with local fast ToT encoding for pixel detectors at HL-LHC

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Abstract: This work describes the design, in 65 nm CMOS, of a very compact, low power, low threshold synchronous analog front-end for pixel detectors at HL-LHC. Threshold trimming is avoided using offset compensation techniques. Fast ToT encoding is possible, as the comparator can be turned into a Local Oscillator up to several hundreds MHz. Two small prototypes have been submitted and tested; a X-ray irradiation up to 600 Mrad has been performed. Detailed results in terms of gain, noise, ToT and threshold dispersion are presented. This design will be part of the CHIPIX65 demonstrator and of the RD53A chip.

Keywords: Analogue electronic circuits; Front-end electronics for detector readout; Radiation-hard electronics

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Contents

1 Introduction

In 2026 the High Luminosity Large Hadron Collider (HL-LHC) [1] will start its operation. The machine will increase the luminosity compared to the present LHC accelerator performance, with the goal of reaching 3000 fb^{-1} in 10 years. As a consequence, the experiments will have to deal with extreme operating conditions, including a pile-up per event between 140 and 200 and for the innermost layer of the silicon pixel detector an expected level of radiation of 1 Grad in 10 years and a pixel rate around 3 GHz/cm^2.

These requirements will lead to an increase in granularity of the silicon sensor (in the order of 50 μm $\times$ 50 μm) and in a reduction of the thickness (around 100–150 μm). As a consequence, the signal provided to the front-end electronics is smaller, leading to strict requirements on low threshold (1 ke^-) and low noise (below 150 e^- for a sensor capacitance of 100 fF) [2] . In addition, since the detector granularity will be increased and the total amount of data will be significantly higher, the introduction of more digital intelligence per pixel is needed. For all these reasons, studies on a new readout chip for silicon pixel detectors at HL-LHC have been started. A 65 nm CMOS technology has been identified as an appropriate choice for this purpose. In this context, the RD53 collaboration at CERN [3] has been established. INFN is part of this collaboration through the CHIPIX65 project [4].

In this paper the design of a synchronous analog front-end for silicon pixel sensors at HL-LHC is described. This architecture is part of the CHIPIX65 demonstrator and of the RD53A large scale chip. Section 2 contains the description of the design. In section 3 a short summary of the prototypes submitted to the foundry is given. An overview of test results during and after a 600 Mrad irradiation is provided in section 4. Section 5 discusses the inclusion of the front-end into the CHIPIX65 demonstrator.

2 Architecture description

The scheme of the architecture is presented in figure 1. It features a single stage Charge Sensitive Amplifier (CSA) with a Krummenacher feedback AC coupled to a synchronous discriminator composed of a Differential Amplifier (DA) and a positive feedback latch [5].

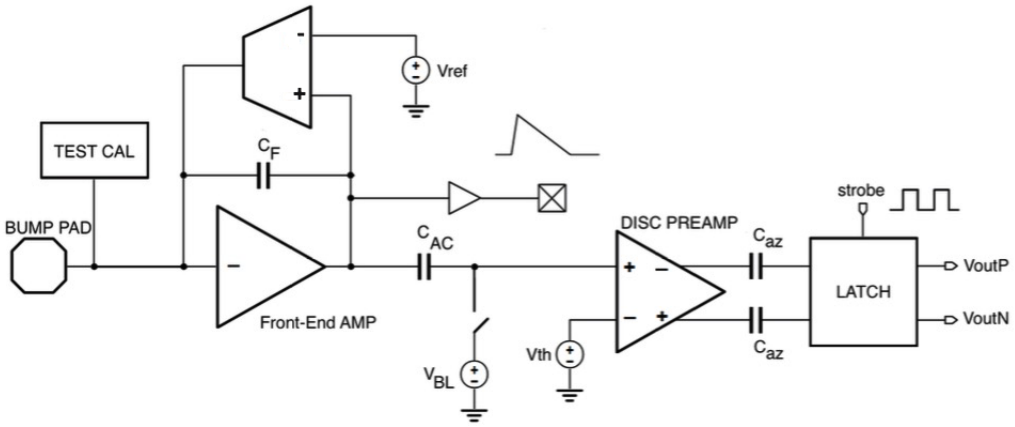

Figure 1. Synchronous front-end architecture.

The CSA contains a telescopic cascode stage with current splitting to minimize noise contributions and a source follower to improve the driving strength. The Krummenacher feedback is designed to provide both the sensor leakage current compensation and the constant current discharge of the feedback capacitor. The larger the current the faster the preamplifier signal returns to the baseline. As a reference, a 10 nA current results in a 400 ns-long signal for an input charge of 10 ke$^-$, which is reduced to around 100 ns for a 40 nA current. Two capacitors, equal to 2.5 and 4 fF respectively, have been included in order to implement different gain values. In addition, a calibration circuit featuring an injection capacitance of around 8 fF has been designed to provide an input charge in the desired interval, which is 1–30 ke$^-$. The preamplifier open loop gain is around 60 dB.

Due to mismatch effects, considerably relevant in deep submicron technologies like 65 nm, the output baseline of the first stage is subject to quite large fluctuations (of the order of tens of mV) between different channels. In order to get rid of this behavior an AC coupling to the discriminator DA has been implemented.

The DA provides a further small gain (around 2). Transistor mismatch results in an offset of the DA output voltage between pixels. In this design an offset compensation using internal capacitors ("auto-zeroing") has been chosen. A compensation phase of around 100 ns every 100 µs is required.

The differential signal is fed into the positive feedback latch stage, which performs the comparison and generates the discriminator output. This stage has been designed to minimize mismatch effects causing a dynamic offset resulting in an additional threshold dispersion. Furthermore, the latch can be turned into a local oscillator up to 800 MHz using an asynchronous logic feedback loop. The latter includes a current-starved delay line which is used to tune the oscillation frequency by changing the value of a dedicated bias current. A similar technique is frequently used in the design of modern Successive Approximation Register (SAR) Analog to Digital Converters which generate

internally the clock needed for operation [8]. It can be used to perform a fast Time-over-Threshold (ToT) counting. Figure 2 shows how the principle of the fast ToT works. When the signal moves above the threshold, the discriminator output starts to oscillate at the chosen frequency. Then it stops oscillating once the signal is finished. By counting the number of oscillations it is therefore possible to have a precise measurement of the ToT.

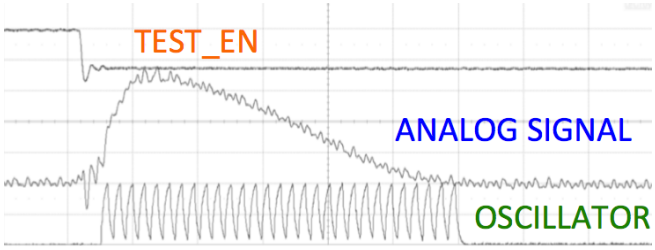

Figure 2. ToT for a 10ke$^-$ input signal.

3 Prototypes

Two small prototypes, called $CHIPIX\_VFE\_1/TO$ and $CHIPIX\_VFE\_2/TO$ have been submitted and tested: the layout is shown in figure 3. They both consist of a 8×8 pixel matrix with analog readout of CSA and discriminator outputs for each pixel. Also the discriminator output, containing the fast ToT information, has been buffered. In the prototypes, in fact, no counters have been included. Therefore, the oscillator output has been directly monitored by using an oscilloscope. A test board has been used to characterize the two prototypes: it provides mechanical sustain, wire-bonding landing pads, power and necessary input/output access points. The testing phase has been started after the chip has been wire bonded to the setup. A picture of the board with the chip lying under a protective box is shown in figure 4. $CHIPIX\_VFE\_2/TO$ features some optimizations in the design. In particular, measurements on the $CHIPIX\_VFE\_1/TO$ prototype showed a threshold dispersion around 174 e$^-$, after threshold compensation, while in the uncompensated configuration the measured dispersion was 272 e$^-$. Therefore, an improvement thanks to auto-zeroing has been seen, but not adequately large. Successive simulations showed that the main cause of this result was the still large residual dynamic offset of the latch, a contribution which is not eliminated by the auto-zeroing. As a consequence, concerning the second prototype the transistor sizes in the latch stage have been increased in order to reduce this contribution. Measurements on $CHIPIX\_VFE\_2/TO$ then showed a very significant improvement in threshold dispersion, reduced down to 70 e$^-$. In addition, noise measurements have shown encouraging results, with an ENC around 100 e$^-$ for an input capacitance equal to 50 fF. A detailed description of the measurements is reported in [5].

4 Irradiation measurements

The $CHIPIX\_VFE\_2/TO$ prototype has been tested under irradiation up to 600 Mrad, using a X-ray machine at CERN. The chip has been irradiated at working conditions with the default biases and the readout active. At fixed steps the main parameters of 16 pixels have been monitored. In

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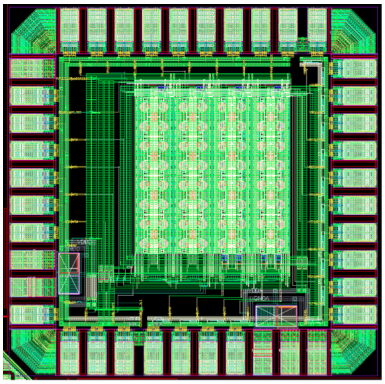

Figure 3. Layout of the prototypes.

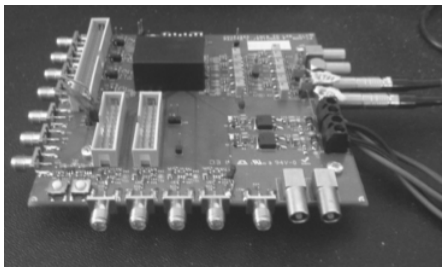

Figure 4. Test board.

addition, the same values have been measured 70 hours and 25 days after the end of the irradiation procedure, having kept the chip at room temperature. In this way, the behavior of the chip after annealing has been studied. The following plots contain average values for 16 pixels. As shown in figure 5 the amplitude of the analog signal, measured for an input signal of 5 ke$^-$, remains almost steady with irradiation. On the other hand, the peaking time tends to increase with an irradiation level larger than 100 Mrad. Figure 6 also shows that there is a partial recovery with annealing. Although the rise of the peaking time is significant, it does not represent a major issue for the front-end operation. In fact, also in the case of the highest value, around 35 ns at 600 Mrad, the time-walk between the smaller signal (1 ke$^-$) and the largest one (30 ke$^-$) in the discriminator is still below one clock cycle. Another key analog parameter is noise. In figure 7 the ENC as a

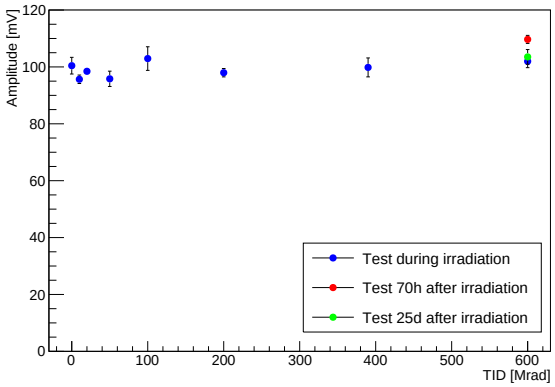

Figure 5. CSA amplitude vs radiation.

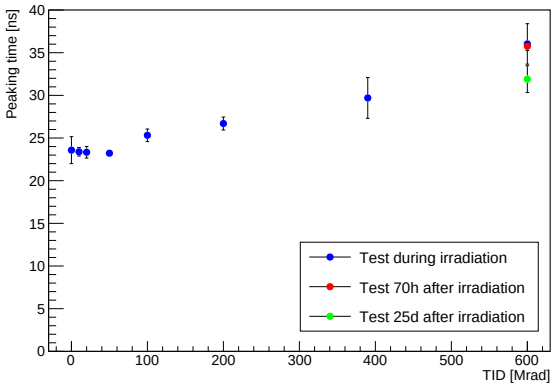

Figure 6. CSA peaking time vs radiation.

function of input capacitance is presented for a single pixel before and after irradiation and after annealing. In all cases the linearity is preserved, but radiation damage results in a slope increase, partially recovered with the annealing. However, for the typical sensor capacitance, which is 50 fF, the discrepancy caused by radiation is only about 10%.

In addition, also the ToT frequency in oscillation mode has been monitored. Results are shown in figure 8. The frequency tends to decrease linearly with irradiation, with a partial recovery after irradiation. This effect can be compensated by trimming the current flowing in the delay line which controls the frequency, moving it back to the original value. Therefore, the fast ToT counting works

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properly also with a TID irradiation equal to 600 Mrad. Furthermore, during irradiation the total analog current consumption of the chip has been monitored, without changing any bias trimmer on the board. At 600 Mrad a slight decrease of about 4% compared to the pre-irradiation case has been observed.

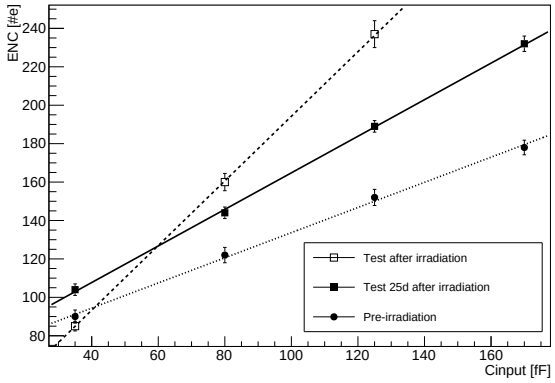

Figure 7. Noise vs input capacitance.

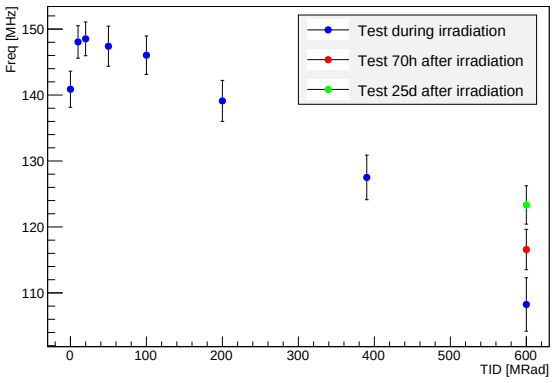

Figure 8. ToT frequency vs radiation level.

5 CHIPIX65 demonstrator

The CHIPIX65 demonstrator is a $3.5 \times 5.1\,\mathrm{mm}^2$ chip which features a small and complex pixel array [6]. The layout of the chip submitted to the foundry is presented in figure 9. It consists of a 64×64 pixel matrix featuring two flavors of analog front-ends, occupying half of the matrix each: in addition to the synchronous design described in this paper, an asynchronous architecture [7] is included. The matrix contains also a digital architecture organized in 4×4 pixel regions. Furthermore, the chip periphery is equipped with the building blocks needed for biasing, readout and monitoring. Regarding the synchronous front-end, two versions have been included. The first

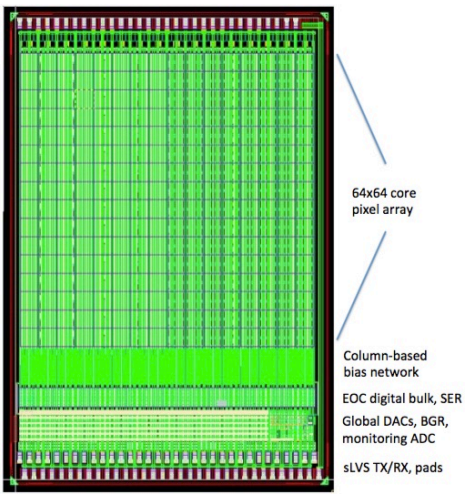

Figure 9. CHIPIX65 demonstrator layout.

one is exactly the same implemented in the $CHIPIX\_VFE\_2/TO$ prototype, in order to have a

confirmation of the measurement results over a larger number of pixels. The second one contains the following optimizations, based on the small prototypes measurements and CAD simulations. Firstly, the CMOS switches used in the offset compensation part have been implemented with Enclosed Layout Transistors (ELT). Radiation damage on linear transistors, in fact, is responsible for an increase of the Source-Drain leakage current, which can lead to a faster discharge of the offset compensation capacitors. ELTs allow to get rid of the leakage current effect. In addition, the sizing of the latch transistors has been improved in order to further reduce the dynamic offset contribution. Finally, in order to ensure better isolation from the digital substrate, all the analog part of the layout has been included in a Deep N-well. The layout of the pixel analog front-end has been reshaped in a squared ($35 \times 35\ \mu m^2$) configuration to be compatible with the RD53A design.

6 Summary

A synchronous analog front-end for silicon pixel sensors at HL-LHC has been designed and tested. The architecutre features an offset compensation via capacitors and a local oscillator for fast ToT counting. Measurements on small prototypes confirm that the design is low noise (ENC around 100 e^- for an input capacitance of 50 fF) and the threshold dispersion is around 70 e^-. A X-ray irradiation campaign has been performed up to 600 Mrad, after which the chip works properly. Beyond 100 Mrad, a significant increase in peaking time is noticed, but with no relevant impact on the discriminator performance. In addition, at 600 Mrad an important rise in the slope of ENC versus input capacitance is observed. Nevertheless, for the expected sensor capacitance, which is 50 fF, the increase is only in the order of 10%. Regarding the fast oscillator for ToT counting, a linear decrease of the frequency with radiation is observed. This effect can be easily compensated by tuning the bias current which controls the frequency in order to restore the original value. All the results are compliant with the RD53A specifications. An optimized version of the design is part of the CHIPIX65 demonstrator chip.

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