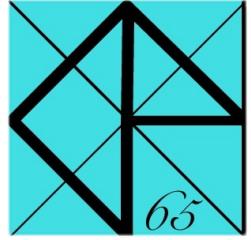


# Basic CHIPIX65 demonstrator informations

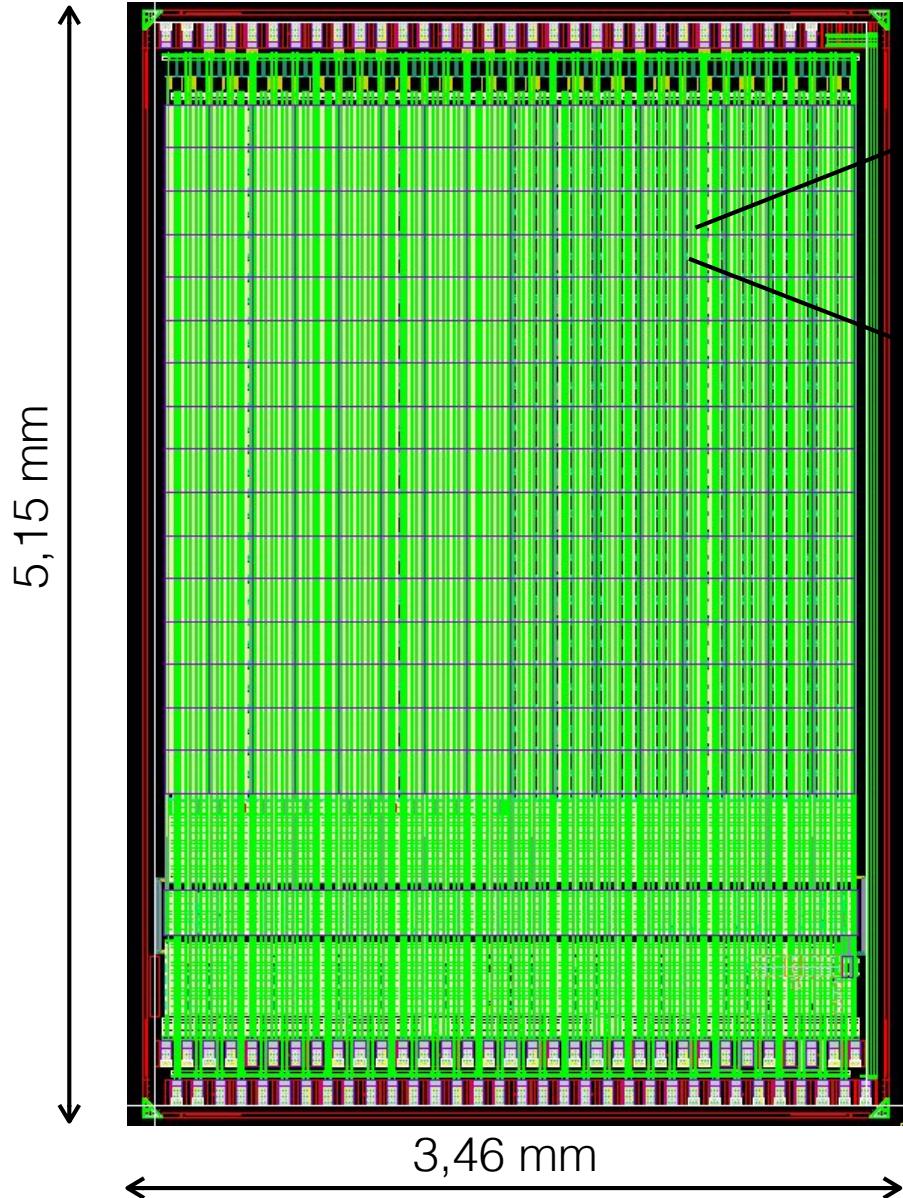
<https://gitlab.cern.ch/CHIPIX65/CHIPIX65>



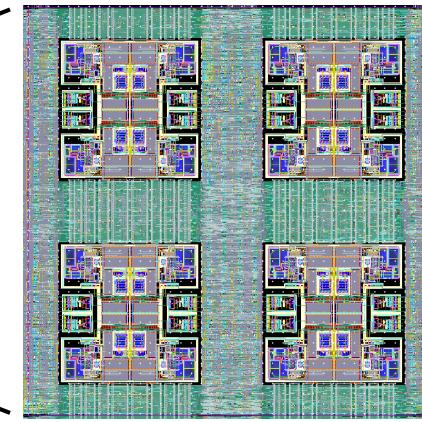
# CHIPIX65 demonstrator



CHIPIX65: 2013 CALL project INFN - CSN5  
Web-site: <http://chipix65.to.infn.it>



(2x2) Analog Islands  
on (4x4) pixel region digital architecture



submitted and  
approved  
on 5-July-2016

## 64x64 pixel matrix - 50x50 $\mu\text{m}^2$

HL\_HLC flux rates: 3 GHz/cm<sup>2</sup>  
Trigger latency : 12,5 us  
Low power consumption  
5-bit ToT signal digitisation  
In-time threshold <1200 e-  
Noise ~100e- @50fF input capacitance

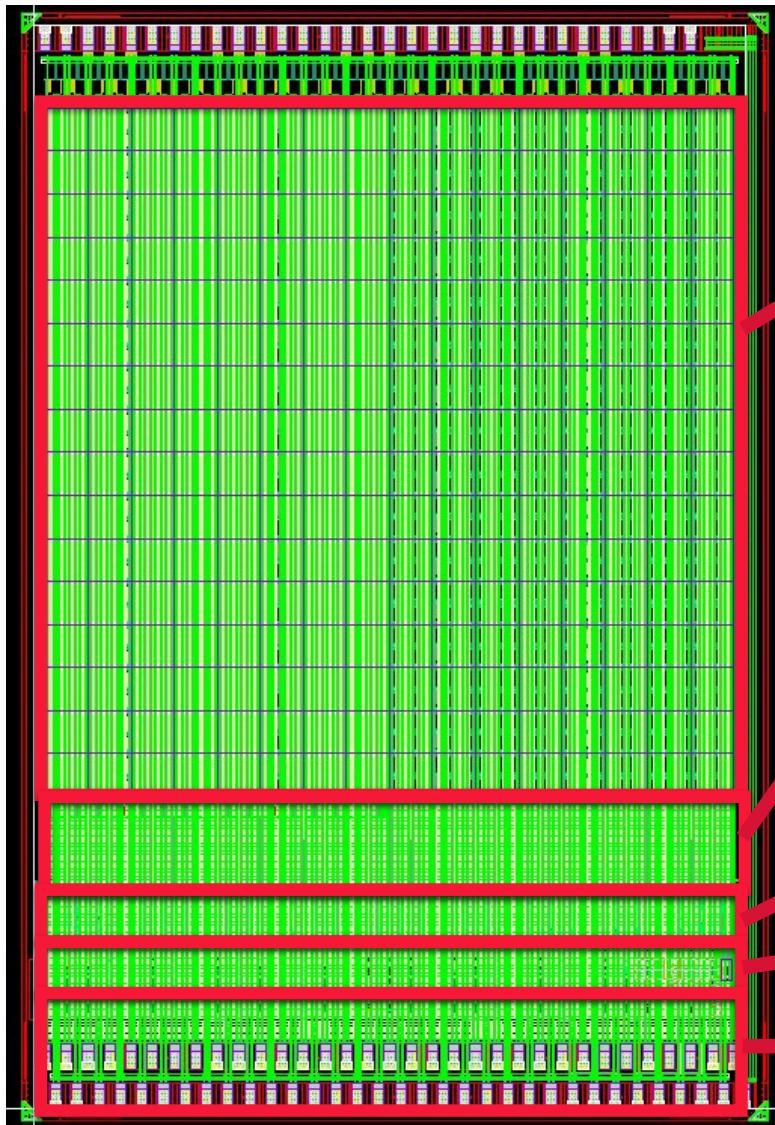
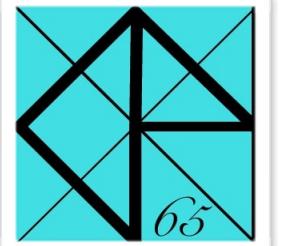
VFE & IP-block developed in RD53

~3M of digital standard cells

INFN institutes: To, Ba, Le, Mi, Pd, Pg, Pi, Pv



# CHIPPIX65 demonstrator



**Pixel Matrix** (digital+analog)

- Organised in (16x16) Pixel Region VFE-Analog
- Pixel Region Digital

**Column Bias** (analog)

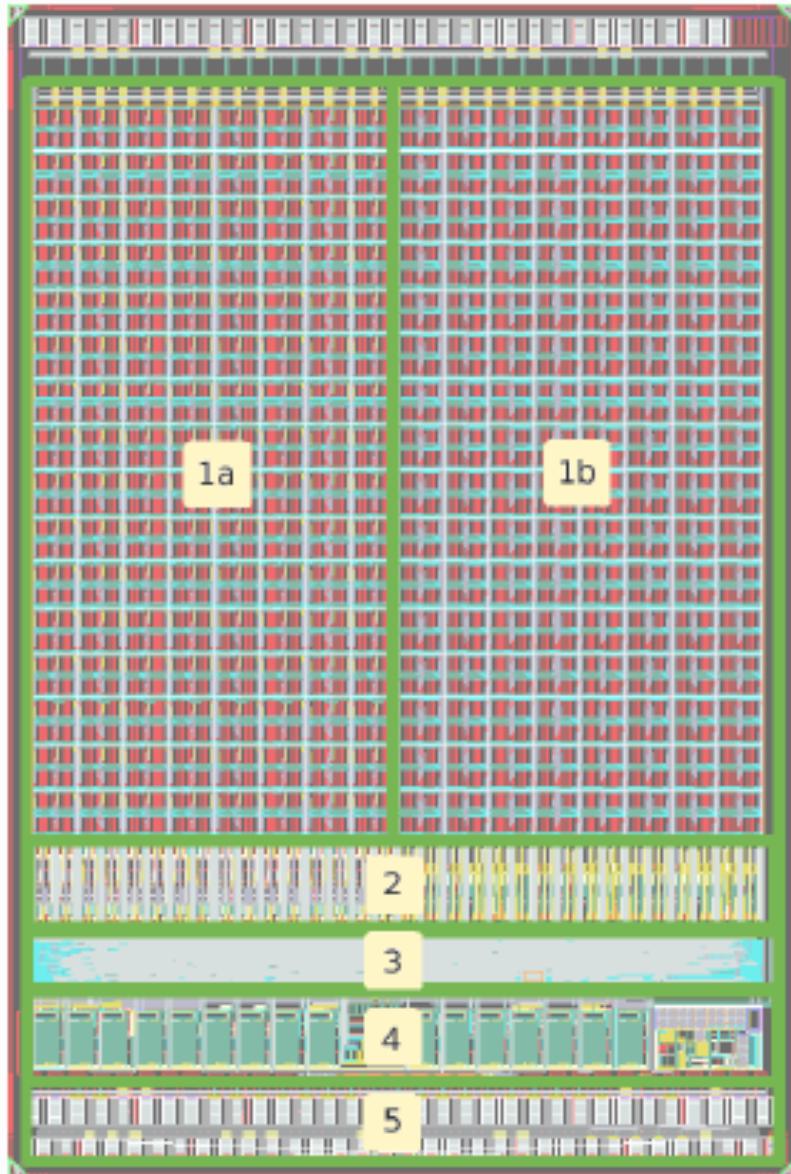
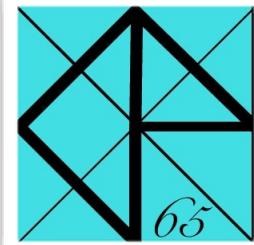
**End of Column** (digital)

**Global Bias** (analog)

**I/O** (IP-Block)



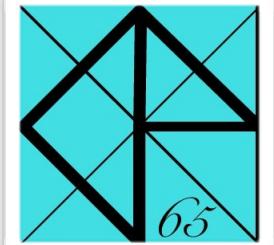
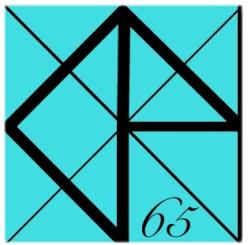
# CHIPIX65 layout



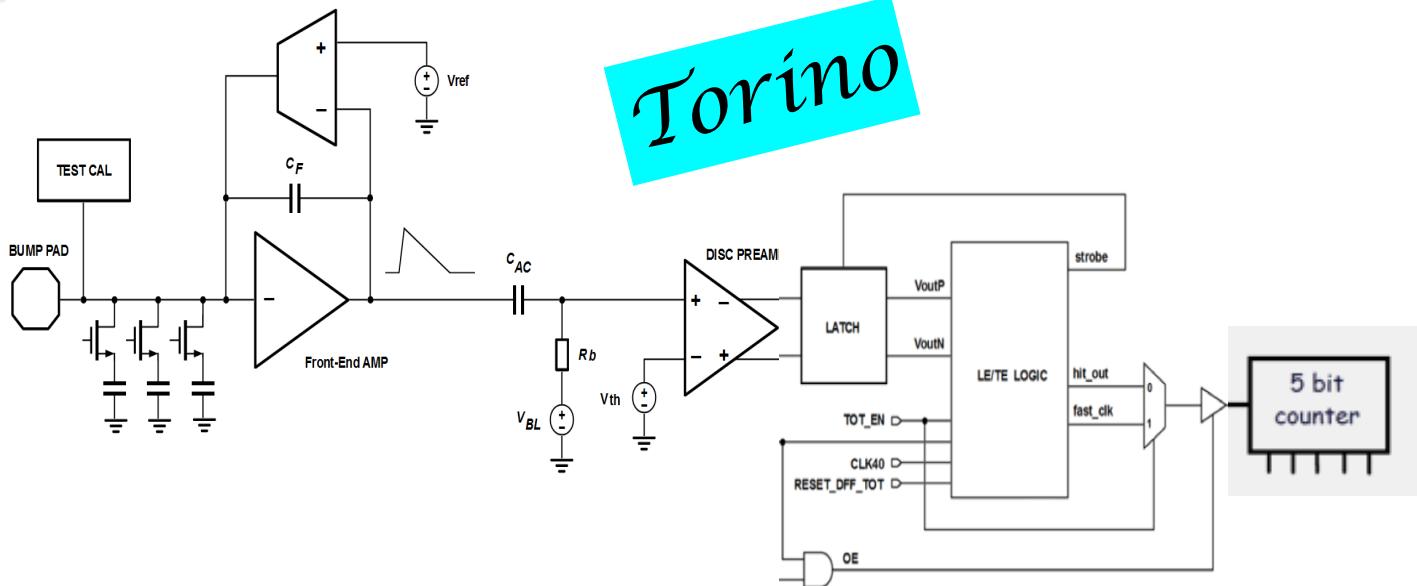
1.  $64 \times 64$  Pixel Array
  - a Synchronous Front-End Architecture
  - b Asynchronous Front-End Architecture
2. Column Bias Cells with current mirrors (Analog)
3. End of Column and SER (Digital)
4. Global DACs, BGR and ADC
5. SLVS TX/RX and I/O cells

VFE-Torino  
VFE-Bg/Pv

- FIFO-based readout architecture, SPI-based chip configuration
- integration of available silicon-proven IP-blocks designed for RD53:
  - Bandgap Voltage Reference (Pavia INFN)
  - SLVS transmitters/receivers (Pisa INFN)
  - High-speed SER (Pisa INFN)
  - 10-bit biasing DAC (Bari INFN)
  - 12-bit monitoring ADC (Bari INFN)
- modified CERN rad-hard I/O library



# Synchronous Analog FE



32x64 pixels

- **PREAMPLIFIER**
  - One stage CSA with Krummenacher feedback
- **Synchronous DISCRIMINATOR**
  - (AC coupled to CSA)
  - off-set compensated diff.amplif. + latch;
  - **FAST Time-over-Threshold**
    - Local oscillator strobing Latch (to 800MHz)
- **Calibration circuit**
  - digital signal + DC calibration leve

TESTED after IRRADIATION

## Performance SUMMARY

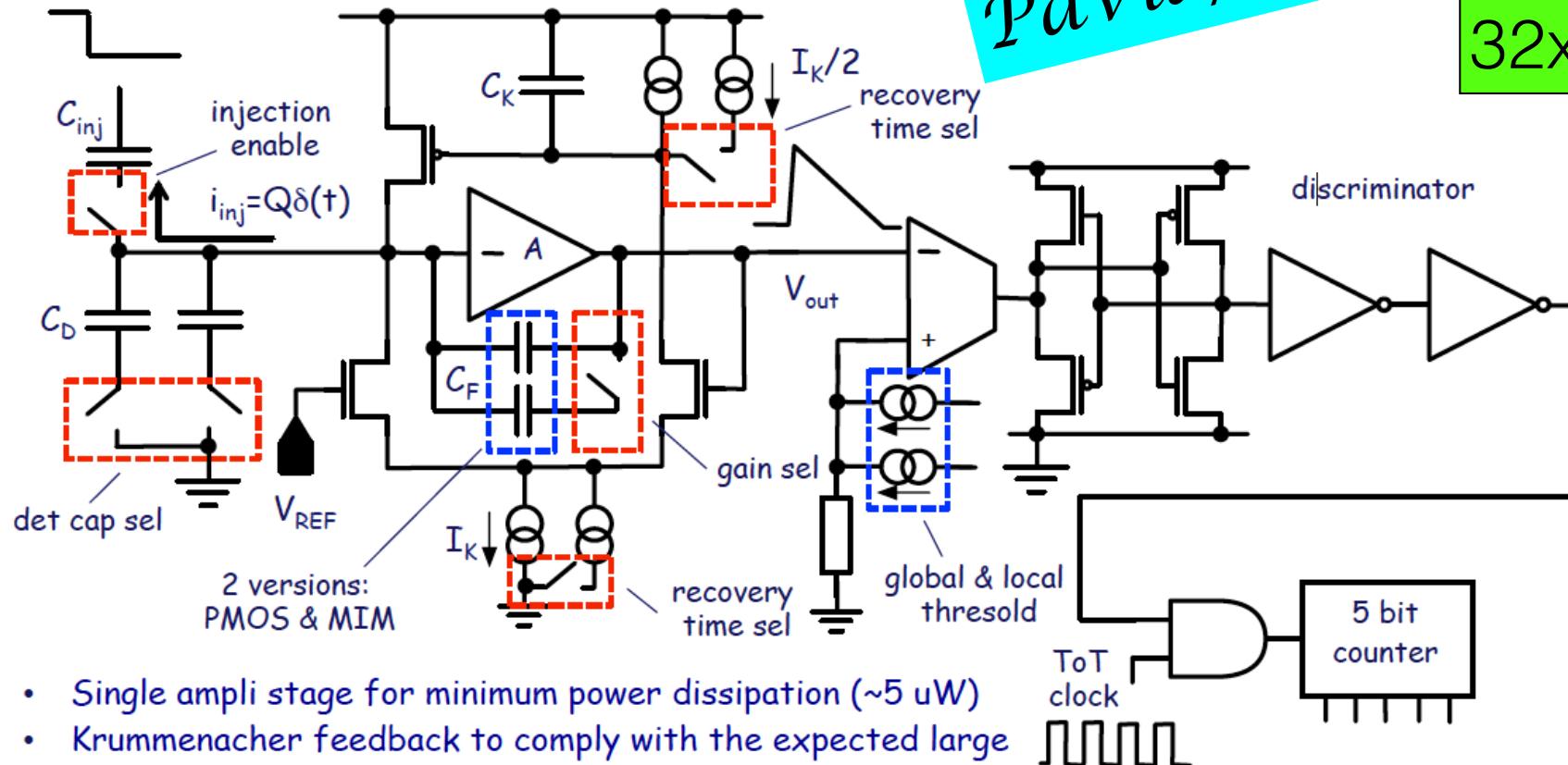
- Compact: ~25um x 40 um
- Low power: < 5.5 uW (with ToT logic)
- Low noise: ENC=100e @ $C_{det}=100$  fF
- Leakage compensation: up to 50nA/pixel
- Fast Charge measurement:
  - 10 ke in : 90 / 180 / 360 ns (Fast/Medium/Low recovery current)
  - up to 7-8bit (125-250e /ADC) - no ext clock
- NO Threshold-Trimming:
  - autozeroing made by hardware



# Asynch Analog FE

Pavia/Bg

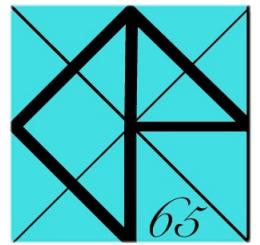
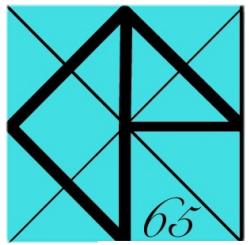
32x64 pixels



- Single ampli stage for minimum power dissipation ( $\sim 5 \mu W$ )
- Krummenacher feedback to comply with the expected large increase in the detector leakage current (up to  $\sim 10 \text{ nA}$ )
- 30000 electron maximum input charge expected,  $\sim 450 \text{ mV}$  preampli output dynamic range
- Selectable gain, recovery current and detector emulating capacitance
- 40 MHz clock, 5 bit dual edge counter, 400 ns maximum ToT

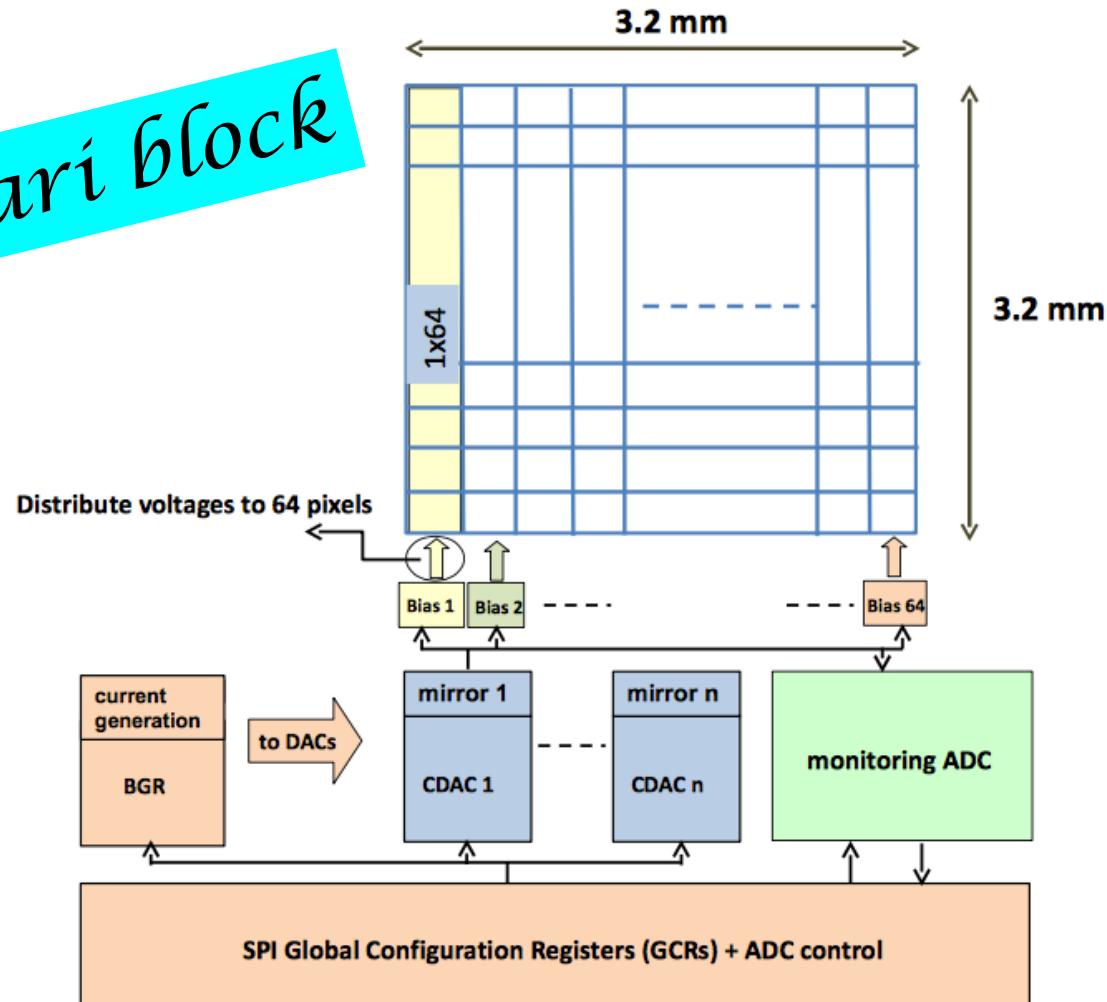


TESTED after IRRADIATION



# Column & Global Bias

Bari block



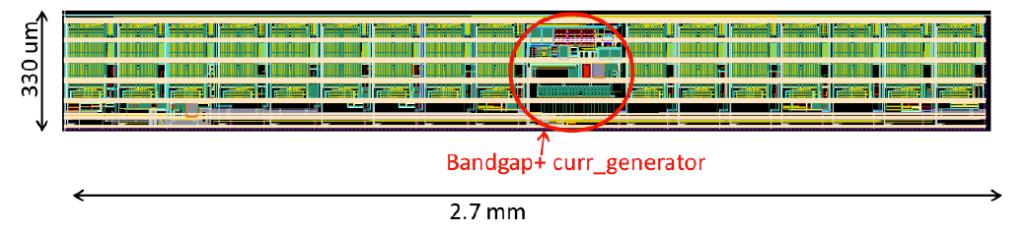
Current are mirrored from DAC to Bias-cells (one per pixel column)

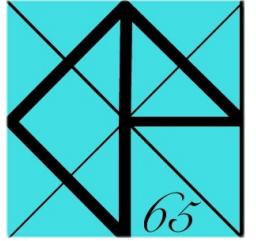
Robust solution for large pixel matrix (thinking to 400x400 pixel)

- 16 10-bit DACs:
- 6 for A-AFE
  - 9 for S-AFE
  - 1 for both

1 bias-cell block / Pixel Col

Bg from Pv

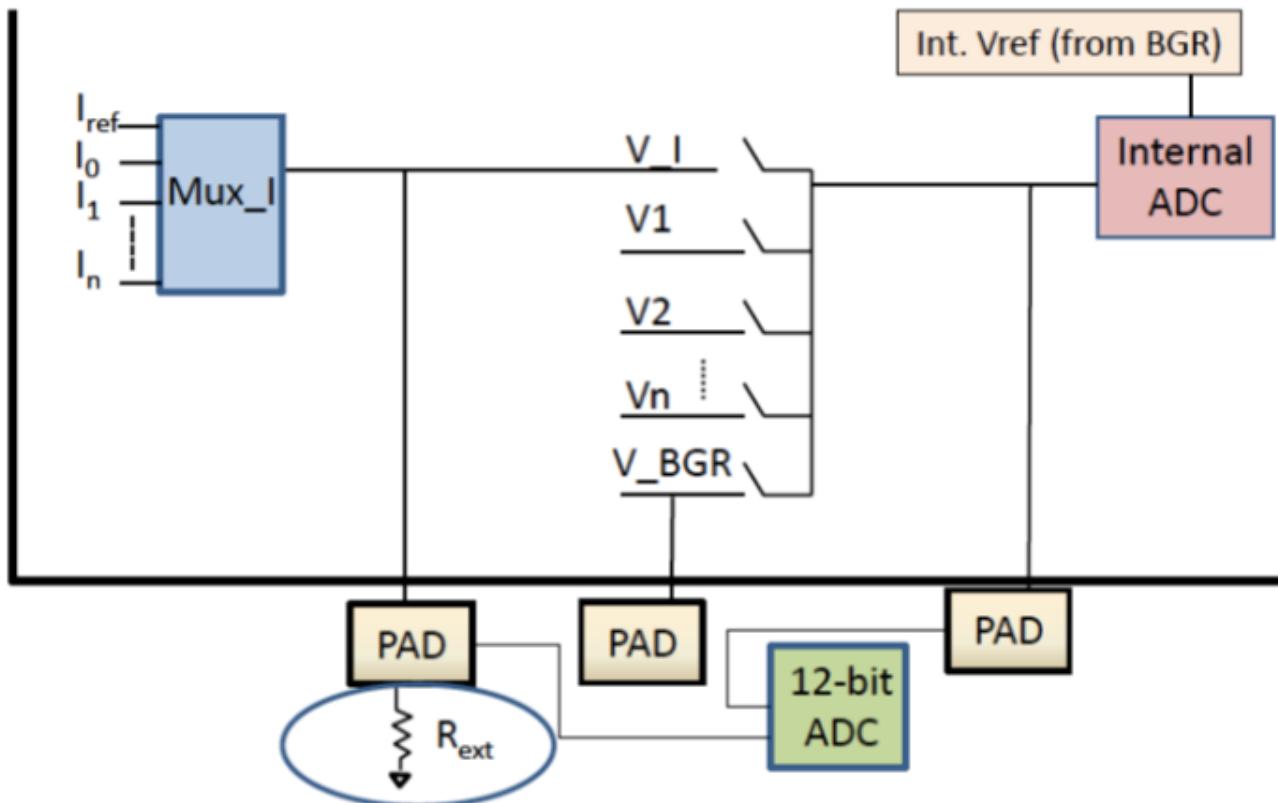




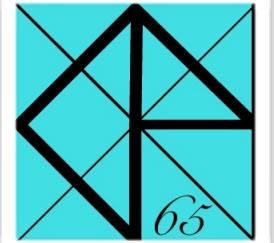
# Column & Global Bias and monitoring



All currents are mirrored and can be monitored

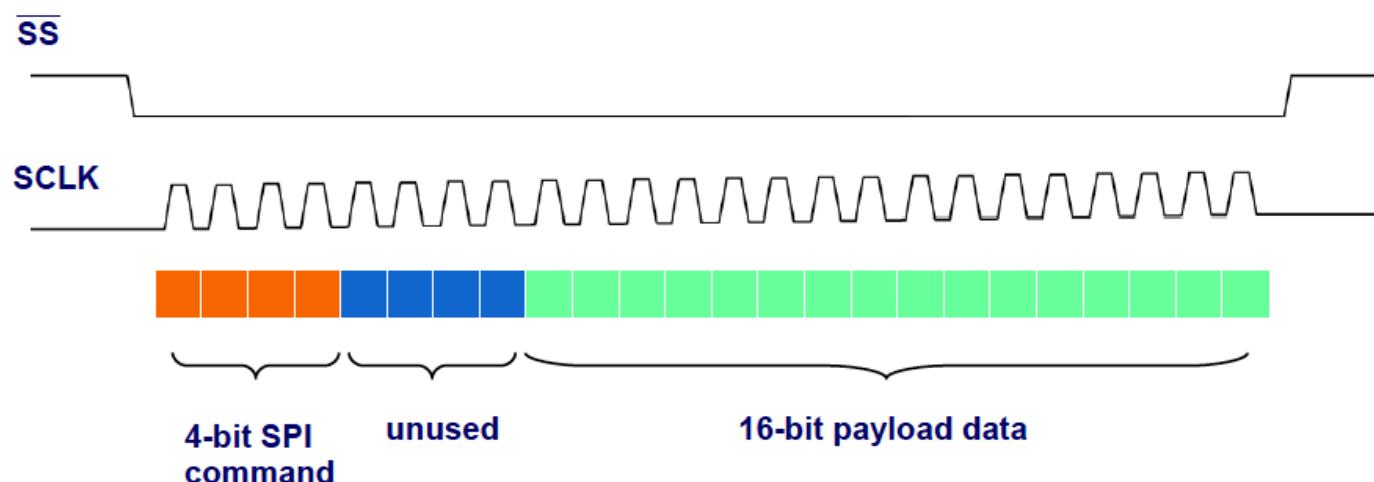


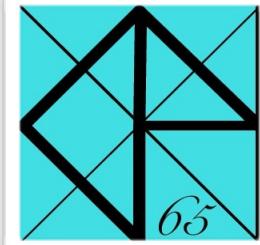
- External high precision resistor (0.1%,  $\pm 25$  ppm/ $^{\circ}\text{C}$ ) : 3 different values required
- 12-bit ADC (and multimeter) to calibrate internal ADC
- Store in database values of  $V_{BGR}$ ,  $I_{ref}$  and LSB of internal ADC



# EoC: configuration

- prototype configuration performed at 13.33 MHz through **fully-duplex synchronous SPI master/slave transactions** ( $\text{CPOL} = 0$ ,  $\text{CPHA} = 1$ )
- **24-bit SPI-words** (frames) contains configuration commands and payload data
  - a dedicated control logic interfaces with a customized **SPI slave-port** and writes/reads configuration data to registers according to commands
  - **Global Configuration Registers (GCR)** [224-bit]
  - **Pixel Configuration Registers (PCR)** [8-bit/pixel]
  - **EOC Configuration Registers (ECCR)**
  - **ADC and autozeroing control commands**



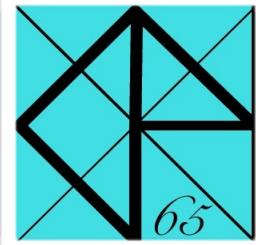


# GCR (1)

<https://gitlab.cern.ch/CHIPIX65/CHIPIX65/blob/master/rtl/eoc/config/README.md>

GCR_DATA slice	LEF bus name	Description	Binary reset value	Additional notes
GCR_DATA[4:0]	-	Torino 5-bit programmable delay for PHI_AZ	5'b00000	zero-delay
GCR_DATA[12:5]	-	Torino 8-bit programmable high-level for PHI_AZ	8'b0001_0100	0.5us high, 20 x 25ns
GCR_DATA[26:13]	-	Torino 14-bit programmable low-level for PHI_AZ	14'b0011111_0001100	99.5us low, 3980 x 25ns
GCR_DATA[36:27]	CFG_CTRLTOT_TO[9:0]	Torino 10-bit ICTRL_TOT global DAC	10'b00_0110_0100	1 uA
GCR_DATA[46:37]	CFG_VTH_TO[9:0]	Torino 10-bit VTH_DISC global DAC	10'b11_1111_1111	highest threshold
GCR_DATA[56:47]	CFG_VBL_TO[9:0]	Torino 10-bit VBL_DISC global DAC	10'b01_1100_0010	485 mV
GCR_DATA[66:57]	CFG_BIASP1_TO[9:0]	Torino 10-bit IBIASP1 global DAC	10'b00_0110_0100	0.5 uA
GCR_DATA[76:67]	CFG_BIASP2_TO[9:0]	Torino 10-bit IBIASP2 global DAC	10'b00_1001_0110	1.5 uA
GCR_DATA[86:77]	CFG_DISC_TO[9:0]	Torino 10-bit IBIAS_DISC global DAC	10'b00_1100_1000	1 uA
GCR_DATA[96:87]	CFG_BIAS_SF_TO[9:0]	Torino 10-bit IBIAS_SF global DAC	10'b00_0110_0100	0.5 uA
GCR_DATA[106:97]	CFG_KRUM_TO[9:0]	Torino 10-bit VREF_KRUM global DAC	10'b01_1110_1010	490 mV
GCR_DATA[116:107]	CFG_FEED_TO[9:0]	Torino 10-bit IBIAS_FEED global DAC	10'b00_0101_0000	20 nA
GCR_DATA[141:132]	CFG_LDAC_BGPV[9:0]	Bergamo/Pavia 10-bit ILDAC global DAC	10'b00_1010_0000	1.6 uA
GCR_DATA[151:142]	CFG_GDAC_BGPV[9:0]	Bergamo/Pavia 10-bit IGDAC global DAC	10'b11_1111_1111	highest threshold
GCR_DATA[161:152]	CFG_ref_krum_BGPV[9:0]	Bergamo/Pavia 10-bit VRIF_KRUM global DAC	10'b01_0010_1100	300 mV
GCR_DATA[171:162]	CFG_Ikrum_BGPV[9:0]	Bergamo/Pavia 10-bit IKRUM global DAC	10'b00_0011_0010	12.5 nA
GCR_DATA[181:172]	CFG_fc_bias_BGPV[9:0]	Bergamo/Pavia 10-bit IFC_BIAS global DAC	10'b00_1100_1000	2 uA
GCR_DATA[191:182]	CFG_inpa_BGPV[9:0]	Bergamo/Pavia 10-bit IPA_IN_BIAS global DAC	10'b01_0010_1100	30 uA
GCR_DATA[201:192]	CFG_CAL[9:0]	Charge-injection calibration DAC	10'b00_0000_0000	No calibration (negative pulse)

TORINO  
VFE  
Bq/Pv



# GCR (2)

<https://gitlab.cern.ch/CHIPIX65/CHIPIX65/blob/master/rtl/eoc/config/README.md>

## Global Bias and Mon

GCR_DATA[121:117]	CFG_IREF[4:0]	5-bit programmable DAC reference current Iref	5'b1_0100	Nominal 4 uA for VBGR = 400 mV
GCR_DATA[126:122]	CFG_BGR[4:0]	5-bit configuration for BGR	5'b0_0101	-
GCR_DATA[131:127]	CFG_MON_MUX[4:0]	5-bit monitoring multiplexer	5'b1_0000	Monitor Iref

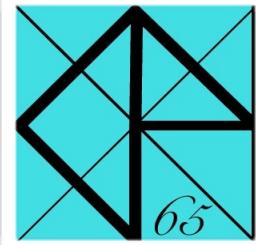
## Monitoring ADC

GCR_DATA[202]	CFG_ADC[0]	Bari ADC operating mode	1'b0	Self-calibration mode
GCR_DATA[206:203]	CFG_ADC[4:1]	Bari ADC 4-bit programmable gain for input transconductor	4'b1000	-
GCR_DATA[212:207]	CFG_ADC[10:5]	Bari ADC 6-bit programmable discharge current	6'b011_100	-
GCR_DATA[218:213]	CFG_ADC[16:11]	Bari ADC 6-bit programmable charge current	6'b011_100	-
GCR_DATA[223:219]	CFG_ADC[21:17]	Bari ADC 5-bit programmable comparator threshold	5'b10000	-



# ECCR

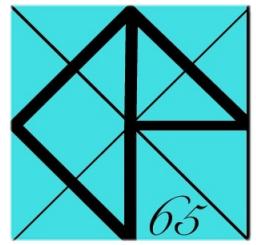
<https://gitlab.cern.ch/CHIPIX65/CHIPIX65/blob/master/rtl/eoc/config/README.md>



ECCR_DATA slice	RTL net name	Description	Binary reset value	Additional notes
ECCR_DATA[9:0]	trigger_latency	programmable trigger latency	10'b0	zero trigger latency
ECCR_DATA[10]	triggerless0_triggered1	triggerless vs. triggered operating mode	1'b0	triggerless operating mode
ECCR_DATA[11]	binary0_tot1	binary only vs. charge encoding (ToT) mode	1'b0	binary-only operations
ECCR_DATA[12]	lowDeadtime0_highDeadtime1	high vs. low Front-End deadtime	1'b0	actually dont-care
ECCR_DATA[13]	gray0_binary1	gray vs. binary timestamp encoding	1'b0	use Gray-encoded timestamp values
ECCR_DATA[14]	8b10bEnable0_8b10bDisable1	enable vs. disable 8b/10b encoding	1'b0	enable 8b/10b encoding
ECCR_DATA[31:16]	mcd_mask	MASK word for Macro-Column Drained (debug)	16'b0	no masking on MCD readout



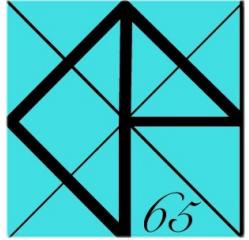
# PCR



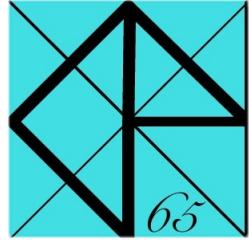
<https://gitlab.cern.ch/CHIPIX65/CHIPIX65/tree/master/rtl/pixel>

Pixel Configuration Registers (PCR) startup values - Bergamo/Pavia			
PCR_DATA slice	Description	Binary reset value	Additional notes
PCR_DATA[0]	MASK	1'b0	Same position for both Torino and Bergamo/Pavia
PCR_DATA[1]	CAL_EN	1'b0	Same position for both Torino and Bergamo/Pavia
PCR_DATA[2]	GAIN_SEL	1'b0	-
PCR_DATA[6:3]	[3:0] TH_DAC	4'b1000	-
PCR_DATA[7]	POWER_DOWN	1'b0	-

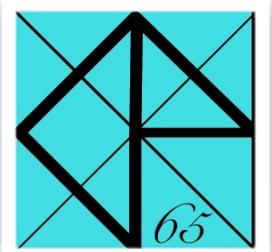
Pixel Configuration Registers (PCR) startup values - Torino			
PCR_DATA slice	Description	Binary reset value	Additional notes
PCR_DATA[0]	MASK	1'b0	Same position for both Torino and Bergamo/Pavia
PCR_DATA[1]	CAL_EN	1'b0	Same position for both Torino and Bergamo/Pavia
PCR_DATA[2]	FAST_EN	1'b0	-
PCR_DATA[3]	SEL_C2F	1'b0	-
PCR_DATA[4]	SEL_C4F	1'b1	-
PCR_DATA[7:5]	unconnected	-	-



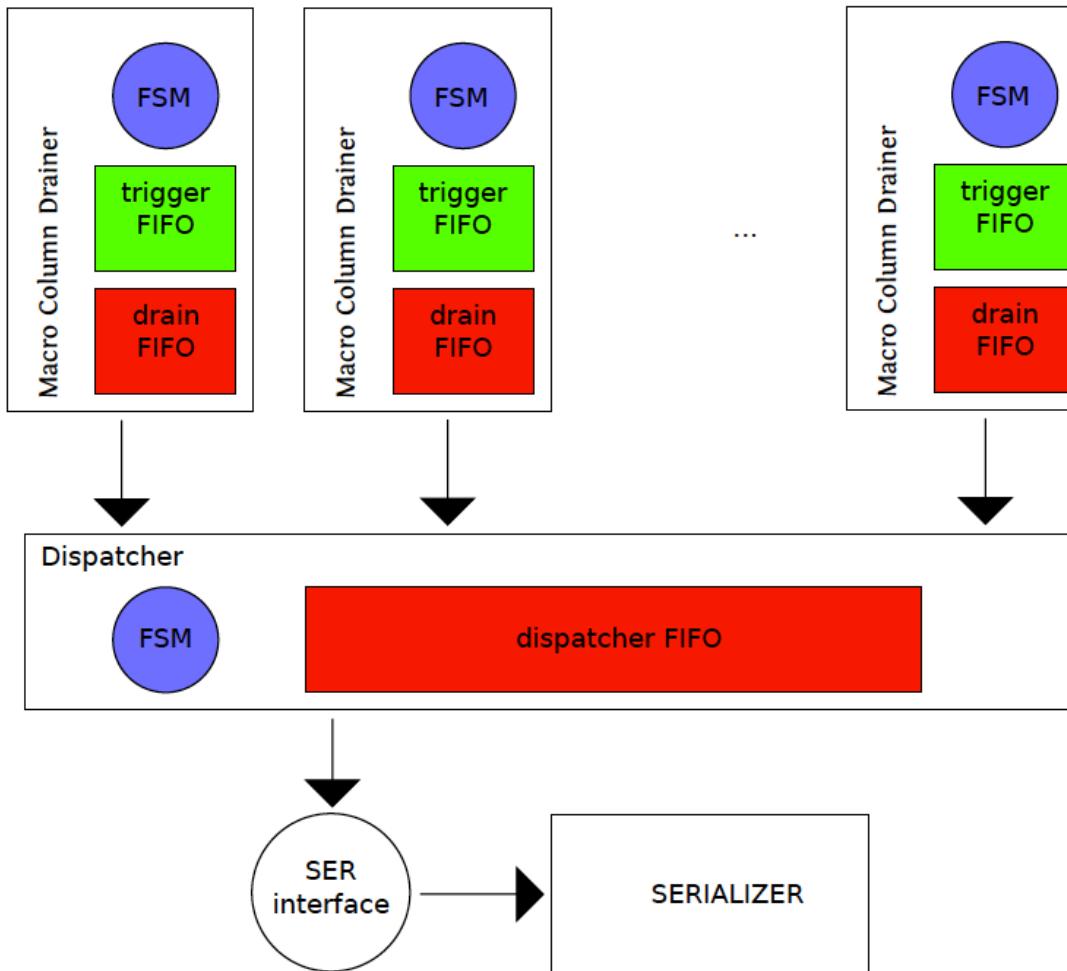
## On-chip monitoring multiplexing



[4:0]CFG_MON_MUX decimal value	RTL name	Description
0	VREF	Bandgap reference voltage
1	VRIF_KRUM_BGPV	Bergamo/Pavia Krummenacher feedback reference voltage
2	CAL_HI	Common calibration level
3	CAL_LO	Common calibration level
4	VTH	Torino global threshold
5	VBL	Torino baseline voltage
6	VREF_KRUM_TO	Torino Krummenacher feedback reference voltage
7	-	-
8	-	-
9	-	-
10	-	-
11	-	-
12	-	-
13	-	-
14	-	-
15	-	-
16	IREF	Reference current for DACs
17	IBIASP1	Torino IBIASP1
18	IBIASP2	Torino IBIASP2
19	IBIAS_DISC	Torino discriminator bias current
20	IBIAS_SF	Torino IBIAS_SF
21	ICTRL_TOT	Torino delay-line current starving
22	IFEED	Torino Krummenacher feedback current
23	IGDAC	Bergamo/Pavia global-DAC current
24	ILDAC	Bergamo/Pavia local-DAC current
25	IFC_BIAS	Bergamo/Pavia Krummenacher feedback current
26	IKRUM	Bergamo/Pavia Krummenacher bias current
27	IPA_IN_BIAS	Bergamo/Pavia CSA bias current
28	-	-



# EoC: Readout



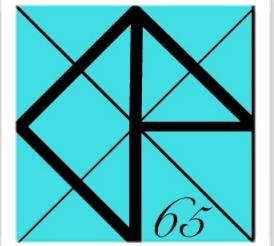
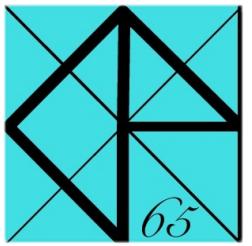
Data to EoC  
46bit + 4bit (PR add)  
= 50bit

the column drain all the data relative to the timestamp of the triggered event

Data to dispatcher:  
 $56 + 4 + 4 = 64$  bits

8b10b ==> 80 bits

TimeStamp(10b)+PRaddress(4b-col,4b-row)+BinaryMap(16b)+6\*ToT (5b) = 64b

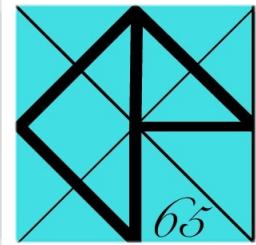
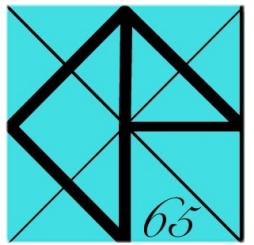


# PR Architecture :summary

- **Inefficiencies (digital) @3GHz/cm<sup>2</sup> ; 12.8 us trigger latency:**
  - particle loss < 0.2%
  - single pixel loss = 0; 5-bit ToT ~0,4%
  - aliasing prob (ghosts) < 0,03%
- **Inefficiency (analog)**
  - depends on dead time : 0.7% (Fast mode, Low dead-time)
- **Digital Region functioning modes:**
  - **TriggerLess / Triggered / Debug**
  - **BinaryOnly / 5-bit-Tot**
  - High / Low deadtime (for Slow or Fast digitisation modes)

PR-packet :

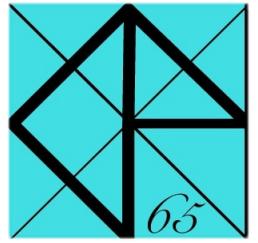
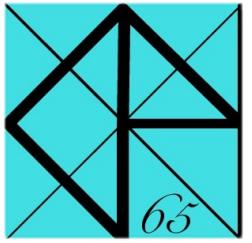
Data-out : (PR-col)-(timestamp)-(PRrow)-HitMap-6ToT



# I/O interface

Name	Direction	Description
CLK_BX±	input	40 MHz BX clock
RSTN±	input	global asynchronous reset (active low)
TRIGGER±	input	trigger
CLK_SER±	input	$\geq 320$ MHz serializer clock
SDO±	output	output serial data stream
TESTP±	input	charge-injection control signal
SCAN_MODE	input	global scan test-mode enable (CMOS)
SCLK±	input	13.33 MHz SPI configuration clock
SSN_or_SCAN_EN±	input	multiplexed SPI slave-select/shift-enable
MOSI_or_SCAN_IN±	input	multiplexed SPI input configuration data/scan-in
MISO_or_SCAN_OUT±	output	multiplexed SPI output configuration data/scan-out / Fast Or
VREF	inout	monitored bandgap reference voltage
IDAC	inout	monitored multiplexed global DACs reference current
VADC	inout	monitored ADC input voltage
VTH_ADC	inout	monitored ADC reference voltage
VTH_BYPASS	inout	bypass point in case ADC extra-noise filtering is required

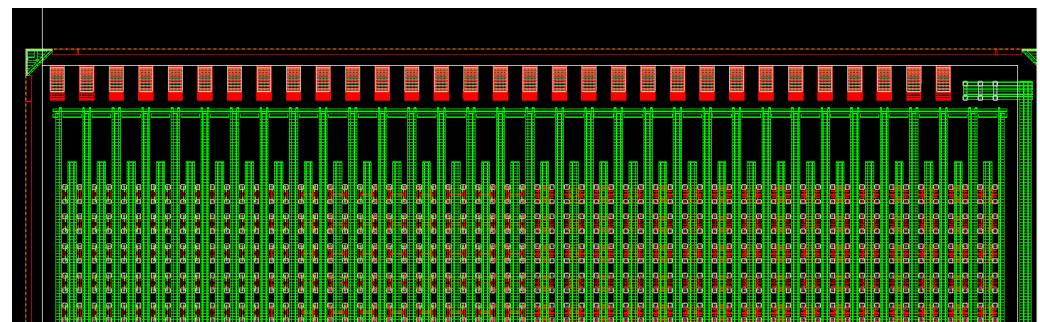
- dedicated **test pads** for monitoring purposes
- **320 Mb/s readout bandwidth** enough to comply with nominal HL-LHC hit rates re-scaled on a small  $64 \times 64$  pixel array

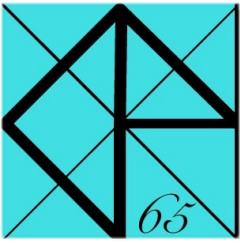


# Top PADs

PAD ROW	PAD number from left	PAD Name
Top Digital	1	VDDIO
Top Digital	2	VSSIO
Top Digital	3	VDD
Top Digital	4	VDD
Top Digital	5	VDD
Top Digital	6	VSS
Top Digital	7	VSS
Top Digital	8	VSS
Top Digital	9	VDD
Top Digital	10	VDD
Top Digital	11	VDD
Top Digital	12	VSS
Top Digital	13	VSS
Top Digital	14	VSS
Top Digital	15	VDD
Top Digital	16	VDD
Top Digital	17	VDD
Top Digital	18	VSS
Top Digital	19	VSS
Top Digital	20	VSS
Top Digital	21	VDD
Top Digital	22	VDD
Top Digital	23	VDD
Top Digital	24	VSS
Top Digital	25	VSS
Top Digital	26	VDD
Top Digital	27	VDD
Top Digital	28	VSS
Top Digital	29	VSS
Top Digital	30	VDDIO
Top Digital	31	VSSIO

THESE PADs are not essential.  
They are test point to measure the  
voltage drop of VDD and VSS if  
unconnected. If connected are  
providing a more robust VDD and VSS



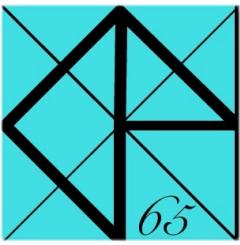


# Bottom PADs

PAD ROW	PAD number from left	PAD Name	Purpose
Bottom Analog	1	AVSSIO	PAD POWER
Bottom Analog	2	AVDDIO	PAD POWER
Bottom Analog	3	AVDD	CHIP POWER
Bottom Analog	4	AVDD	CHIP POWER
Bottom Analog	5	AVDD	CHIP POWER
Bottom Analog	6	AVSS	CHIP POWER
Bottom Analog	7	AVSS	CHIP POWER
Bottom Analog	8	AVSS	CHIP POWER
Bottom Analog	9	AVDD	CHIP POWER
Bottom Analog	10	AVDD	CHIP POWER
Bottom Analog	11	AVDD	CHIP POWER
Bottom Analog	12	AVSS	CHIP POWER
Bottom Analog	13	AVSS	CHIP POWER
Bottom Analog	14	AVSS	CHIP POWER
Bottom Analog	15	AVDD	CHIP POWER
Bottom Analog	16	AVDD	CHIP POWER
Bottom Analog	17	AVDD	CHIP POWER
Bottom Analog	18	AVSS	CHIP POWER
Bottom Analog	19	AVSS	CHIP POWER
Bottom Analog	20	AVSS	CHIP POWER
Bottom Analog	21	AVDD	CHIP POWER
Bottom Analog	22	AVDD	CHIP POWER
Bottom Analog	23	AVSS	CHIP POWER
Bottom Analog	24	AVSS	CHIP POWER
Bottom Analog	25	VREF_MON	Monitoring Band GAP voltage
Bottom Analog	26	VADC_MON	Monitoring V-ADC
Bottom Analog	27	IDAC_MON	Connection to Ext-RES
Bottom Analog	28	VTH_MON	Monitored ADC REF voltage
Bottom Analog	29	VTH_BYPASS	Noise-Filter for ADC
Bottom Analog	30	AVDD	CHIP POWER
Bottom Analog	31	AVDD_IO	PAD POWER
Bottom Analog	32	AVSS_IO	PAD POWER
Bottom Analog	33	GND_SENSORS	Silicon Sensor Ground

PAD ROW	PAD number from left	PAD Name	Purpose
Bottom Digital	1	VDDIO	PAD POWER
Bottom Digital	2	VSSIO	PAD POWER
Bottom Digital	3	RSTN_P	CHIP RESET
Bottom Digital	4	RSTN_N	CHIPI RESET
Bottom Digital	5	VDD	CHIP POWER
Bottom Digital	6	VDD	CHIP POWER
Bottom Digital	7	VSS	CHIP POWER
Bottom Digital	8	VSS	CHIP POWER
Bottom Digital	9	SCLK_P	SPI 13,33 MHz CLKC
Bottom Digital	10	SCLK_N	SPI 13,33 MHz CLKC
Bottom Digital	11	MOSI or SCAN_IN_P	SPI Master Out serial IN
Bottom Digital	12	MOSI or SCAN_IN_N	SPI Master Out serial IN
Bottom Digital	13	MISO_or_SCAN_OUT or FASTOR_P	SPI Master IN serial Out
Bottom Digital	14	MISO_or_SCAN_OUT or FASTOR_N	SPI Master IN serial Out
Bottom Digital	15	SSN_OR_SCAN_EN_P	SPI Slave Select
Bottom Digital	16	SSN_OR_SCAN_EN_N	SPI Slave Select
Bottom Digital	17	TESTP_P	TEST Pulse
Bottom Digital	18	TESTP_N	TEST Pulse
Bottom Digital	19	CLK_BX_P	40 MHz Clock
Bottom Digital	20	CLK_BX_N	40 MHz Clock
Bottom Digital	21	SDO_P	DATA Serial OUT
Bottom Digital	22	SDO_N	DATA Serial OUT
Bottom Digital	23	CLK_SER_P	Serial 320 MHz CLOCK
Bottom Digital	24	CLK_SER_N	Serial 320 MHz CLOCK
Bottom Digital	25	TRIGGER_P	Trigger
Bottom Digital	26	TRIGGER_N	Trigger
Bottom Digital	27	VDD	CHIP POWER
Bottom Digital	28	VSS	CHIP POWER
Bottom Digital	29	SCAN_MODE	Scan MODE
Bottom Digital	30	VSS	CHIP POWER
Bottom Digital	31	VDD	CHIP POWER
Bottom Digital	32	VDDIO	PAD POWER
Bottom Digital	33	VSSIO	PAD POWER

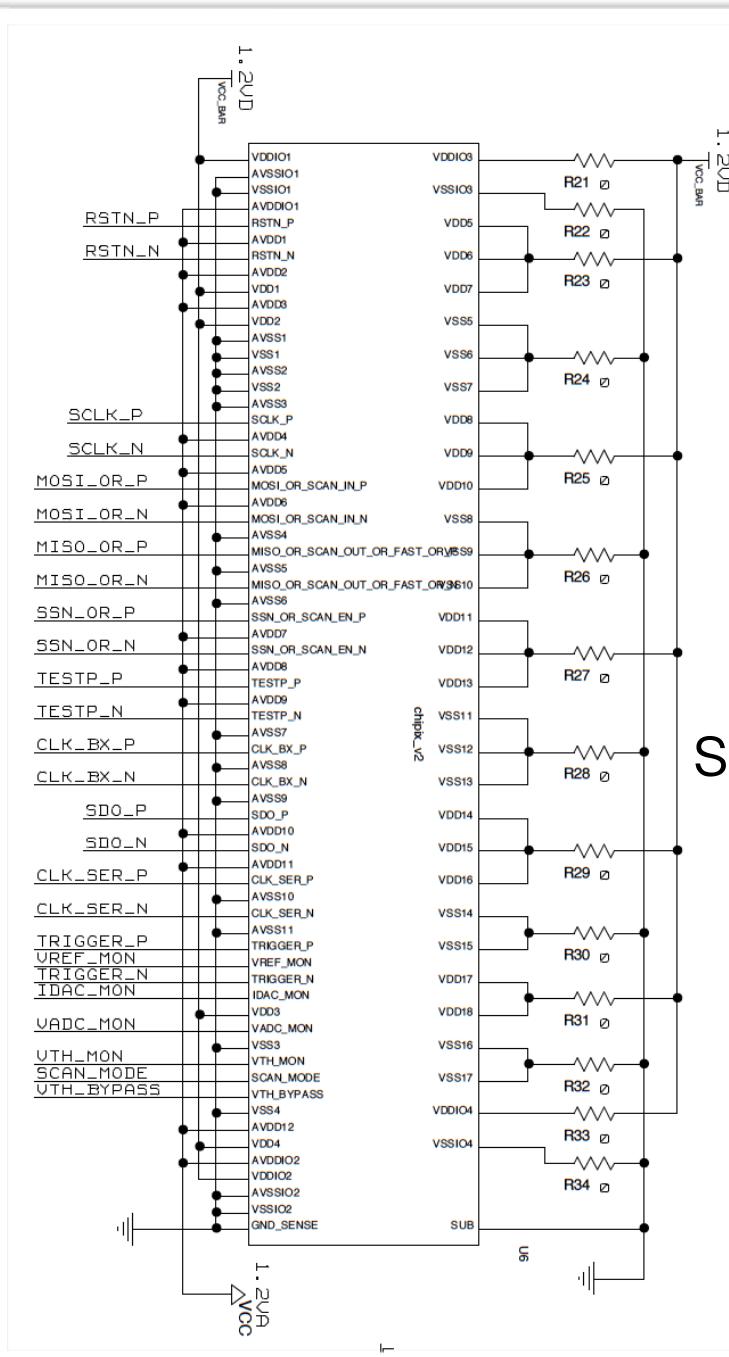




# Check PCB connections

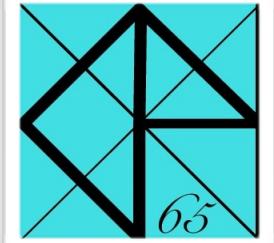
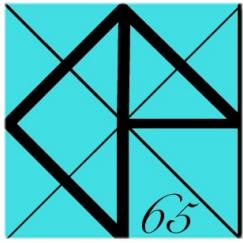


PAD ROW	PAD number from left	PAD Name
Bottom Analog	1	AVSSIO
Bottom Analog	2	AVDDIO
Bottom Analog	3	AVDD
Bottom Analog	4	AVDD
Bottom Analog	5	AVDD
Bottom Analog	6	AVSS
Bottom Analog	7	AVSS
Bottom Analog	8	AVSS
Bottom Analog	9	AVDD
Bottom Analog	10	AVDD
Bottom Analog	11	AVDD
Bottom Analog	12	AVSS
Bottom Analog	13	AVSS
Bottom Analog	14	AVSS
Bottom Analog	15	AVDD
Bottom Analog	16	AVDD
Bottom Analog	17	AVDD
Bottom Analog	18	AVSS
Bottom Analog	19	AVSS
Bottom Analog	20	AVSS
Bottom Analog	21	AVDD
Bottom Analog	22	AVDD
Bottom Analog	23	AVSS
Bottom Analog	24	AVSS
Bottom Analog	25	VREF_MON
Bottom Analog	26	VADC_MON
Bottom Analog	27	IDAC_MON
Bottom Analog	28	VTH_MON
Bottom Analog	29	VTH_BYPASS
Bottom Analog	30	AVDD
Bottom Analog	31	AVDD_IO
Bottom Analog	32	AVSS_IO
Bottom Analog	33	GND_SENSORS



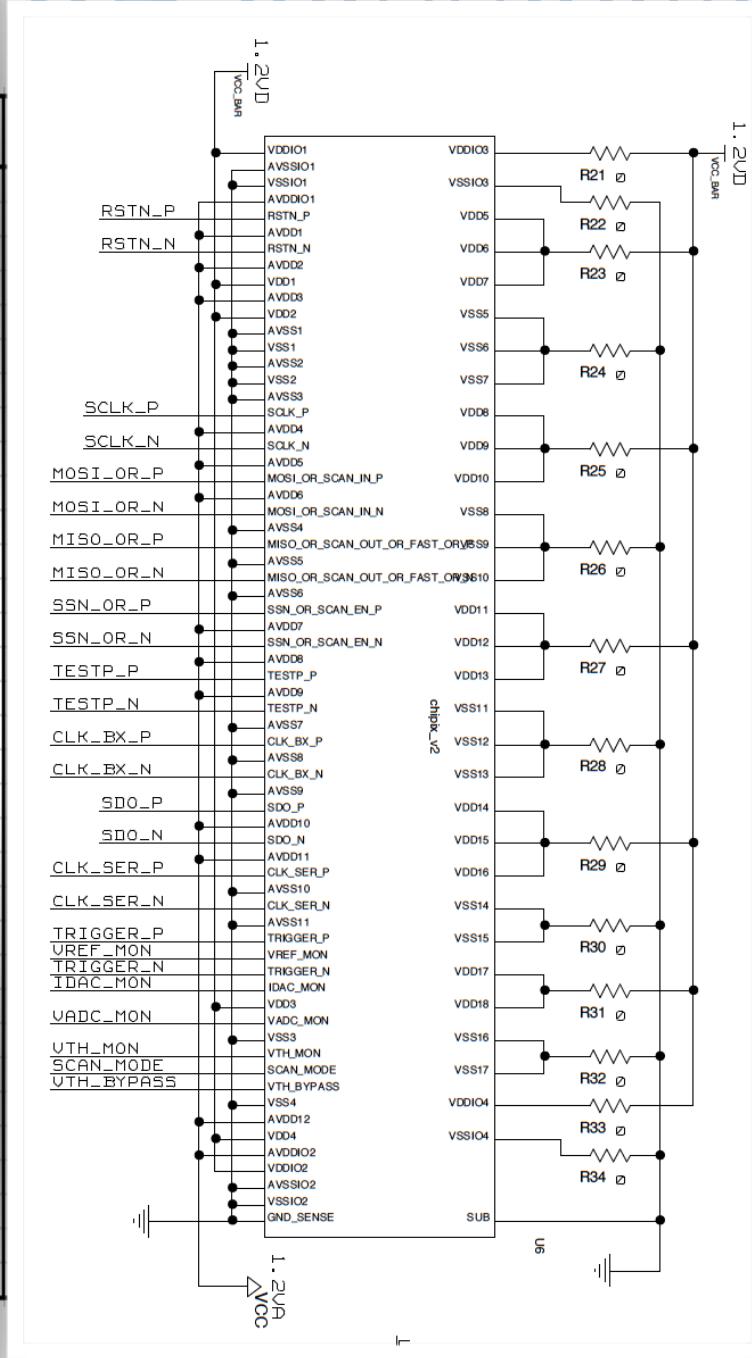
- VADC\_MON
- IDAC\_MON

seems swapped



# Check PCB connections

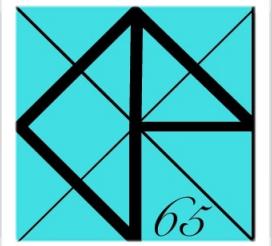
PAD ROW	PAD number from left	PAD Name
Bottom Digital	1	VDDIO
Bottom Digital	2	VSSIO
Bottom Digital	3	RSTN_P
Bottom Digital	4	RSTN_N
Bottom Digital	5	VDD
Bottom Digital	6	VDD
Bottom Digital	7	VSS
Bottom Digital	8	VSS
Bottom Digital	9	SCLK_P
Bottom Digital	10	SCLK_N
Bottom Digital	11	MOSI or SCAN_IN_P
Bottom Digital	12	MOSI or SCAN_IN_N
Bottom Digital	13	MISO_or_SCAN_OUT or FASTOR_P
Bottom Digital	14	MISO_or_SCAN_OUT or FASTOR_N
Bottom Digital	15	SSN_OR_SCAN_EN_P
Bottom Digital	16	SSN_OR_SCAN_EN_N
Bottom Digital	17	TESTP_P
Bottom Digital	18	TESTP_N
Bottom Digital	19	CLK_BX_P
Bottom Digital	20	CLK_BX_N
Bottom Digital	21	SDO_P
Bottom Digital	22	SDO_N
Bottom Digital	23	CLK_SER_P
Bottom Digital	24	CLK_SER_N
Bottom Digital	25	TRIGGER_P
Bottom Digital	26	TRIGGER_N
Bottom Digital	27	VDD
Bottom Digital	28	VSS
Bottom Digital	29	SCAN_MODE
Bottom Digital	30	VSS
Bottom Digital	31	VDD
Bottom Digital	32	VDDIO
Bottom Digital	33	VSSIO



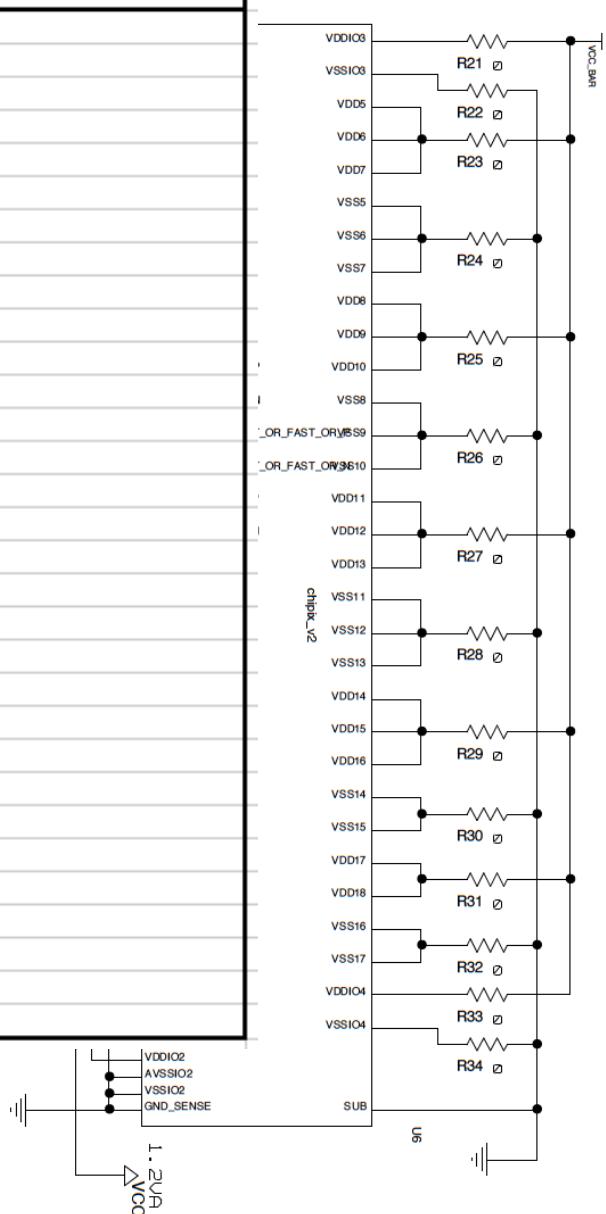
Digital  
Connection  
All Right



# Check PCB connections



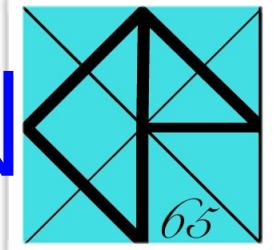
PAD ROW	PAD number from left	PAD Name
Top Digital	1	VDDIO
Top Digital	2	VSSIO
Top Digital	3	VDD
Top Digital	4	VDD
Top Digital	5	VDD
Top Digital	6	VSS
Top Digital	7	VSS
Top Digital	8	VSS
Top Digital	9	VDD
Top Digital	10	VDD
Top Digital	11	VDD
Top Digital	12	VSS
Top Digital	13	VSS
Top Digital	14	VSS
Top Digital	15	VDD
Top Digital	16	VDD
Top Digital	17	VDD
Top Digital	18	VSS
Top Digital	19	VSS
Top Digital	20	VSS
Top Digital	21	VDD
Top Digital	22	VDD
Top Digital	23	VDD
Top Digital	24	VSS
Top Digital	25	VSS
Top Digital	26	VDD
Top Digital	27	VDD
Top Digital	28	VSS
Top Digital	29	VSS
Top Digital	30	VDDIO
Top Digital	31	VSSIO



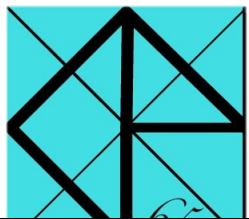
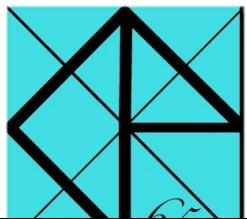
# Digital Connection All Right



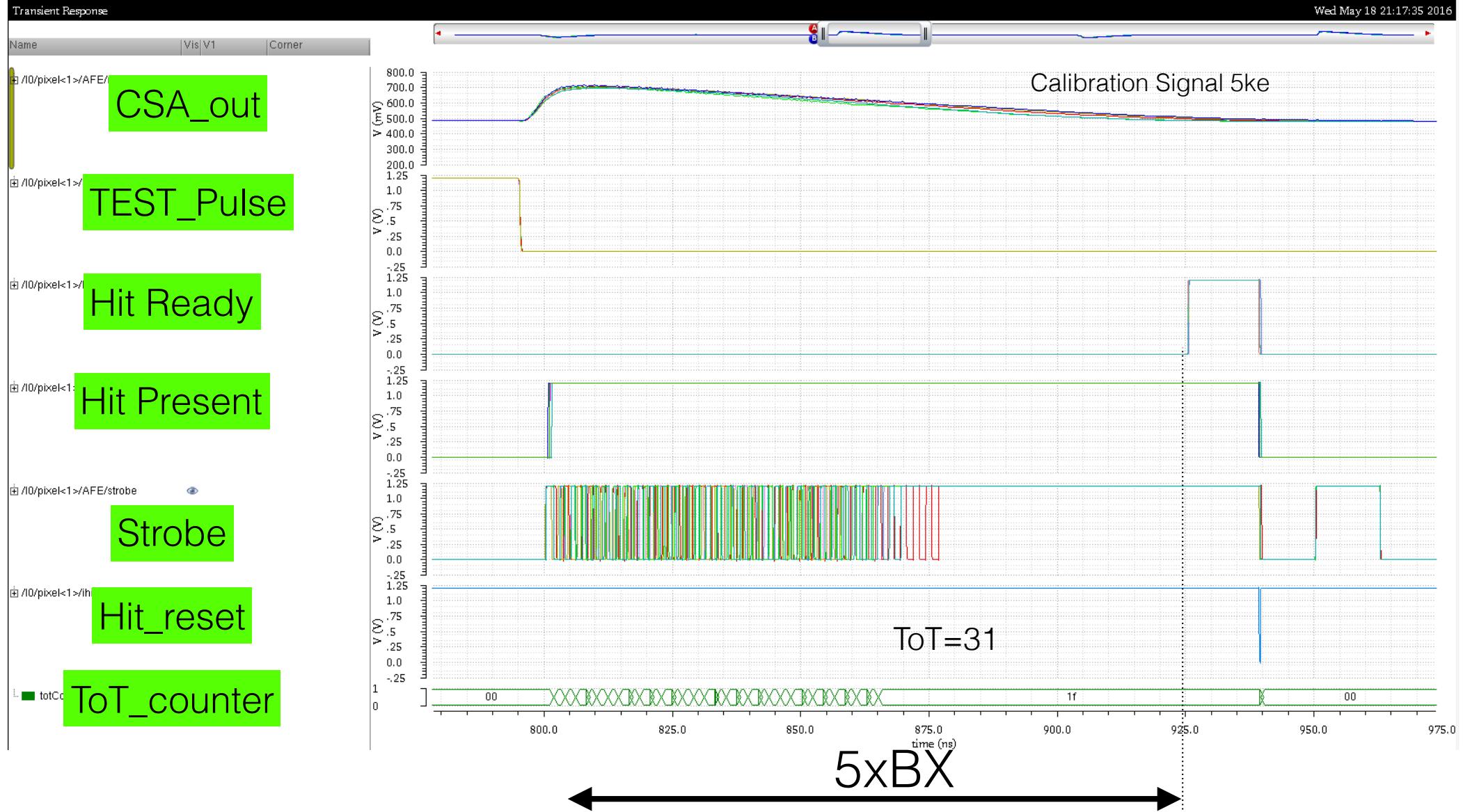
# VMON and IDAC-MON



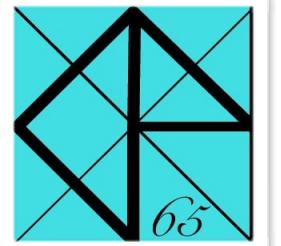
Pixel



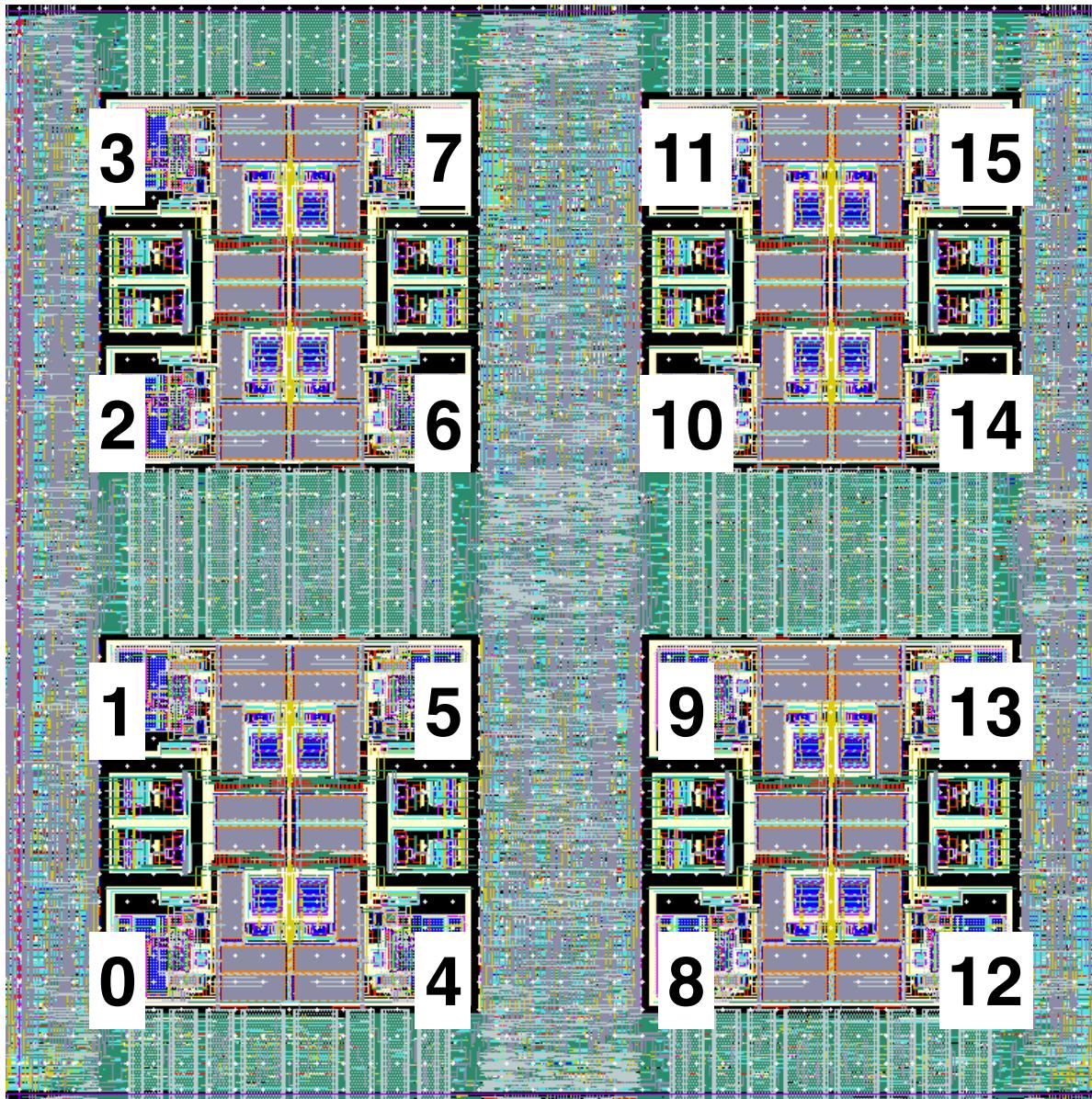
# PR: Hit Logic

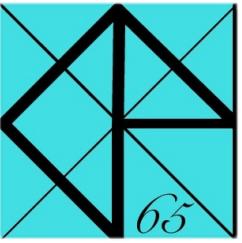


# Pixel Region



# Pixel numbering

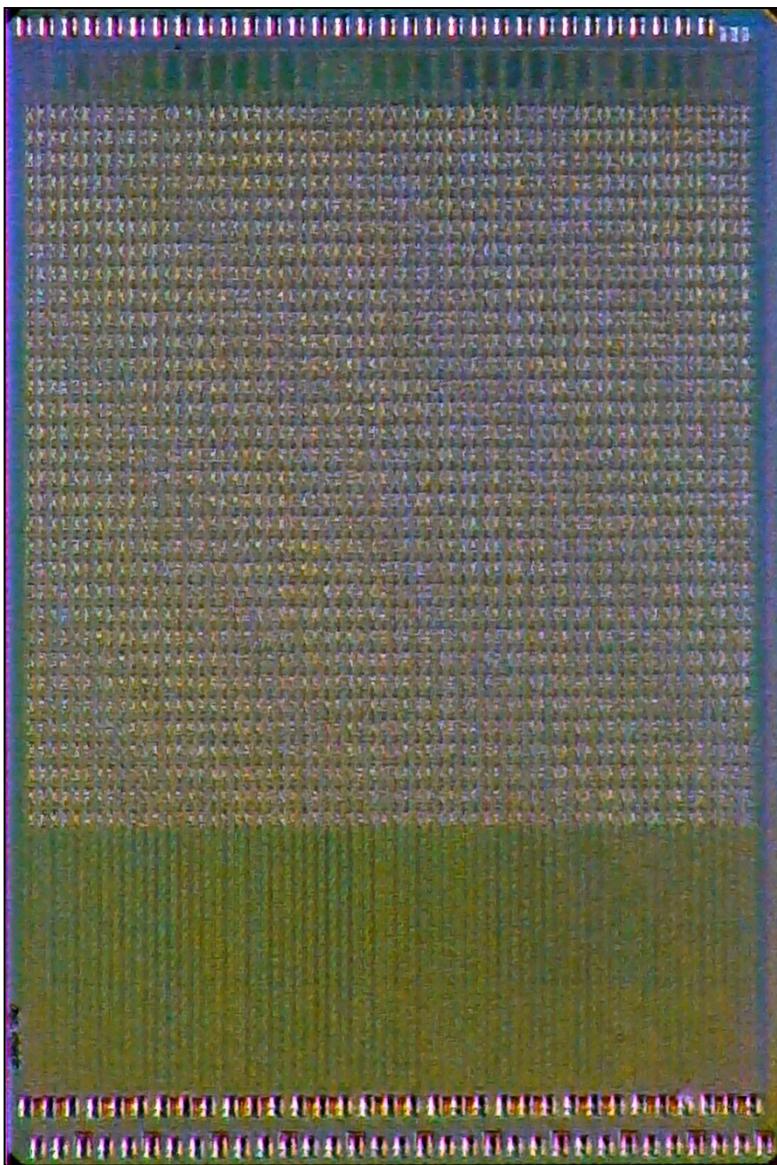
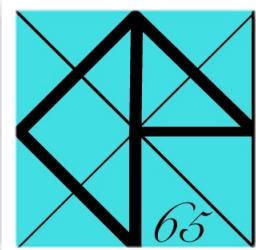
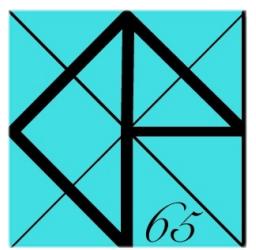




# Data format



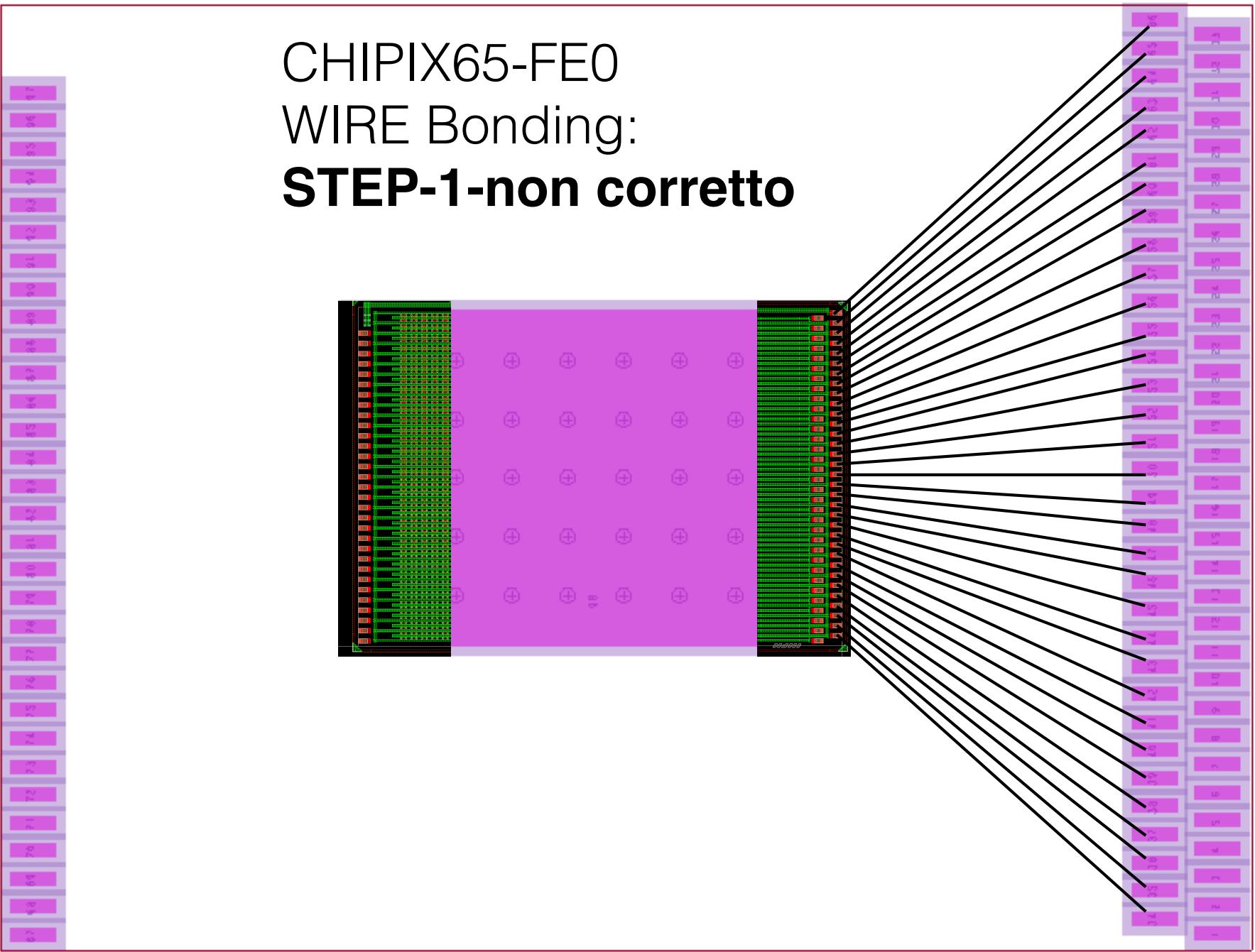
- Pixel region memory buffer
  - 10b (time-stamp) + 16b (hit-map) + 6\*5b (ToT) = 56b
- Pixel region-readout to EOC
  - 4b (PR addr) + 16b (hit-map) + 6\*5b (ToT) = 50b
- EOC buffer
  - 10b (timestamp) + 4b (PR add) + 16b (hit-map) + 6\*5 (ToT) = 60b
- Dispatcher
  - 10b (timestamp) + 4b (PR add) + 4b (PixCol-add) + 16b (hit-map) + 6\*5 (ToT) = 64b
  - same as EOC buffer
- Serialiser input
  - the 64b of Dispatcher become 80b with the 8b10b encoder
  - encoding is done with 16b words input ==> 20b words output
  - the data of the Serialiser are sent with 20b packets



# CHIPIX65-FE0

## WIRE Bonding:

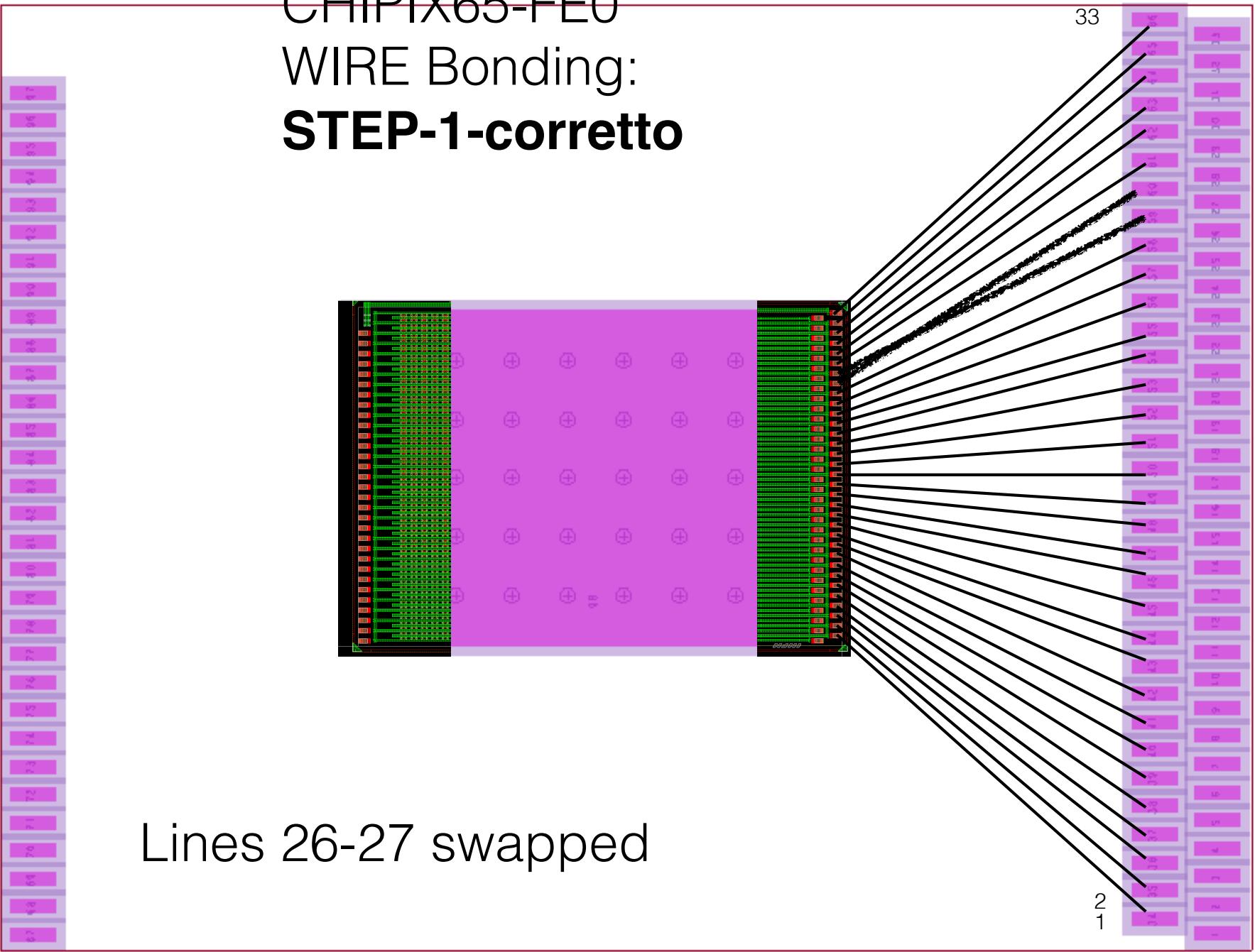
### **STEP-1-non corretto**



# CHIPIX65-FE0

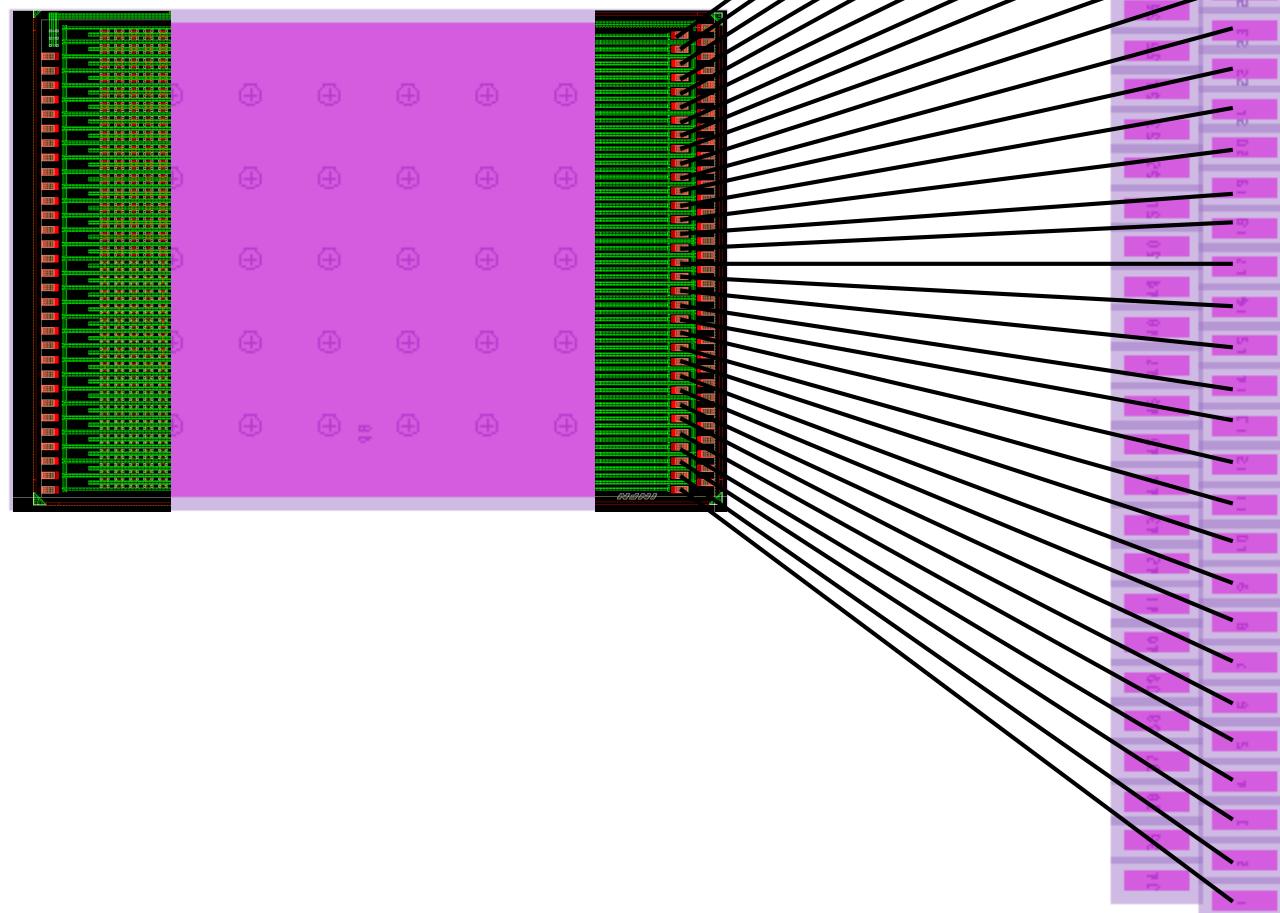
## WIRE Bonding:

### STEP-1-corretto



# CHIPIX65-FE0

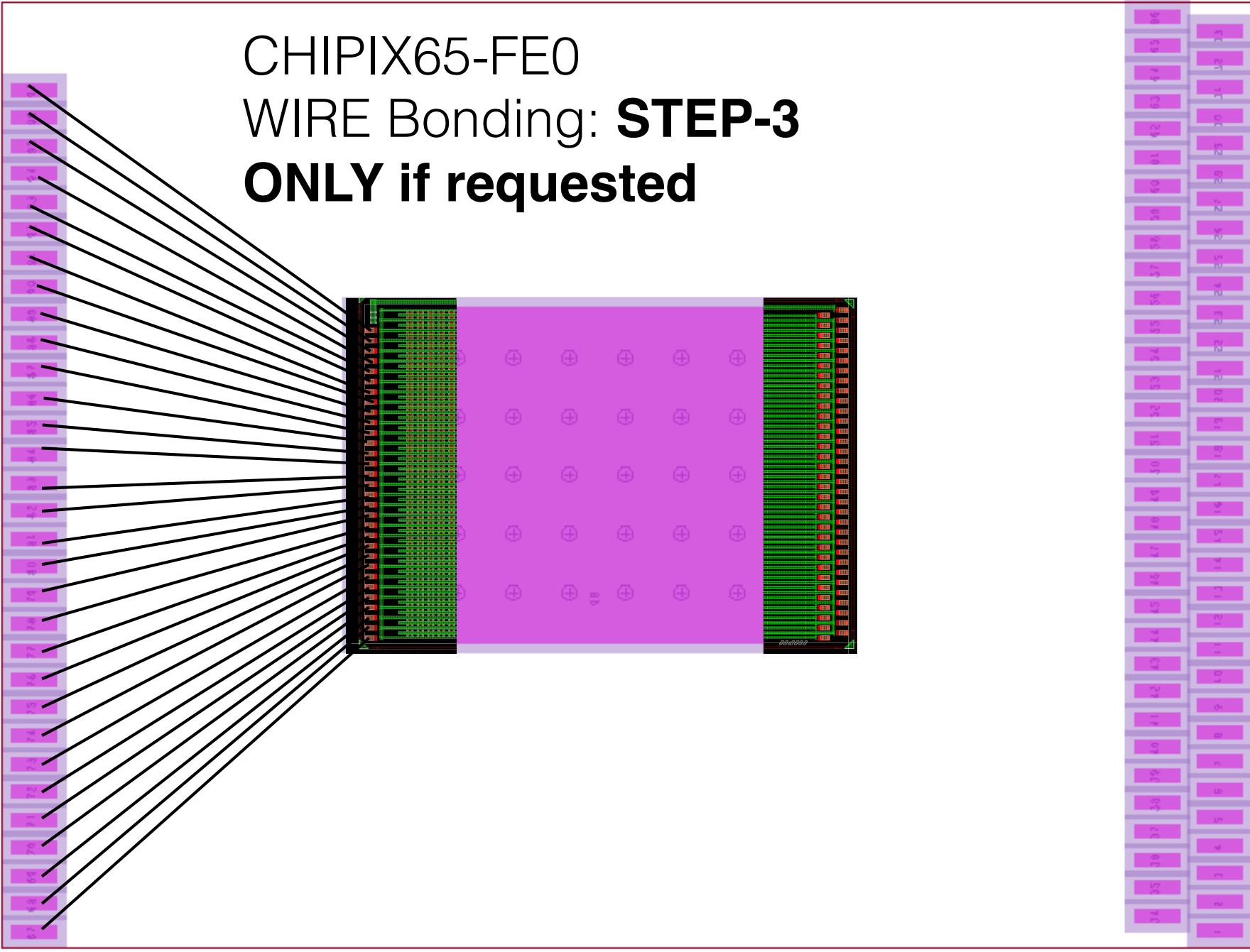
## WIRE Bonding: **STEP-2**

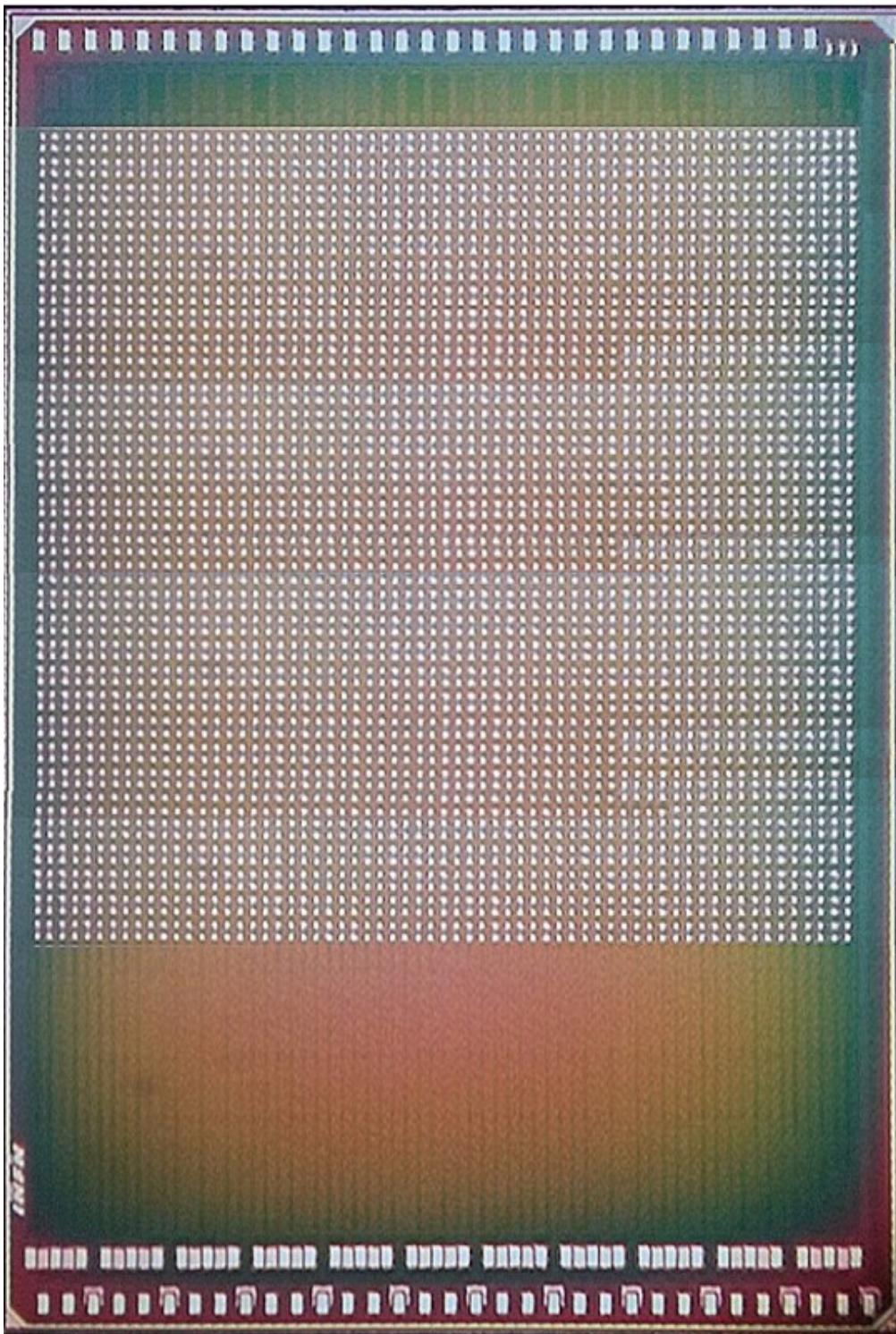


# CHIPIX65-FE0

## WIRE Bonding: **STEP-3**

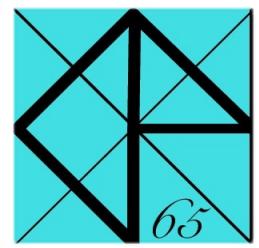
### **ONLY if requested**



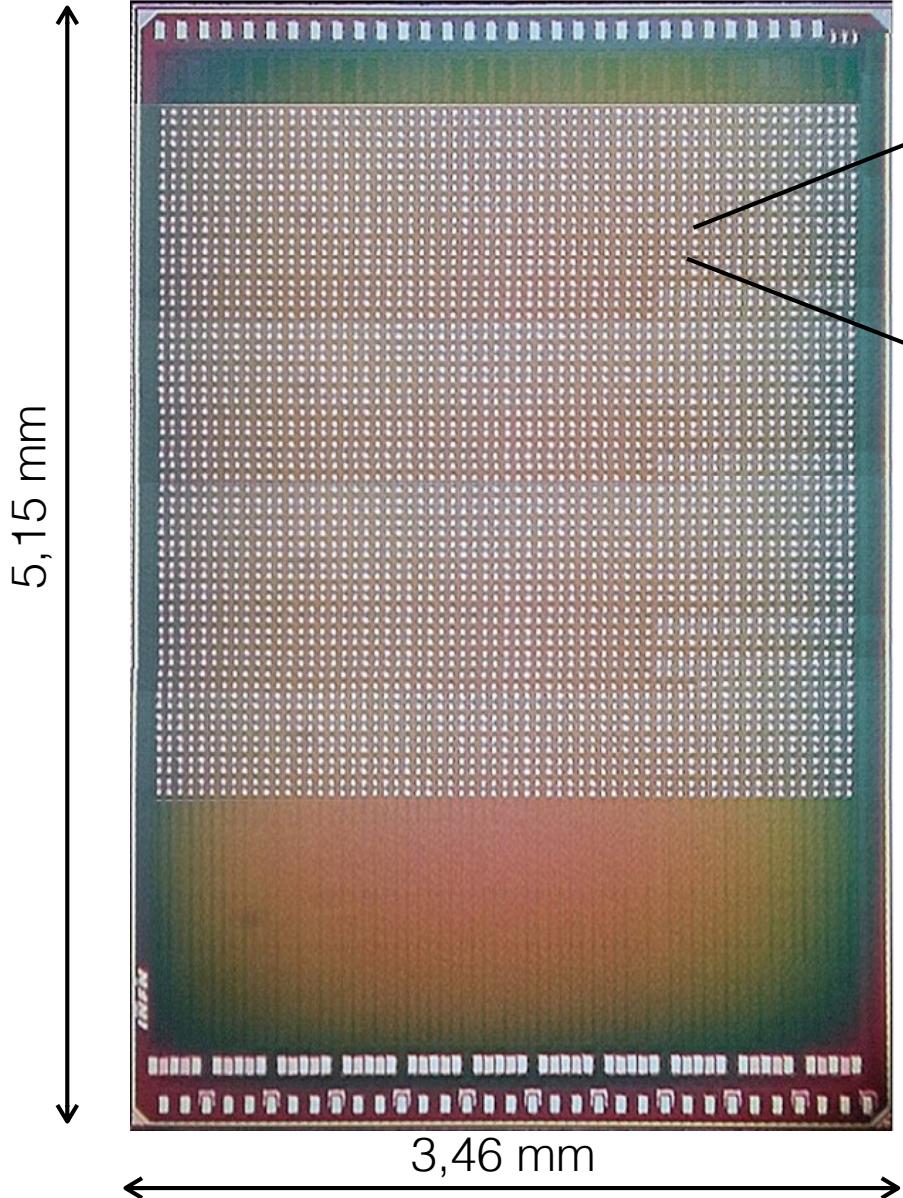




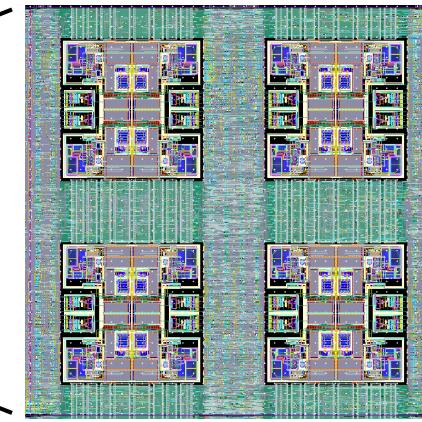
# CHIPIX65 demonstrator



CHIPIX65: 2013 CALL project INFN - CSN5  
Web-site: <http://chipix65.to.infn.it>



(2x2) Analog Islands  
on (4x4) pixel region digital architecture



arrived on  
26-Sept-2016

**64x64 pixel matrix - 50x50  $\mu\text{m}^2$**

HL\_HLC flux rates: 3 GHz/cm<sup>2</sup>  
Trigger latency : 12,5 us  
Low power consumption  
5-bit ToT signal digitisation  
In-time threshold <1200 e-  
Noise ~100e- @50fF input capacitance

VFE & IP-block developed in RD53

~3M of digital standard cells

INFN institutes: To, Ba, Le, Mi, Pd, Pg, Pi, Pv