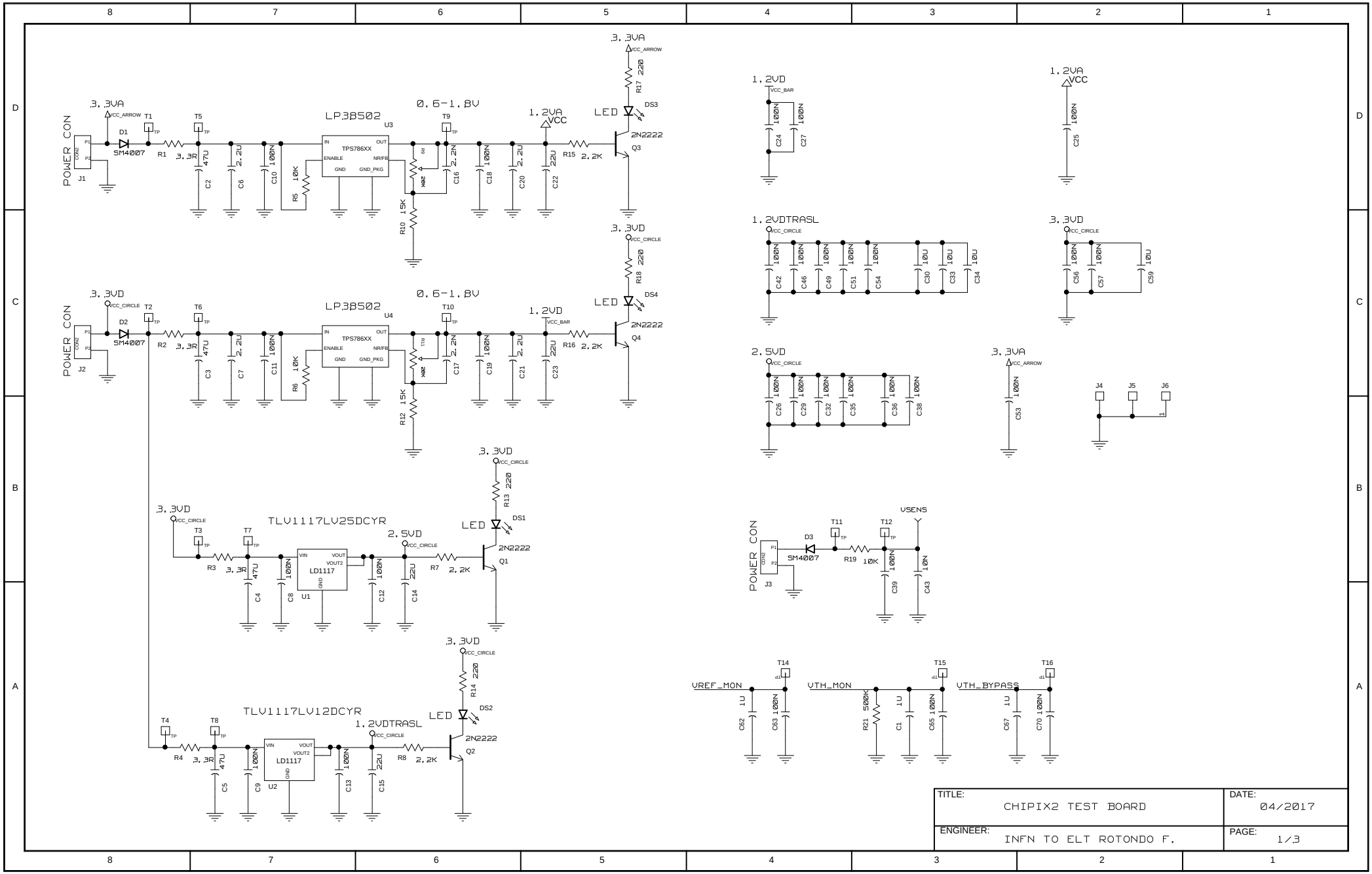

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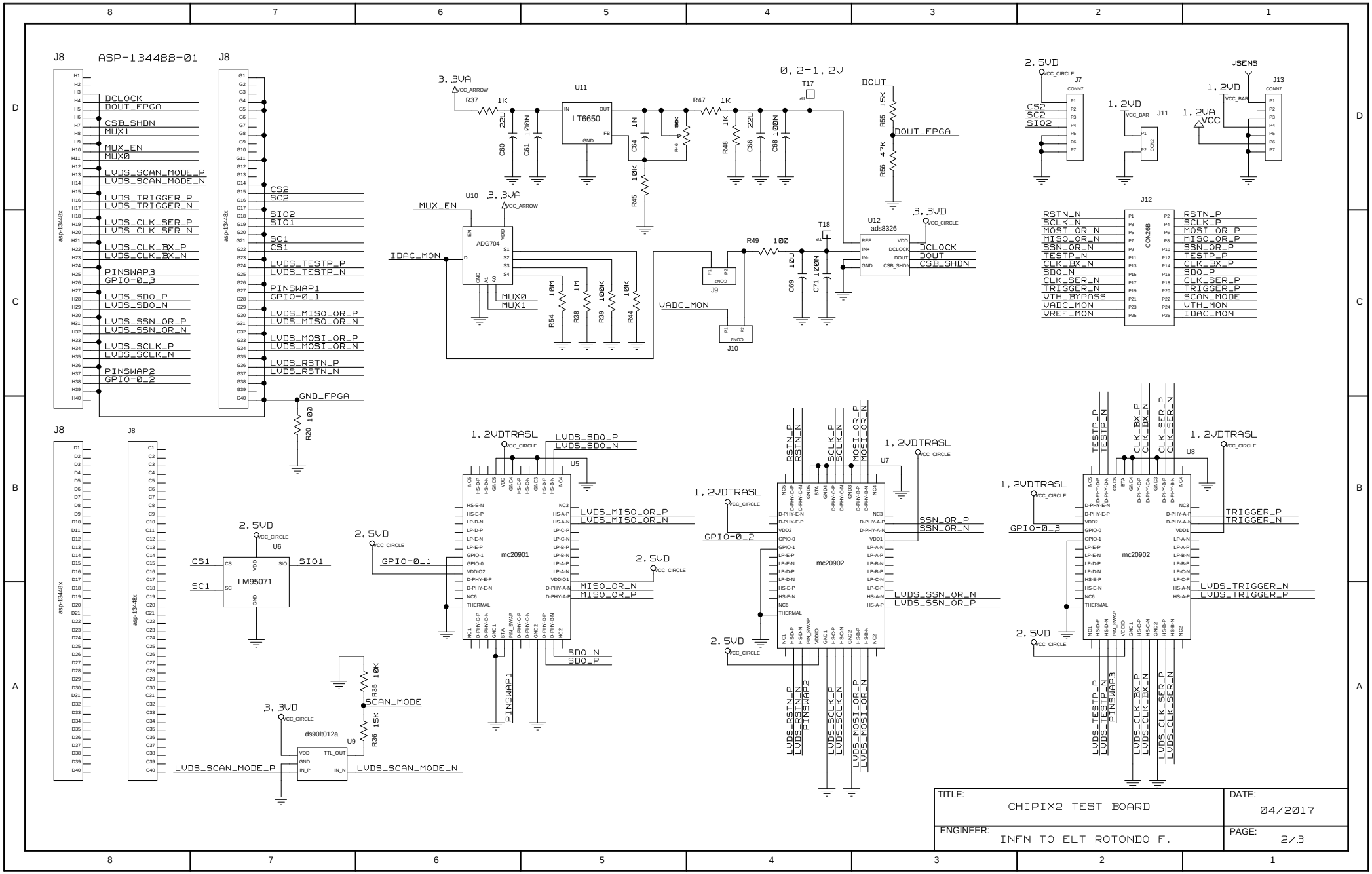
J8
ASP-134488-01
DCLOCK
DOUT_FPGA
CSB_SHDN
MUX1
MUX_EN
MUX0
LVDS_SCAN_MODE_P
LVDS_SCAN_MODE_N
LVDS_TRIGGER_P
LVDS_TRIGGER_N
LVDS_CLK_SER_P
LVDS_CLK_SER_N
LVDS_CLK_BX_P
LVDS_CLK_BX_N
PINSWAP3
GPIO-0_3
LVDS_SDO_P
LVDS_SDO_N
LVDS_SSN_OR_P
LVDS_SSN_OR_N
LVDS_SCLK_P
LVDS_SCLK_N
PINSWAP2
GPIO-0_2
CS2
SC2
SIO2
SIO1
SC1
CS1
LVDS_TESTP_P
LVDS_TESTP_N
PINSWAP1
GPIO-0_1
LVDS_MISO_OR_P
LVDS_MISO_OR_N
LVDS_MOSI_OR_P
LVDS_MOSI_OR_N
LVDS_RSTN_P
LVDS_RSTN_N
GND_FPGA
R20 100
3.3VA
U11
LT6650
R37 1K
C60 22U
C61 100N
C64 1N
R45 10K
R46 50K
R47 1K
R48 1K
C66 22U
C68 100N
0.2-1.2V
T17
DOUT
R55 15K
R56 47K
DOUT_FPGA
U10
ADG704
IDAC_MON
R54 10M
R38 1M
R39 100K
R44 10K
MUX0
MUX1
J9
VADC_MON
J10
R49 100
C69 10U
C71 100N
T18
U12
ads8326
REF
IN+
IN-
GND
VDD
DCLOCK
DOUT
CSB_SHDN
3.3VD
2.5VD
J7
CONN7
1.2VD
J11
CON26
1.2VA
VCC
VSENS
J13
J12
CON26B
RSTN_N
SCLK_N
MOSI_OR_N
MISO_OR_N
SSN_OR_N
TESTP_N
CLK_BX_N
SDO_N
CLK_SER_N
TRIGGER_N
VTH_BYPASS
VADC_MON
VREF_MON
RSTN_P
SCLK_P
MOSI_OR_P
MISO_OR_P
SSN_OR_P
TESTP_P
CLK_BX_P
SDO_P
CLK_SER_P
TRIGGER_P
SCAN_MODE
VTH_MON
IDAC_MON
1.2VDTRASL
U5
mc20901
LVDS_SDO_P
LVDS_SDO_N
LVDS_MISO_OR_P
LVDS_MISO_OR_N
MISO_OR_N
MISO_OR_P
SDO_N
SDO_P
PINSWAP1
U6
LM95071
CS
SC
SIO
GND
GPIO-0_1
U7
mc20902
GPIO-0_2
SSN_OR_P
SSN_OR_N
LVDS_SSN_OR_N
LVDS_SSN_OR_P
LVDS_RSTN_P
LVDS_RSTN_N
PINSWAP2
LVDS_SCLK_P
LVDS_SCLK_N
LVDS_MOSI_OR_P
LVDS_MOSI_OR_N
U8
GPIO-0_3
TRIGGER_P
TRIGGER_N
LVDS_TRIGGER_N
LVDS_TRIGGER_P
LVDS_TESTP_P
LVDS_TESTP_N
PINSWAP3
LVDS_CLK_BX_P
LVDS_CLK_BX_N
LVDS_CLK_SER_P
LVDS_CLK_SER_N
R35 10K
R36 15K
SCAN_MODE
U9
ds90lt012a
VDD
GND
IN_P
TTL_OUT
IN_N
LVDS_SCAN_MODE_P
LVDS_SCAN_MODE_N
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