2023 Digital IC Design Homework 5

NAME	
Student ID	

Simulation Result

Functional simulation	Completed

```
VSIM 4> run -all
# ****************************************************************************
# **                        Simulation Start                                **
# ****************************************************************************
# ****************************************************************************
# **               Simulation completed successfully!                       **
# ****************************************************************************
# ** Note: $finish    : D:/Master shit life/111-2/dic2023/HWs/HW5/testfixture.v(149)
#    Time: 6370100 ns  Iteration: 1  Instance: /testfixture
# 1
```

Gate-level simulation	Completed

```
# WARNING: No extended dataflow license exists
VSIM 2> run -all
# ****************************************************************************
# **                        Simulation Start                                **
# ****************************************************************************
# ****************************************************************************
# **               Simulation completed successfully!                       **
# ****************************************************************************
# ** Note: $finish    : D:/Master shit life/111-2/dic2023/HWs/HW5/gate_sim/testfixtur
#    Time: 6370100 ns  Iteration: 1  Instance: /testfixture
# 1
# Break in Module testfixture at D:/Master shit life/111-2/dic2023/HWs/HW5/gate_sim/t

VSIM 3>
```

Ln: 149 Col: 0 | READ | Project : gate_hw5 | Now: 6,370,100 ns Delta: 1

沒做任何優化所以會跑蠻久的。

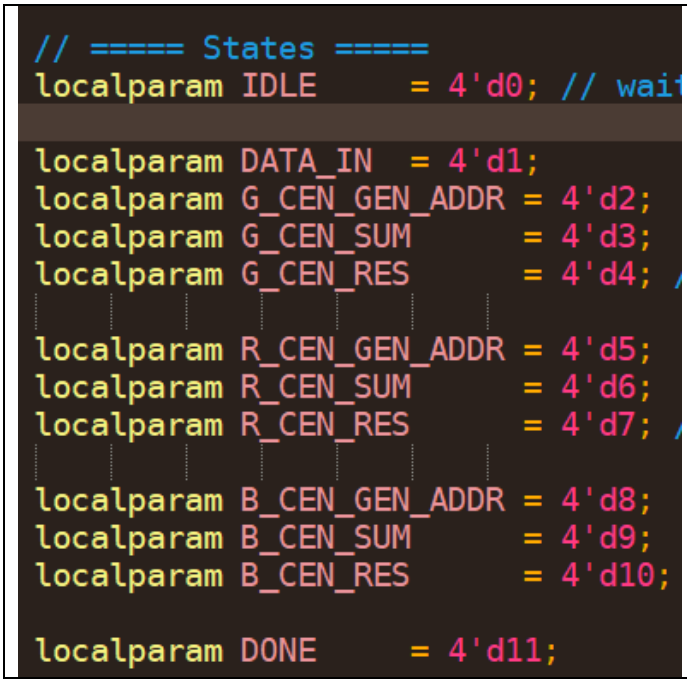
Evaluation Results

test1.png	25.29	test2.png	24.78
test3.png	29.13	test4.png	21.00
test5.png	21.98	test6.png	25.27

Description of your design

這次的題目也是需要對圖片矩陣進行處理，在狀態上面我主要有 4 個部分，IDLE 等待 in_en 的出現切到 DATA_IN 狀態開始讀值(Bayer filtered inputs)並放到對應的排列位置 (GRBG)，讀完輸入後開始依序 (G>R>B) 針對各個 channel 的 pixel 進行 bilinear interpolation.，在填補的過程中個別又有三種狀態(GEN_ADDR, SUM, RES)，GEN_ADDR 會根據 idx 去找出要拿來累加的 src_addr，如果要插值 G channel 在原本的紅色區塊就要依序算出上下左右的位置，同理差值 B/R channel 在原本紅/藍的區塊，接著就會進入累加 SUM state，RES state 主要是當 idx 取完所有的 src 後就會進入，透過取位移的 bits 來計算 divide by 2 或者 divided by 4。

最後所有的區塊都插值完就會進入 DONE state 把 done 拉高，完成插值。



```
// ===== States =====
localparam IDLE     = 4'd0; // wai

localparam DATA_IN  = 4'd1;
localparam G_CEN_GEN_ADDR = 4'd2;
localparam G_CEN_SUM      = 4'd3;
localparam G_CEN_RES      = 4'd4;

localparam R_CEN_GEN_ADDR = 4'd5;
localparam R_CEN_SUM      = 4'd6;
localparam R_CEN_RES      = 4'd7;

localparam B_CEN_GEN_ADDR = 4'd8;
localparam B_CEN_SUM      = 4'd9;
localparam B_CEN_RES      = 4'd10;

localparam DONE     = 4'd11;
```

Scoring = average PSNR of the six test images

*** PSNR of all interpolation results should meet at least the baseline.**