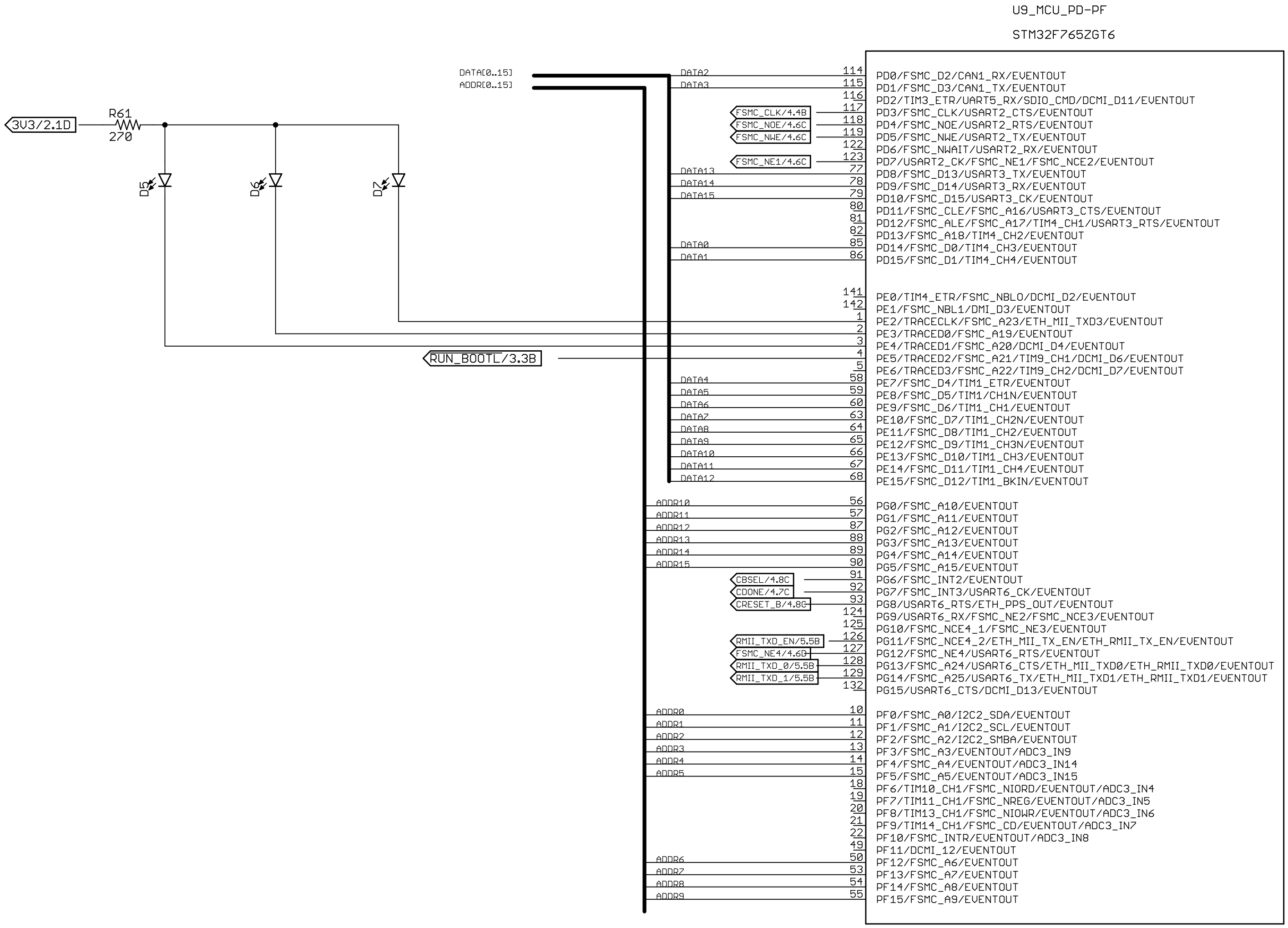

DESIGNED t.elliott	PREL.			
DRAWN	PROTO			
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	PROD			
UNLESS OTHERWISE SPECIFIED TOLERANCES DECIMAL .XX +/- 0.010 .XXX +/- 0.005 FRACTIONAL +/- 1/64 ANGULAR +/- 1/2 HOLE +/- .004 +/- .002 DIMENSIONS: INCHES	NEXT ASSY.	SYSTEM		
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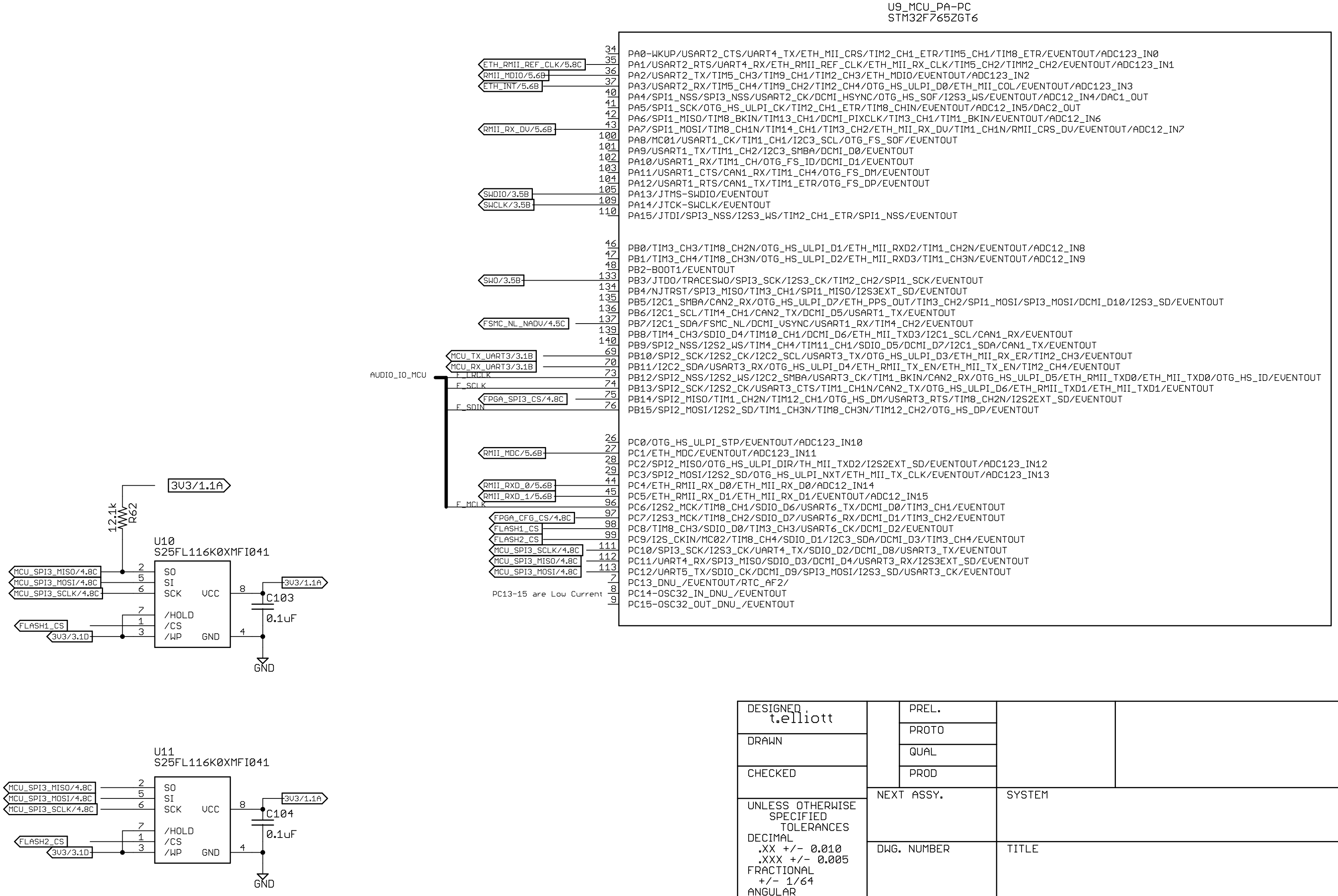

DESIGNED
t.elliott
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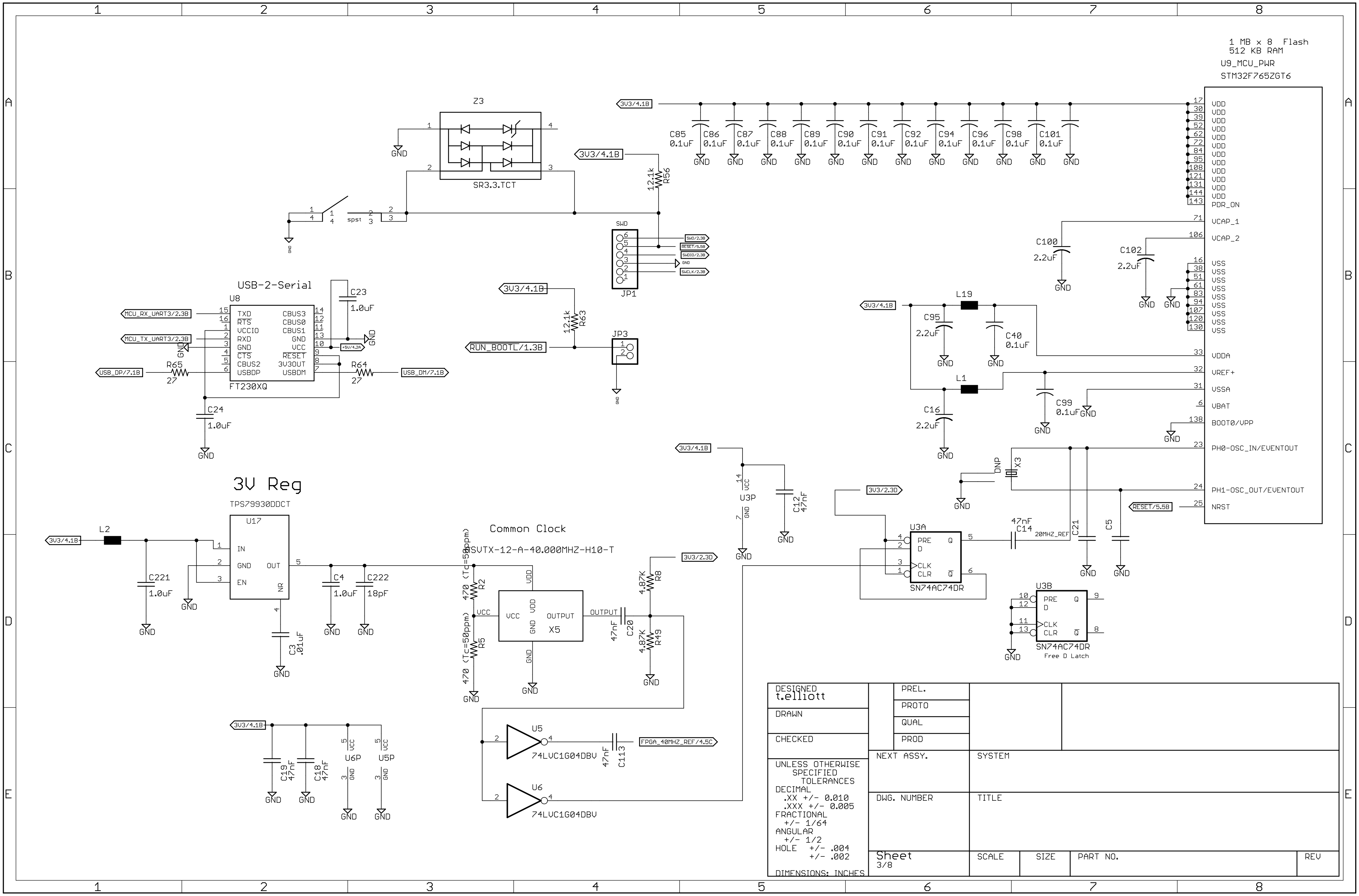
UNLESS OTHERWISE
SPECIFIED
TOLERANCES
DECIMAL
.XX +/- 0.010
.XXX +/- 0.005
FRACTIONAL
+/- 1/64
ANGULAR
+/- 1/2
HOLE +/- .004
+/- .002
DIMENSIONS: INCHES
NEXT ASSY.
SYSTEM
DWG. NUMBER
TITLE
Sheet
2/8
SCALE
SIZE
PART NO.
REV



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t.elliott

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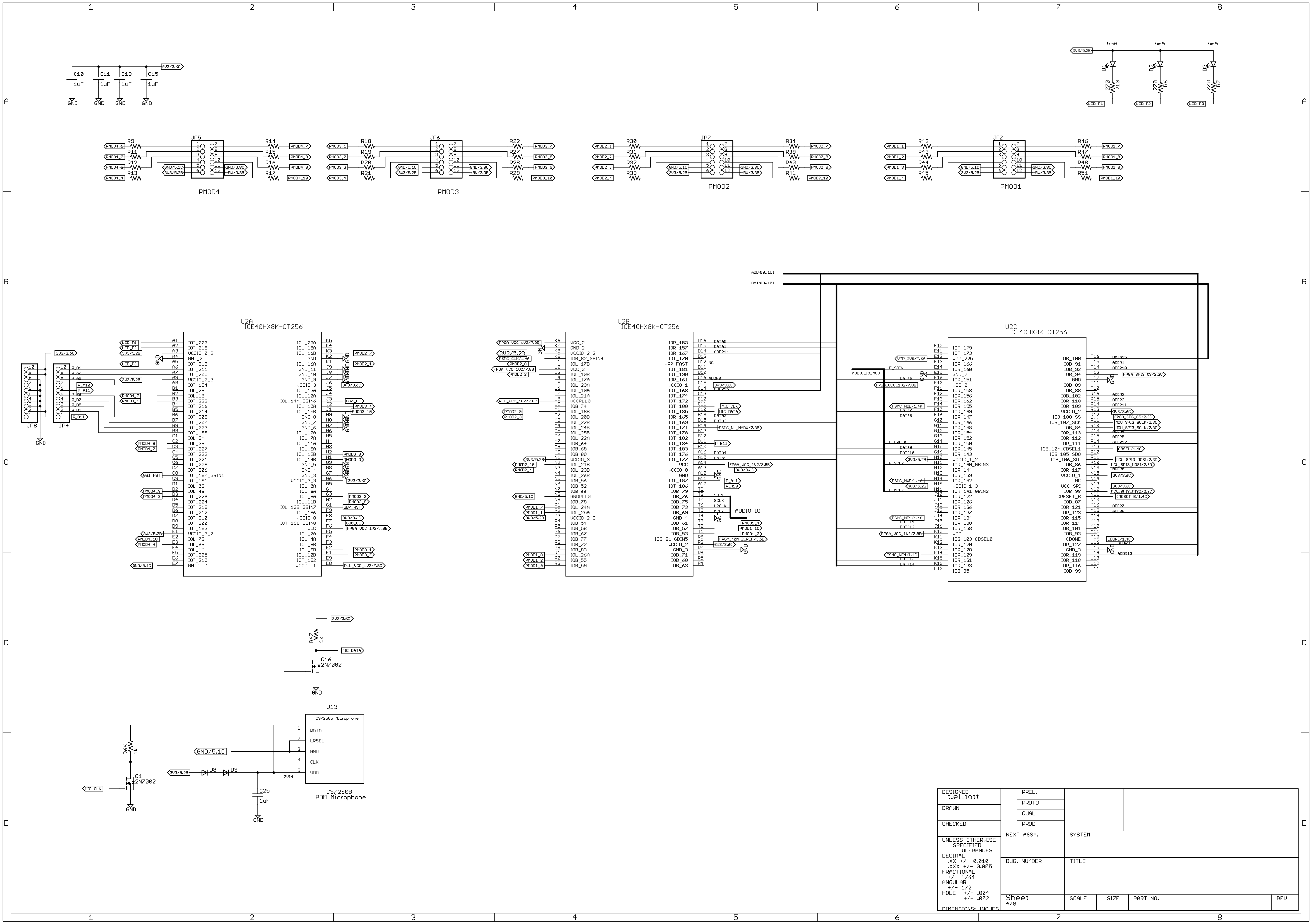
UNLESS OTHERWISE
SPECIFIED
TOLERANCES
DECIMAL
.XX +/- 0.010
.XXX +/- 0.005
FRACTIONAL
+/- 1/64
ANGULAR
+/- 1/2
HOLE +/- .004
+/- .002
DIMENSIONS: INCHES

PREL.
PROTO
QUAL
PROD

NEXT ASSY.
SYSTEM
DWG. NUMBER
TITLE

Sheet
3/8

SCALE
SIZE
PART NO.
REV



DESIGNED t.elliott
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PREL.
PROTO
QUAL
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NEXT ASSY.
SYSTEM
UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMAL
.XX +/- 0.010
.XXX +/- 0.005
FRACTIONAL
+/- 1/64
ANGULAR
+/- 1/2
HOLE +/- .004
+/- .002
DIMENSIONS: INCHES
DWG. NUMBER
TITLE
Sheet 4/8
SCALE
SIZE
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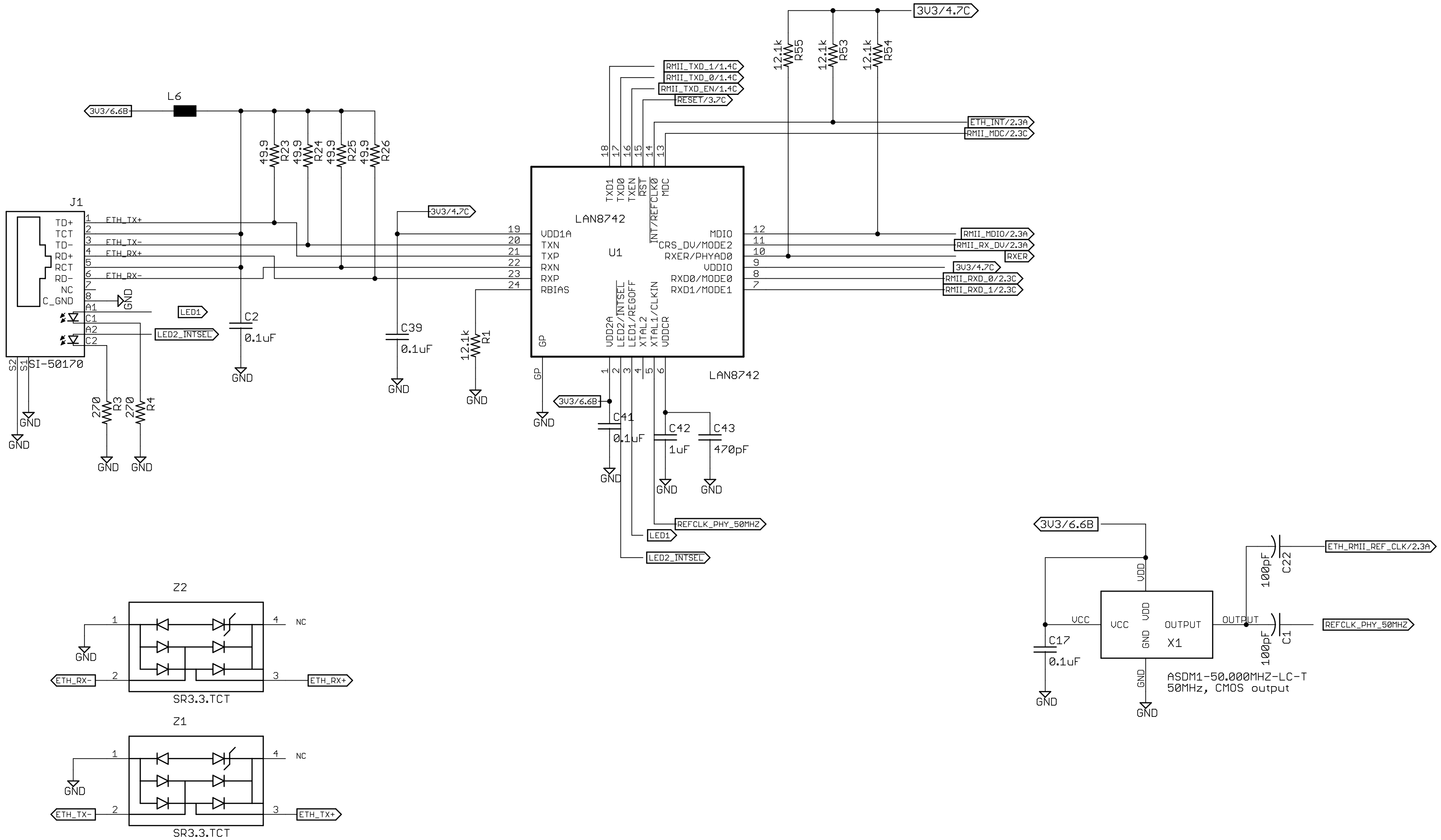

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t.elliott

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UNLESS OTHERWISE
SPECIFIED
TOLERANCES
DECIMAL
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.XXX +/- 0.005
FRACTIONAL
+/- 1/64
ANGULAR
+/- 1/2
HOLE +/- .004
+/- .002
DIMENSIONS: INCHES

PREL.
PROTO
QUAL
PROD

NEXT ASSY.

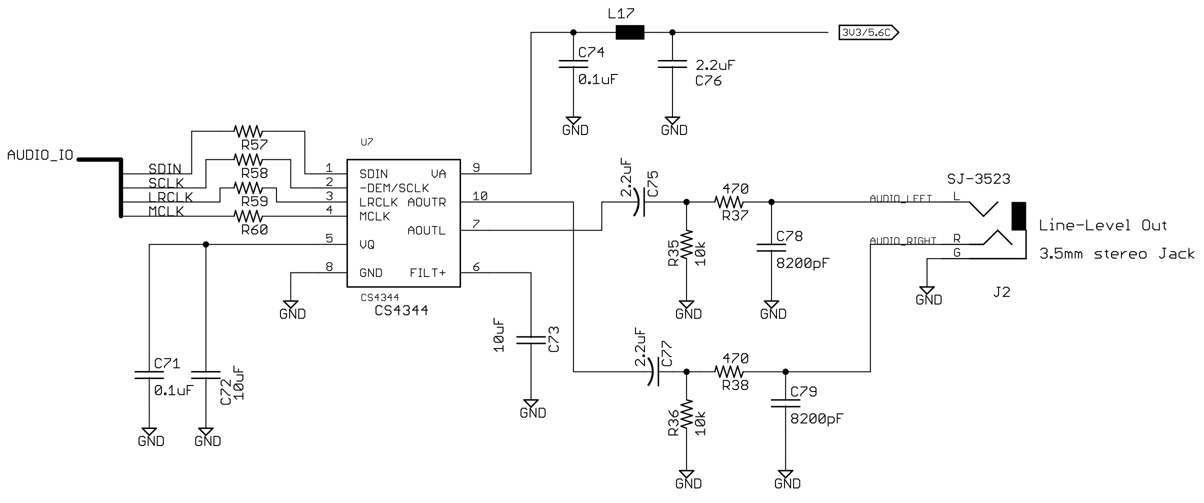
SYSTEM

DWG. NUMBER

TITLE

Sheet
5/8

SCALE
SIZE
PART NO.
REV



DESIGNED
t.elliott

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CHECKED

UNLESS OTHERWISE
SPECIFIED
TOLERANCES
DECIMAL
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.XXX +/- 0.005
FRACTIONAL
+/- 1/64
ANGULAR
+/- 1/2
HOLE +/- .004
+/- .002
DIMENSIONS: INCHES

PREL.
PROTO
QUAL
PROD

NEXT ASSY.

SYSTEM

DWG. NUMBER

TITLE

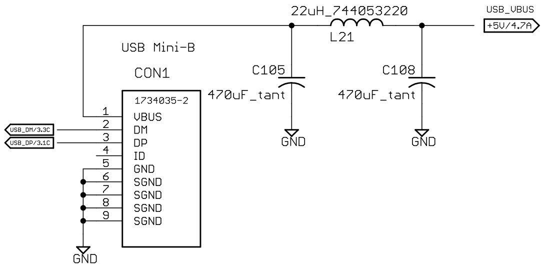
Sheet
6/8

SCALE

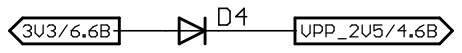
SIZE

PART NO.

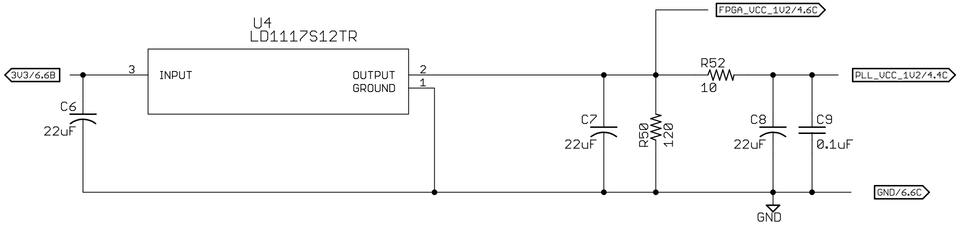
REV
1



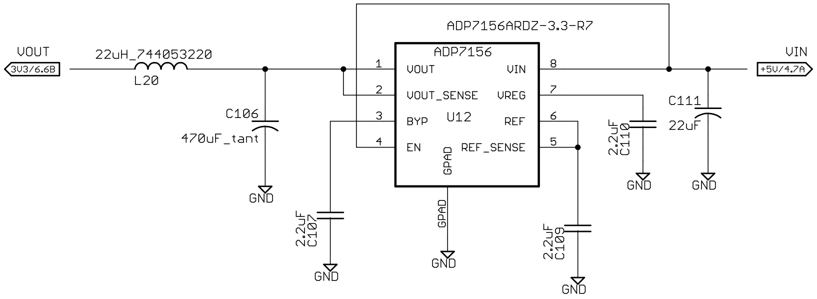
2.5V supply



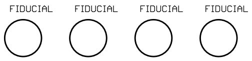
1.2V supply



3.3 Volt Supply Digital



Ultra Low-Noise 3v3 Rail



DESIGNED
t.elliott
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PREL.
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UNLESS OTHERWISE
SPECIFIED
TOLERANCES
DECIMAL
.XX +/- 0.010
.XXX +/- 0.005
FRACTIONAL
+/- 1/64
ANGULAR
+/- 1/2
HOLE +/- .004
+/- .002
DIMENSIONS: INCHES

NEXT ASSY.
SYSTEM
DWG. NUMBER
TITLE

Sheet
7/8
SCALE
SIZE
PART NO.
REV
1

Changes from rev0

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fix AC coupling into inverters for 40mhz clock done

add R57, R58, R59, R60

add R53, R54, R55, R56

Fix missing VCC_IO2 connection on FPGA

change C105 and C108 to 470uF tant (already on bom)

Disconnect MISO / from FPGA P12

add D5,D6,D7, R61

change phy address to 1 via pullup

add X3, C5, C21 all DNP

add R62

added FSMC_CLK signal

add FT230XQ USB to UART bridge

added PDM MEMS Microphone