S0
MAR_load <= 1
PC_valid <= 1
PC_inc <= 1

S1 MEM_en <=1

S2
MEM_valid <= 1
IR_load <= 1

IR_opcode == J

IR_opcode == BZERO or
IR_opcode == BGREATER or
IR_opcode == BLESS

(else)

IR_opcode == INC   IR_opcode == NOP   IR_opcode == WAIT

S3
IR_valid <= 1
MAR_load <= 1
IOAR_load <= 1

S0

S10

IR_opcode == STORE   IR_opcode != STORE

WAKE_SIGNAL == 1

S8

S4
ALU_valid <= 1
MDR_load <= 1
IODR_load <= 1

MEM_en <= 1
IO_en <= 1   S6

S0

BRANCH_trigger == 1

(else)

S9

S5
MEM_en <= 1
MEM_rw <= 1
IO_en <= 1
IO_rw <= 1

S7
MEM_valid <= 1
IO_valid <= 1
ALU_enable <= 1
ALU_cmd <= cmdDecode(IR_opcode)

IR_valid <= 1
PC_load <= 1

S0

S0

S0

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