Timing diagram showing Wishbone bus signals:

| Time | 5210 ns | 5220 ns | 5230 ns | 5240 ns | 5250 ns | 5260 ns | 5270 ns | 5280 ns | 5290 ns | 5300 ns | 5310 ns | 5320 ns | 5330 ns |

- wb_stb_i=1
- wb_cyc_i=1
- wb_we_i=0
- wb_ack_o=1
- wb_adr_i[31:0]=F0000000 : 00000258, F0000000
- wb_sel_i[3:0]=F : F
- wb_dat_i[31:0]=00000060 : 00000000, 00000060
- wb_dat_o[31:0]=00000000 : 000000xx, 00000000
- uart_rxd=z
- uart_txd=1