

# Intrinsic Evolvable Hardware for Combinatorial Synthesis Based on SoC+FPGA and GPU Platforms

Artificial Life, Robotics, Evolvable  
Hardware

## ABSTRACT

Evolutionary algorithms are another option for combinatorial synthesis because they allow for the generation of hardware structures that cannot be obtained with other techniques. This paper presents a novel a parallel genetic programming (PGP) boolean synthesis implementation on a low cost cluster of an embedded platform called SIE, based on a 32-bit processor and a Spartan-3 FPGA. Some tasks of the PGP have been accelerated through a hardware coprocessor called FCU, that allows to evaluate individuals onchip as intrinsic evolution. Results have been compared with GPU and HPC implementations, resulting in speedup values up to approximately 2 and 180 respectively.

TRACK: Genetic Programming.

## Keywords

Embedded systems, Evolutionary algorithms, boolean synthesis, cluster.

## 1. INTRODUCTION.

One of the main goals in combinatorial synthesis consists of finding compact boolean expressions in the sum of products (SOP) form with the smallest possible number of variables and terms. Boolean algebra offers a way to find compact expressions, but this process depends on the designer's experience, resulting in non-optimal or inadequate expressions. There are other techniques available for combinatorial synthesis such as the Karnaugh maps, the Quine-McCluskey algorithm, the Reed-Muller algorithm. In general terms, these algorithms have disadvantages such as exponential complexity, lack of restrictions management, and multiple solutions.

As an alternative to the traditional design of combinatorial circuits, some authors have proposed bio-inspired techniques to create combinatorial circuits that can not be obtained with the traditional methods and to add some restrictions to the design such as delay, area, etc. Nicholson [14] has used Simple Genetic Algorithms (SGAs) with a fixed

length representation for small problems, Kajitani [11] has worked with Variable-length Genetic Algorithms (VGAs) evolving up to 6-bit problems. Aguirre *et al* [1] used tree-based genetic programming (GP) for evolving small circuits, Xu [23] has worked with adaptive immune GA obtaining only 4-variable circuits, as well as Coello with ant colony algorithms [3]. Others authors have proposed a platforms to use reconfiguration techniques with hard-time restrictions due the high reconfiguration latency [20, 13, 19].

One of the main problems to create circuits by using these techniques is the response time, due the high computational requirements for implementing any bio-inspired algorithm. As a result, only small circuits can be created in reasonable time [21, 12]. To solve the scalability restriction of creating digital circuits by using parallel genetic programming (PGP), we have developed a low cost cluster-based SoC + FPGA architecture called SIE. A fitness coprocessor unit (FCU) was developed on each FPGA in order to accelerate the convergence of a Intrinsic PGP (individuals are tested in the same platform), as well as provides an appropriate support for 8 variables synthesis problems.

These strategies allow to create combinatorial blocks that cannot be obtained with traditional methods, and to add some restrictions to the design such as delay and area. These designs have a very low limited number of variables [4] and they are mainly oriented to obtain a few basic structures.

In order to use parallel genetic programming (PGP), an FPGA cluster-based architecture to solve the combinatorial synthesis problem on-chip has been developed. The fitness coprocessor unit (FCU) on each FPGA helps to accelerate the convergence of the algorithm, as well as provide an appropriate support for 12-variable synthesis problems. The success of the system is mainly due to the capability of evaluating a chromosome in the FPGA through a virtual LUT-oriented architecture without using high-latency partial reconfiguration techniques, and determining the fitness value for an individual faster than other related works.

Due to that the capability of GP to run on massive parallel architectures, the proposed synthesis algorithm was compared to a High Performance Cluster (HPC) and a graphics processing unit (GPU) implementations.

## 2. GENETIC PROGRAMMING IN COMBINATORIAL SYNTHESIS

This section describes some of the most important aspects of the proposed evolutionary algorithm for the combinatorial synthesis problem, such as chromosome representation, the fitness problem and the genetic operators.

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee.

GECCO 2011 2011 Genetic and Evolutionary Computation Conference  
Copyright 20XX ACM X-XXXXX-XX-X/XX/XX ...\$10.00.

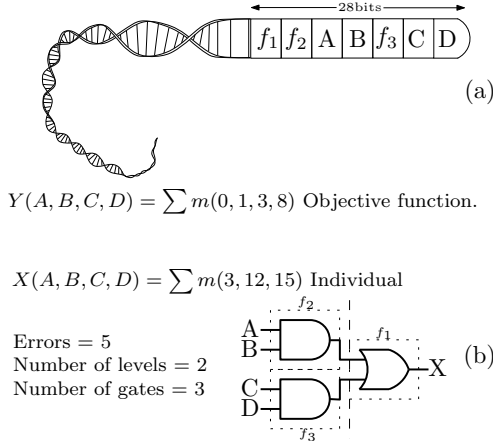
## 2.1 Chromosome representation.

The codification is the way a logic circuit is represented using a bit array in order to be used in the evolution process [5]. This representation must be able to represent all the different solutions to the problem, also the crossover and mutation operators should not generate infeasible individuals, and it must cover all the solution space. There are different ways of representing combinatorial hardware for a genetic algorithm: tree-based representation in 2-D, PLD-like structures and cartesian representation are some of them [8] [18] [9].

The 2-D tree representation is appropriate for implementing parallel systems because it allows splitting the chromosomes for balancing the computational load [15]. Figure 1 shows the selected cell-based structure representation. Each basic cell has 3 functions  $f$  and 4 input variables  $v$  coded in binary. This representation allows the addition of more cells to represent larger circuits. It must be mentioned that the chromosome length has to be variable because the length of the solution to the synthesis problem is unknown a priori.

## 2.2 Fitness function.

Finding the appropriate fitness function is important because it is responsible for quantifying the way a chromosome or individual meets or does not meet the requirements.



**Figure 1: Cell-based structure representation.**

$$fitness = \omega_1 \cdot \left[ \sum_{j=1}^m \sum_{i=1}^n Y(j, i) - X(j, i) \right] + \omega_2 \cdot P(x) + \omega_3 \cdot L(x) \quad (1)$$

In equation 1 the fitness function for the proposed GP is shown. Constants  $\omega_1$ ,  $\omega_2$  and  $\omega_3$  are used for establishing the weights of each of the parameters that will determine the fitness function. The double-summation term calculates the number of matches of the individual  $X$  for all the possible combinations at the output with the target functions  $Y$ ; the  $P(X)$  function is used for calculating the number of logic gates of a chromosome taking into account some of the *introns* or segments of the genotype string that will not have any associated function and that do not contribute to the result of the logic circuit that they represent. The function  $L(X)$  is used for determining the number of levels the circuit

has, or in other words the number of gates that the critical path crosses. The  $m$  constant is the number of outputs in the circuit and  $n$  the number of possible combinations of inputs in the circuit.

## 2.3 Genetic operators.

The selection operator is responsible for identifying the best individuals of the population taking into account the exploitation and the exploration [15]. The first one allows the individuals with better fitness to survive and reproduce more often, and the second one means searching in more areas and making it possible to find better results. In the other hand, the mutation operator modifies the chromosome randomly in order to increase the search space. It can change: 1) an operator or variable and 2) a segment in the chromosome. Both are executed randomly with a certain probability. A variable mutating probability during the execution of the algorithm (evolvable mutation) [16] is more effective for evolvable systems. Finally, the crossover operator combines two selected individuals for obtaining two additional individuals to add to the population. A crossover system with one or two crossover points randomly selected has been implemented because it is more efficient for evolvable systems [10].

## 3. COPYLEFT SIE PLATFORM.

The hardware project copyleft SIE [?] [?] created by our team work, is composed of a custom embedded platform and a software development kit based on Linux operating system; allowing the generation of commercial applications under the Creative Commons BY-SA licenses, which allows the distribution and modification of the design (including commercial applications), with only the requirements that the derived products be under the same license and that the proper credit be given to the author of the original work. This is what defines the base of the *hardware copyleft* products.

### 3.1 The SIE Platform.

The SIE platform is composed by a System-On-a-Chip processor and a FPGA (Figure 2). The SoC is a MIPS processor (Ingenic JZ4725) running at 400MHz with peripherals that allows to control: a 2GB NAND memory for file storage, a 32MB SDRAM, a serial communication channel (UART), micro-SD memories, I2C port, 3-inch color LCD display, 2 input and 1 output audio stereo interfaces and 2 analog inputs. The XC3S500E Xilinx FPGA gives 25 GPIOs and controls an 8 channel analog-to-digital converter. There are two communication channels between the FPGA and the processor, the first one is a JTAG that allows the FPGA configuration and the execution of tests to the implemented circuits. The data, address and control buses are part of the second channel, which is used to exchange information between the processor and the peripherals implemented inside the FPGA.

SIE provides power connection through a USB port, which is also configured as a network interface. This allows the file transfer and the execution of a remote console using the *ssh* protocol. This communication channel can also be used to configure the non-volatile NAND memory, which simplifies the whole configuration of the platform through the USB port.

SIE provides an economical alternative (70 USD per node)

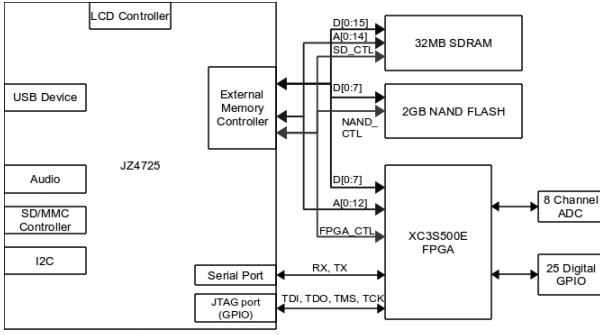


Figure 2: SIE development platform structure

for implementing evolutionary algorithms; Vasicek et al. [17], Higuchi et al. [7] and Sekanina[24] use architectures based on Xilinx Virtex 2 Pro family for implementing similar applications, closed to 1000 USD y 3000 USD per node. By separating the FPGA and the processor and providing a communication channel between them, SIE can use cheaper devices (4 USD for the processor, 10 USD for the FPGA) reducing significantly the cluster's costs. On the other hand, selected GPU for the present work is about 200 USD.

## 4. GP IMPLEMENTATION

The GP was implemented in two stages: the first one is about software development and its parallelization on HPC and GPUs, and the second one refers to a hardware implementation to speed it up on the SIE plataform.

### 4.1 Parallel software design.

#### 4.1.1 HPC

Natural evolution works with a whole population not with a single individual (except for selection and reproduction) some operations can be done separately, therefore almost all operations in a GP are implicitly parallel. Using the island approach, the population is divided into sub-populations that will evolve in each processor of the cluster or parallel architecture. Figure 3 shows the GP communications scheme in the parallel system. When the system starts, each processor receives the objective function (i.e, a true table), creates its sub-population and starts the evolution process, consisting of fitness evaluation, selection, crossover, mutation and reproduction. Once the system reaches a number of generations, some individuals are selected to be transfered from one processor to another one. A master processor is in charge of collecting the in-transfer individuals and moving them to the rest of the nodes (slaves),

Increasing the probability of convergence of the algorithm [2]. The ratio of data exchange (the number of the best individuals to exchange increases the probability of finding a better solution) and migration frequency are important parameters to improve the performance of the algorithm.

To implement communications in SIE, a custom message passing library was created to program the distributed system. Standard libraries such Open MPI executes on SIE with a very low performance, due they were designed for robust platforms.

#### 4.1.2 GPU.

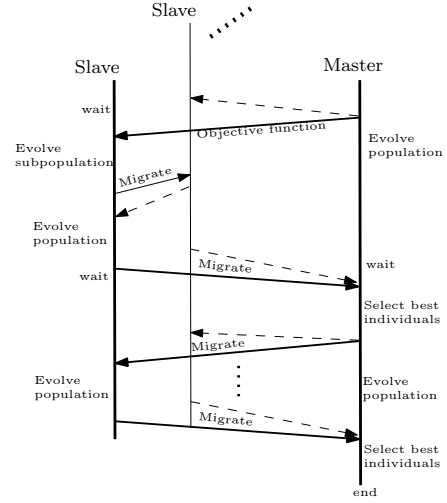


Figure 3: GP communications scheme in parallel architecture.

Two main parts can be identified to implement the system on GPUs. The first part involves the random number generation and the second one the GP as such. The GP requires random numbers for generating an initial population and then to mutate and cross their individuals. Due that a GPU can not generate random numbers by using C classical libraries, it is necessary generate them in a different way. Generate these numbers on CPU and then transport them to the GPU is not viable because it takes a lot of system clocks. To solve this problem a Mersenne-twister algorithm is executed on the GPU before the *kernel - GP* to make a buffer of random numbers on its own global memory.

#### Kernel structure..

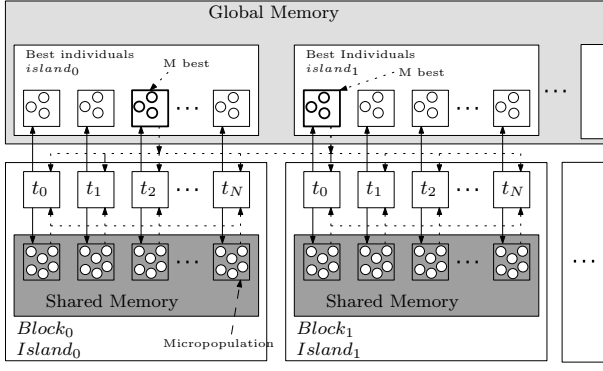
Figure 4 shows the way the GP has been implemented on the graphics device. A thread  $t$  executes a *kernel - GP* (a common segment of code that process different data in each instance), and generates a  $\mu$ -population, performs the operators of selection, mutation and crossover a number of generations required. After  $P$  generations,  $M$  individuals will be transferred to the global memory and then to the host device (CPU system).  $P$  is known as the frequency of migration and the  $M$  number is called the migration factor.

Also, it can be observed that each thread can cooperate with other threads inside the same block through shared memory, sharing the best individuals and improving the efficiency of the GP.

### 4.2 Hardware design.

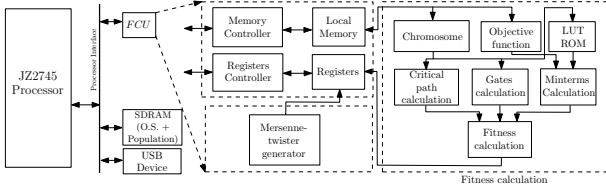
In the second stage a profiling of the software implementation with gprof tool, determined that the most costs were the fitness function calculation and the new individual generation (25% and 35% of the execution time, respectively).

Therefore, these two steps have been accelerated with a dedicated hardware in the FPGA. The Fitness Calculation Unit (FCU, see Figure 5) is the hardware element designed in order to accelerate this processes. This coprocessor is connected to the JZ4725 processor through its custom interface (using data, address, control buses).



**Figure 4: GPU implementation of the evolvable algorithm.**

Inside the FCU, the chromosome passes from the DRAM memory to local memory through the custom interface, and each of its basic cells are converted to an equivalent Virtual Look Up Table (VLUT) with a ROM based translation. Then the number of wrong minterms is calculated using the information from the objective function and a counter as input. Finally, the FCU calculates the final fitness value including the number of gates and the critical path, and will be sent back to the JZ4725 processor. In order to speed up pseudo random number generation, a Mersenne-Twister-based coprocessor was inserted through the same custom interface.



**Figure 5: FCU structure.**

## 5. PERFORMANCE EVALUATION.

To obtain the performance and prove the scalability of the algorithm in SIE, it was compared to two parallel architectures. The first one is a High Performance Computer (HPC) called ALTAMIRA. The HPC setup is made up of 18 eServer BladeCenters with 256 JS20 nodes (512 processors), using a Myrinet network with 1 Gbps bandwidth. The second platform is a GPU architecture based on a NVIDIA GTS450, made by 192 CUDA cores, each one working at 1,56 GHz and a DDR5-1GB global memory.

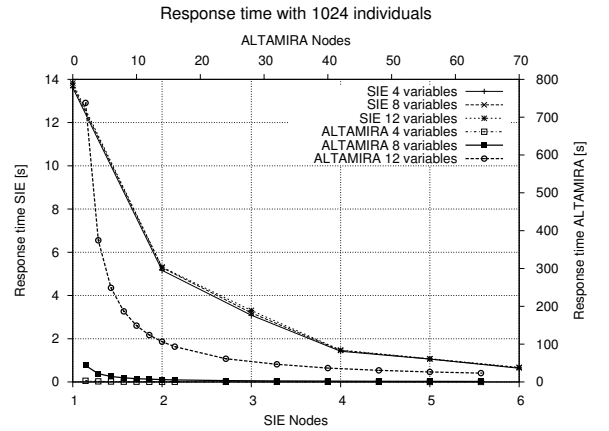
On the other hand, the SIE configuration is made up of 6 JZ4725-FPGA nodes with the architecture described above. The response time is measured for the parallelized versions of the GP in both ALTAMIRA and SIE. Several scenarios have been tested with different input parameter configurations: 1) number of input variables (4, 8 or 12, corresponding to a comparator problem of 2, 4 and 6 bits); 2) population size (512, 1024 or 2048) and 3) number of nodes running the experiment, ranged from 1 to 6 in SIE, and 2 to 16 or 64 in ALTAMIRA. The first and second parameters determine

the size of the problem. The last one gives an idea about the scalability of the system.

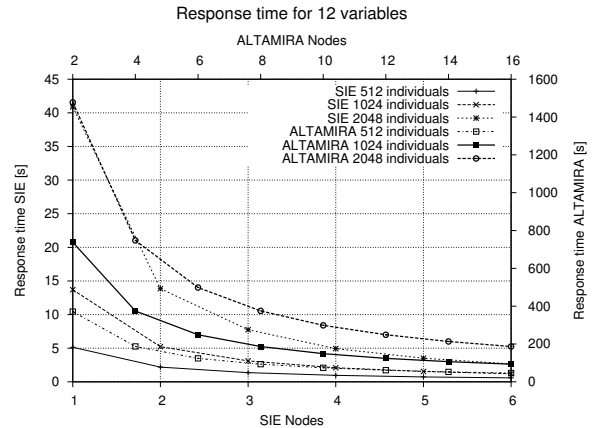
### 5.1 Response Time.

Figure 6 shows the response time for both platforms with different numbers of nodes and variables with 1024 individuals during 100 generations. These results show the high performance of SIE cluster for the algorithm. This experiment demonstrates that the response time for SIE does not depend on the size of the problem. In contrast, response time in ALTAMIRA has a high dependency of the size of the problem, because individuals had to be evaluated by software.

Figure 7 shows the response time in both architectures when varying the number of individuals of the population. It is observed that both architectures have a strong dependency of the number of individuals in the algorithm. This is because increasing this number causes an increment of the software computational load for both clusters. Even in this scenario, SIE shows an excellent performance compared to ALTAMIRA.



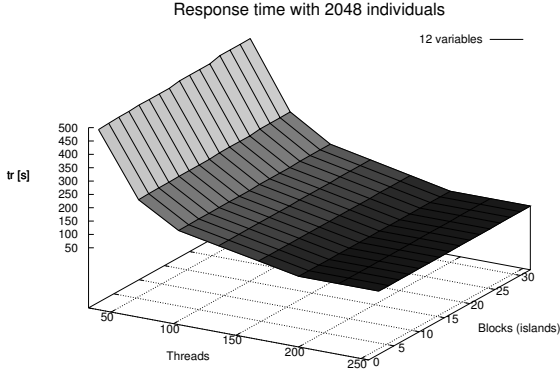
**Figure 6: Response time in SIE and ALTAMIRA for different number of variables.**



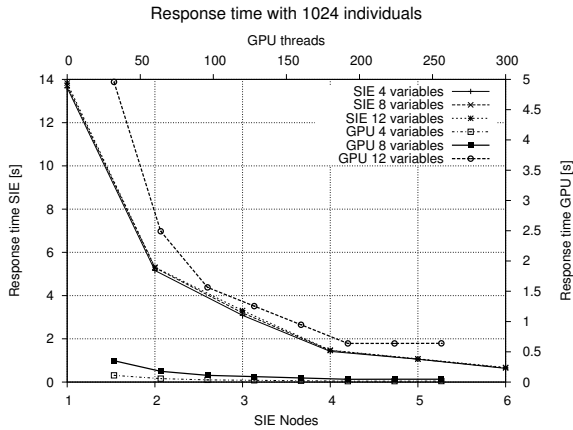
**Figure 7: Response time in SIE and ALTAMIRA for different number of individuals.**

Figure 8 shows the response time of executing the GP in

the graphics hardware with problems of 4, 8 and 12 variables are fixed. Varying the number of islands and threads, can be observed that the best scenario is obtained when the number of threads is increased independently the number of islands. This is because when more threads are launched more parallelism is performed in the system, until the maximum of threads permitted by the GPUs is reached.



**Figure 8: Response time of the algorithm in NVIDIA GTS450 GPU.**

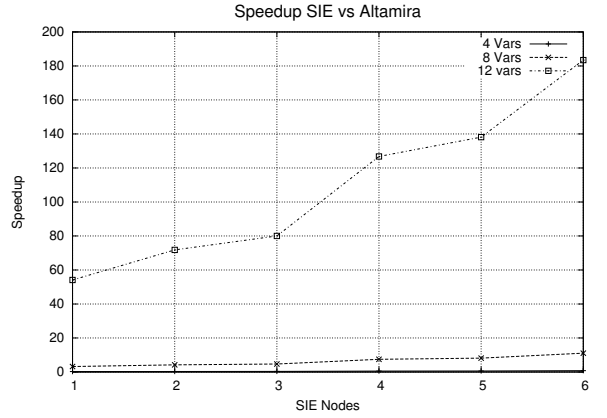


**Figure 9: Response time in SIE and GPU for different number of individuals.**

## 5.2 Speedup.

The speedup of the SIE vs ALTAMIRA for different number of variables is presented in figure 10 with the number of variables fixed to 12. The excellent performance of SIE can be explained because individuals have been directly tested in hardware (FPGA), obtaining a combination of their true table on each cycle of the system clock. On the other hand, individuals evaluated in software by ALTAMIRA require a lot of system clocks, causing response times hundreds of times higher than SIE.

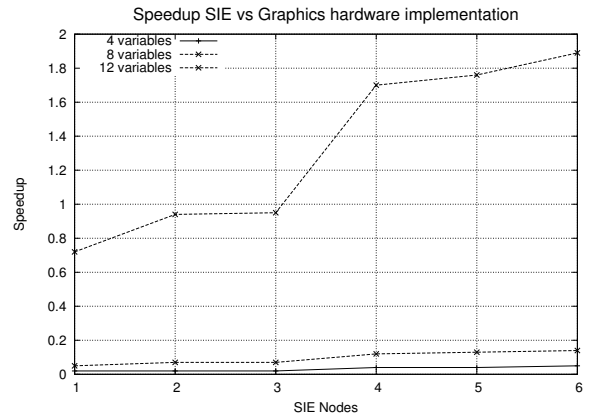
On the other hand, figure 11 shows the speedup number when SIE and GPU are compared. It can be observed that SIE performance is higher than GPU only when 12-variables



**Figure 10: Speedup of SIE vs Altamira comparing 1 SIE node = 2 Altamira nodes.**

problems are evolved. This can be explained because the whole population have been tested in hardware, obtaining a combination of their output on each cycle of the system clock. But, when an individual is tested in software, each combination requires a set of instructions, that requires a lot of cycles of the system clock.

The obtained speedup number is significant (about 50 and 180) when SIE is compared against ALTAMIRA. In [22, 6] the obtained speedup is about 30-40 when 1 accelerator processor was used and compared against a single PC.



**Figure 11: Speedup of SIE vs GPU comparing 1 SIE node = 32 threads.**

## 6. CONCLUSIONS AND FUTURE WORK.

This paper presented a novel way to evaluate individuals in an intrinsic evolvable algorithm on an open embedded platform called SIE, and results were compared to an HPC called ALTAMIRA and a high performance NVIDIA GPU. To accelerate the evolution process, a coprocessor was implemented to calculate the fitness function and to generate random numbers, improving the performance for problems with more than 6 bits.

Results showed a speedup of 2 when SIE was compared

to GPU, even when 192 processing cores were used in the last one. When compared with ALTAMIRA, SIE showed a speedup up to 180, due the high computational load in software when 16 nodes were used in ALTAMIRA. Significant speedup numbers were obtained due individuals have been directly tested in hardware, getting a combination of their true table on each cycle of the system clock. In the other hand, when an individual is tested in software, each combination requires a set of instructions, that requires a lot of cycles of the system clock.

Tests proved that the algorithm is more effective for 4-bit and 8-bit problems. 12-bit problems in SIE had excellent performance, but because the search space is too long, converging to a suitable solution was difficult for the algorithm. This problem could be solved as future work with some improvements in terms of multiple FCUs inside an FPGA, more nodes, and other hardware-accelerated genetic operators.

## 7. REFERENCES

- [1] A Aguirre, C Coello, and B Buckles. A genetic programming approach to logic function synthesis by means of multiplexers. *Proc. of the I NASA/DoD Workshop on Evolvable hardware.*, pages 46 – 53, 1999.
- [2] Erick Cantú-Paz. Migration policies, selection pressure, and parallel evolutionary algorithms. *Journal of Heuristics*, 7(4):311–334, 2001.
- [3] CAC Coello, RL Zavala, and BM Garcia. Ant colony system for the design of combinational logic circuits. *Lecture Notes in Computer Science*, pages 21–30, 2000.
- [4] D Goldberg and J Holland. Genetic algorithms and machine learning. *Machine Learning*, January 1998.
- [5] F. Rothlauf. *Representations for genetic and evolutionary algorithms*. Springer, January 2006.
- [6] Zbysek Gajda and Lukas Sekanina. An efficient selection strategy for digital circuit evolution. In *Evolvable Systems: From Biology to Hardware*, LNCS 6274, pages 13–24. Springer Verlag, 2010.
- [7] J. Jeon and P. Rhee. An Evolvable Hardware System Under Varying Illumination Environment. *Advances in Natural Computation*.
- [8] J Koza, F Bennett, D Andre, and M Keane. Genetic programming iii: darwinian invention and problem solving. *Evolutionary Computation*, January 1999.
- [9] J Miller and P Thomson. Aspects of digital evolution: Evolvability and architecture. *Lecture Notes in Computer Science*, January 1998.
- [10] J Miller and P Thomson. Aspects of digital evolution: Evolvability and architecture. *Lecture Notes in Computer Science*, January 1998.
- [11] I Kajitani, T Hoshino, M Iwata, and T Higuchi. Variable length chromosome ga for evolvable hardware. *Evolutionary Computation*, pages 443 – 447, Jan 1996.
- [12] JR Koza, MA Keane, MJ Streeter, W Mydlowec, and J Yu. Genetic programming iv: Routine human-competitive machine intelligence. *Kluwer Academic Publishers*, 2005.
- [13] Juan Manuel Moreno, Yann Thoma, and Eduardo Sanchez. Poetic: A prototyping platform for bio-inspired hardware. In *ICES*, pages 177–187, 2005.
- [14] A Nicholson. Evolution and learning for digital circuit design. *Proc. Genetic and Evolutionary Computation Conf*, pages 519 – 524, 2000.
- [15] Q. Yu, C. Chen, and C. Pan. Parallel genetic algorithms on programmable graphics hardware. *Lecture notes in computer scienc*, January 2006.
- [16] R Krohling, Y Zhou, and A Tyrrell. Evolving fpga-based robot controllers using an evolutionary algorithm. *Proc. I Int. Conf. on Artificial Immune Syst*, January 2002.
- [17] R. Oreifej, R. Al-haddad, H. Tan, and R. Demara. Layered Approach to Intrinsic Evolvable Hardware Using Direct Bitstream Manipulation of Virtex II PRO Devices. *International Conference on Field Programmable Logic and Applications*, 2007.
- [18] T Higuchi, T Niwa, T Tanaka, H Iba, and H de Garis. Evolving hardware with genetic learning: a rst step towards building a darwin machine. *Proc. of the second Int. Conf. on from animals to animats*, January 1992.
- [19] Andres Upegui and Eduardo Sanchez. Evolving hardware by dynamically reconfiguring xilinx fpgas. In *ICES*, pages 56–65, 2005.
- [20] Andres Upegui and Eduardo Sanchez. Evolving hardware with self-reconfigurable connectivity in xilinx fpgas. In *AHS*, pages 153–162, 2006.
- [21] Z Vascek and L Sekanina. Hardware accelerators for cartesian genetic programming. *Lecture Notes in Computer Science*, pages 230–241, 2008.
- [22] Zdenek Vasicek and Lukas Sekanina. Hardware accelerators for cartesian genetic programming. In *Eleventh European Conference on Genetic Programming*, LNCS 4971, pages 230–241. Springer Verlag, 2008.
- [23] H Xu, Y Ding, and Z Hu. Adaptive immune genetic algorithm for logic circuit design. *Proc. of the first ACM/SIGEVO*, pages 639–644, 2009.
- [24] Z. Vasicek and L. Sekanina. An evolvable hardware system in Xilinx Virtex II Pro FPGA. *Int. J. Innovative Computing and Applications*, 2007.