Design, Simulation and Experiment of a PID Using Rapid Control Prototyping Techniques

Odair Augusto Trujillo, Fredy Edimer Hoyos † and Nicolás Toro García ‡
Department of Electrical and Electronics Engineering and Computer Sciences
Universidad Nacional de Colombia Sede Manizales, Km 7 vía al aeropuerto Campus La Nubia, Manizales, Colombia
Email: haldrik@gmail.com
† Email: fehoyosv@unal.edu.co
‡ Email: ntoroga@unal.edu.co

***Abstract*—To analyze the performance of the PID controller in a buck type converter implemented in real time, the start of design will be the continuous controller using the analytical method for calculating PIDs. PWM is then used and from this point you will find the bifurcation diagrams analytically and it will show some problems of switching and sampling time. Then the model of the converter is used and implements PID controller [1] in a dSPACE. In the experimental case it shows in more detail the requirements of sampling frequency and switching speed. Finally it shows the performance of PID controller.**

***Index Terms*—PID, rapid control prototyping, numerical bifurcation diagrams, PID hardware, PID software, PID tuning, DC-DC converters, PWM.**

I. Introduction

You could say that the buck converter is a switching power supply with two semiconductor devices, transistor (Q) and diode (D), an inductor (L), an output capacitor (C) and its respective load, as shown in Figure 1. This system usually converts an unregulated DC voltage to another regulated lower voltage. The transistor switches the input power E by pulse width modulation PWM to feed the filter LC, the diode conducts when the transistor is off if there is positive current in the coil, the inductor does not allows rapid changes in current and the capacitor does not support abrupt changes of voltage creating between them a low pass filter. This process gives an average voltage lower than the input. The device used for switch is a MOSFET. Thus, the control technique must determine the switch's time "on" and "off", this control form where the input of the system switches between two values is known as pulse width modulation (PWM) [2], [3], [4], [5], [6].

Figure 2 shows a block diagram of the system under study. This system is divided into two major subgroups, the hardware that includes the physical and electronic components and the software implemented on a dSPACE which performs the signal acquisition and implementation of PID control technique.

The hardware consists of: a sensor measuring V_C state variable (capacitor voltage) this are high impedance resistors connected in parallel. The converter's switch is handled from

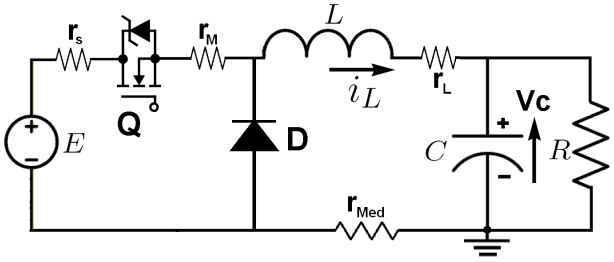

Figure 1. Buck converter model

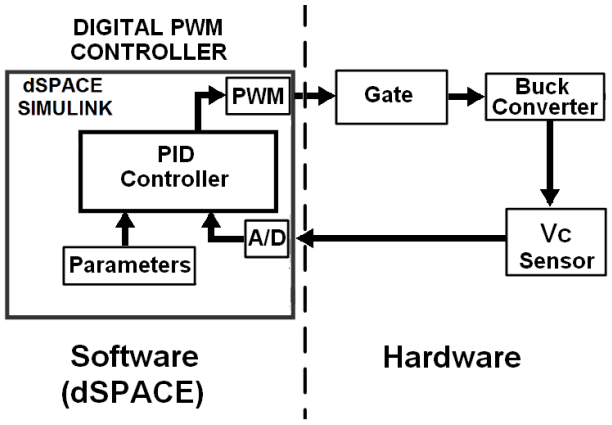

Figure 2. Block diagram of the proposed system

the control and development card through the PWM, the pulse is opto-isolated through fast optocouplers.

The digital part is developed in the control and development card dSPACE DS1104, where the the PID control technique is implemented. This card is programmed with Matlab/Simulink® platform and has a display interface called ControlDesk. The controller is implemented in Simulink® and downloaded to the DSP to operate at a given frequency. The state variable comes to the controller through the input ADC 12bits, with a sampling rate set for te experiment at 10 kHz and then 30 kHz. The controller parameters are set through variable gain blocks because

they were tuned in real time. At each sampling period the controller calculates the duty cycle in real time and its equivalent in PWM control switch.

This article is intended for digital PWM approach, which presents rich nonlinear dynamics and has the following advantages: immunity to analog component variations, faster process design, low sensitivity to changes in parameters, programmable, it allows reduction or elimination of passive external components, calibration of protection algorithms, and support digital systems interface for implement nonlinear control techniques, [7], [8], [9], [10], [11], [12]. But the DPWM also has disadvantages, it is affected by two limitations: quantization effects [8], [9], and delays in the control loop [13], [14].

II. Buck converter model

A. Mathematical Equivalent

$$E = (r_{int} + r_L)i_L + L\dot{i_L} + V_C$$

Where r_{int} is the internal resistance of the mosfet ($r_{_M}$) plus the resistance source (r_s) and the resistance coil (r_L) plus the shunt resistor's resistance used for the current mesure ($r_{_{Med}}$) as shown in the figure 1.

By summation of currents in the capacitor's node, it gives:

$$C\dot{V_C} = i_L - \frac{V_C}{R}$$

Solving and simplifying, it gives:

$$\dot{i_L} = -\frac{r_{in} + r_L}{L}i_L - \frac{1}{L}V_C + \frac{E}{L}$$

$$\dot{V_C} = \frac{1}{C}i_L - \frac{1}{RC}V_C$$

Converting to matrix form, it gives:

$$\begin{bmatrix} \dot{i_L} \\ \dot{V_C} \end{bmatrix} = \begin{bmatrix} -\frac{r_{int}+r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{E}{L} \\ 0 \end{bmatrix}$$
$$y = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix}$$

Converting to state variables and making $a = \frac{r_{int}+r_L}{L}$, $b = \frac{1}{L}$, $c = \frac{1}{C}$, $d = \frac{1}{RC}$ and maintaining sings, it gives:

$$\begin{bmatrix} \dot{X_1} \\ \dot{X_2} \end{bmatrix} = \begin{bmatrix} -a & -b \\ c & -d \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} + \begin{bmatrix} \frac{E}{L} \\ 0 \end{bmatrix}$$
$$y = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} \quad (1)$$

If the switch stays off, $u = 0$ the equation would be: $\dot{X} = AX$, because it doesn't take into account the diode's voltage.

In the case where the switch is closed you can find the transfer function using:

$$G(s) = \frac{Y(s)}{U(s)} = C(SI - A)^{-1}B$$

It, gives:

$$G(s) = \frac{\frac{c}{L}E}{s^2 + (a+d)s + (ad+bc)} \quad (2)$$

Remember $c = \frac{1}{C}$

In the equation 2 the following values will be replaced to find the system's response:

$$E = 40V,\ C = 46.27\mu F$$
$$R = 39.3\Omega,\ r_{int} = 0.688\Omega$$
$$L = 2.47mH,\ r_L = 1.345\Omega$$

$$G(s) = \frac{8.739e06}{s^2 + 1372s + 9.192e06} \quad (3)$$

Number 3 equation's poles are:

$$-681 \pm j2953$$

The root locus is shown in figure 3

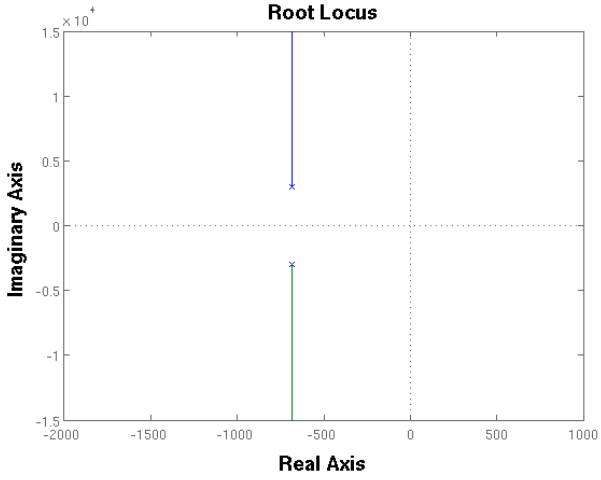

Figure 3. Root Locus

Therefore the system is stable with the values used for constants and it is underdamped.

The response to step E volts can be seen in the figure 4, where we see that in fact the system is underdamped, it has an overshoot that is necessary to reduce and has a steady-state error of about 2 volts.

In low power buck converters such as computers sources, it is usual to find a zener diode and transistor based regulation on converter output. This technique has the advantage of avoiding the use of control but in turn the disadvantage that increases

the probability of failure on points where it handles the power output. To get the desired voltage with proper mosfet handling without adding elements that may fail in the converter output is the goal of implementing a controller.

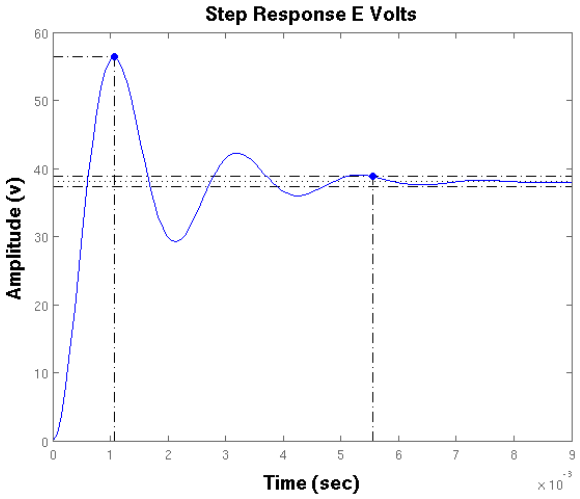

Figure 4. Step Response

III. Continuous PID controller

The used method is known as the analytical method, which start from a desired behavior, determined by the second order canonical equation, which should match to the characteristic equation of the closed loop system with PID to find the constant Kp, Kd, Ki.

A. Desired response

$ts = 2.5ms,\ Mp = 10\% = 0.1$

$$\zeta = \sqrt{\frac{ln(Mp)^2}{\pi^2 + ln(Mp)^2}} = \sqrt{\frac{ln(0.1)^2}{\pi^2 + ln(0.1)^2}} = 0.591$$

$$\sigma = \frac{4}{ts} = \frac{4}{2.5ms} = 1600$$

$$\sigma = \zeta.\omega_n \Rightarrow \omega_n = \frac{1600}{0.591} = 2707.27$$

Second order canonical equation (*desired behavior*):

$$\frac{\omega_n^2}{s^2 + 2.\zeta.\omega_n + \omega_n^2}$$

$$\frac{2707^2}{s^2 + 3200.s + 2707^2}$$

Poles on:

$$-1.600 \pm j2.183$$

Figure 5. Block Diagram

B. Closed loop with unknown PID constants

Replacing the parameters in the transfer function and making a change of variables $m = 8739229$, $n = 1372$, $p = 9191377$, you must close the loop with unknown PID.

This gives the transfer function with the unknowns constants of PID:

$$Glc(s) = \frac{mKds^2 + mKps + mKi}{s^3 + (n + mKd)s^2 + (p + mKp)s + mKi}$$

But before matching the characteristic equations you must increase the degree of the second order characteristic equation in order to be able to match them, this is done by adding a remnant pole to the characteristic equation so as not affect the desired behavior, in this case 5 times away from the dominant poles, this modification usually affects the amplitude but the behavior of canonical system is preserved.

$$(s + 8000)(s^2 + 3200s + 2707^2)$$

Thus it is possible to do the coefficients matching:

$$(n + mKd) = 11200 \Rightarrow Kd = 0.0011245$$

$$(p + mKp) = 32929310 \Rightarrow Kp = 2.7162$$

$$(mKi = 5) = 863448e10 \Rightarrow Ki = 6709$$

Replacing these constants in the closed loop transfer function, then the simulation is performed with a step value of E volts.

In figure 6 you can see that the controlled system does not reach the desired overshoot but its normal to tune a little, it is advisable to do it when the controller is already modulated by the PWM and so avoid double tuning. The settling time and the steady-state error are the desired. The new root locus is shown in figure 7:

IV. Discrete time system

For a continuous time system the general solution is given by:

$$X(t) = e^{A(t-t_o)}X(0) + \int_{t_o}^{t} e^{A(t-\tau)}Bu(\tau)\,\mathrm{d}\tau$$

Therefore the solution in discrete time form is given by:

$$X(k+1)T = e^{AT}X(kT) + \int_{0}^{T} e^{A(T-\tau)}Bu(kT)\,\mathrm{d}\tau \quad (4)$$

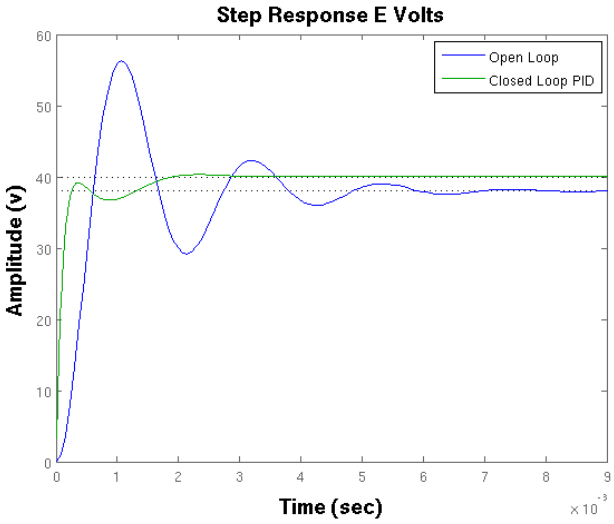

Figure 6. Comparison Open Loop and Closed Loop with PID

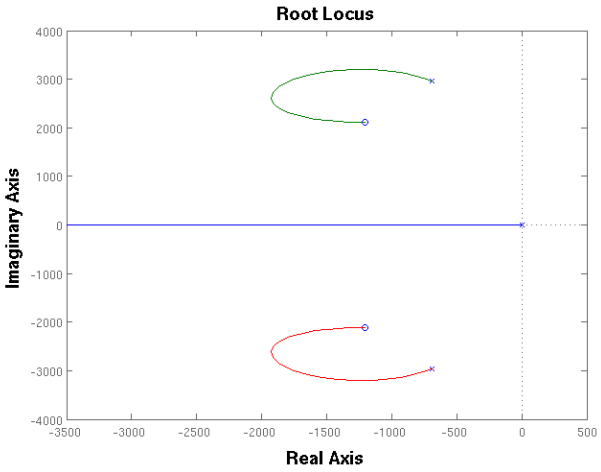

Figure 7. New Root Locus

The solution of equation 4 is obtained as:

$$X(k+1)T = e^{AT}X(kT) + (e^{AT} - I)A^{-1}Bu(kT)$$

Making $Ad = e^{AT}$ y $Bd = (e^{AT} - I)A^{-1}B$, the solution can be presented as:

$$Ad.X(kT) + Bd.u(kT) \tag{5}$$

Then, the solution of e^{AT} is:

$$\mathscr{L}^{-1}(SI - A)^{-1}$$

$$= \begin{pmatrix} \frac{s+d}{s^2+(a+d)s+(ad+bc)} & -\frac{b}{s^2+(a+d)s+(ad+bc)} \\ \frac{c}{s^2+(a+d)s+(ad+bc)} & \frac{s+a}{s^2+(a+d)s+(ad+bc)} \end{pmatrix} \tag{6}$$

From the equation 6 applying the Laplace's anti-transformation we obtain the matrix e^{AT}:

$$e^{AT} = \begin{pmatrix} Term2 + dTerm1 & -bTerm1 \\ cTerm1 & Term2 + aTerm1 \end{pmatrix} \tag{7}$$

Where:

$$Term1 = \frac{e^{-\zeta\omega_n t} sen(\omega_d t)}{\omega_d}$$

$$Term2 = -\frac{e^{-\zeta\omega_n t} sen(\omega_d t) - \phi}{\sqrt{1-\zeta^2}}$$

and:

$$\omega_d = \omega_n\sqrt{1-\zeta^2}$$

$$\phi = tan^{-1}\frac{\sqrt{1-\zeta^2}}{\zeta}$$

At this point you can probe that e^{AT} evaluated at $t = 0$ is equal to the identity matrix.

Knowing e^{AT} an algorithm was implemented in Matlab® to produce the discrete equivalent shown in figure 8.

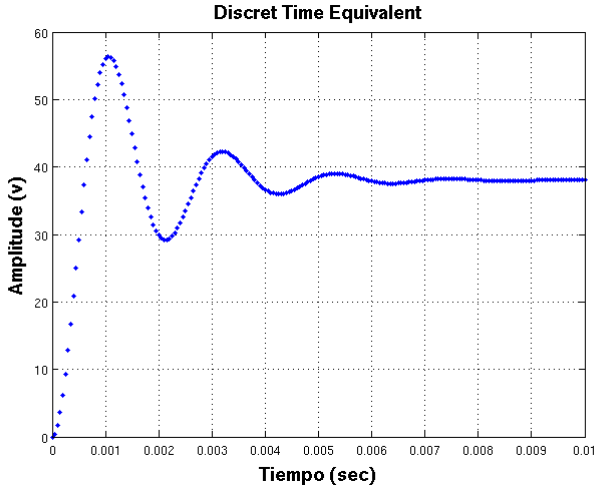

Figure 8. Discrete Time Equivalent

The continuous time system has a $Ts = 5.9ms$ so we can choose a sampling rate $T = 50\mu seg$. Initializing the necessary variables, you get the output shown in Figure 8. So you can see how the discrete equivalent is very close to the real equivalent.

V. PID MODULATED BY PWM

The found constants will be used in this controller. The essence of the PWM control is shown in the following implemented code in Matlab® which defines a duty cycle $D = (\frac{u}{Sat})T$ with $Sat = 40V$, changing t for D on equation 7 and calculating e^{AD} to get Xfin1, is also necessary to calculate $e^{A(t-D)}$ replacing t for $(t - D)$ to get Xfin2:

```
Ref=30; Kp=2.7162; Kd=0.001124; Ki=6709;

for i=1:200
    % It gets the error, that will change each iteration due to CondIni
    EdeK=Ref-C*CondIni
    % On each iteration it gets the control signal u
    u=(Kp*EdeK) + (Ki*(((EdeK+EdeKmen1)/2)*T) + Eacum) +
```

```
    (Kd*((EdeK - EdeKmen1)/T))

if (Eacum+Ki*(((EdeK+EdeKmen1)/2)*T) > E) % Anti Wind-Up
    Eacum=Eacum;
else
    % Error's integral addition
    Eacum=Eacum + Ki*(((EdeK+EdeKmen1)/2)*T);
end
% Control signal saturation
if (u > E)
    u=E;
else if (u < 0)
        u=0
    end
end

D=(u/E)*T; % Duty cicle definition.
% Calculation of eAd terms on each iteration
Term1=(1/Wd)*(exp(-Zeta*Wn*D)*sin(Wd*D));
Term2=(-1/(sqrt(1-Zeta^2)))*(exp(-Zeta*Wn*D)*sin(Wd*D - Phi));

eAD=[Term2+d*Term1 -b*Term1; c*Term1 Term2+a*Term1];
Bd=invA*(eAD-eye(2))*[(1/L);0];

% Generation and addition of the output signal in saturation mode
Xfin1=[Xfin1 eAD*CondIni+Bd*Sat];

% Calculation of the eA(T-D) terms
Term1=(1/Wd)*(exp(-Zeta*Wn*(T-D))*sin(Wd*(T-D)));
Term2=(-1/(sqrt(1-Zeta^2)))*(exp(-Zeta*Wn*(T-D))*sin(Wd*(T-D) - Phi));

eATmenD=[Term2+d*Term1 -b*Term1; c*Term1 Term2+a*Term1];
% Generation and addition of the output signal in off mode
Xfin2=[Xfin2 eATmenD*Xfin1(:,i+1)];

% Save the error to use it as previous point on next iteration
EdeKmen1=EdeK;
% inital conditions will be the last xfin2 values (off mode)
CondIni=Xfin2(:,i+1);
% Generation of a time vector to drawn
Tiempo=[Tiempo T*i];
```

Initializing variables and respective vectors to zero the output Xfin2 is obtained (V_C) (Load Voltage) shown in figure 9.

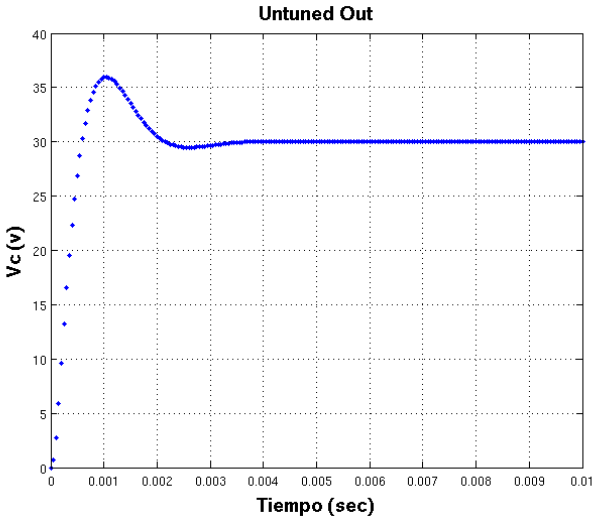

Figure 9. PID with PWM

We see then that the overshoot appears even higher than previously estimated, to reduce the overshoot you can follow the table I taken from [1], showing a online tuning form of PID, depending the output characteristics required by the user.

The use of this table is valid as long as the constants to tune are calculated with a known method. Therefore from the values that we have calculated, we reduce $Ki = 2400$ with which we get an overshoot close to zero as shown in Figure 10, which is very convenient for such converters.

Table I
EFFECTS OF INDEPENDENT P, I AND D TUNING

PID	Rise Time	Overshoot	Settling Time	Steady Stage Error	Stability
⇑Kp	Decrease	Increase	Small Increase	Decrease	Degrade
⇑Ki	Small Decrease	Increase	Increase	Large Decrease	Degrade
⇑Kd	Small Decrease	Decrease	Decrease	Minor Change	Improve

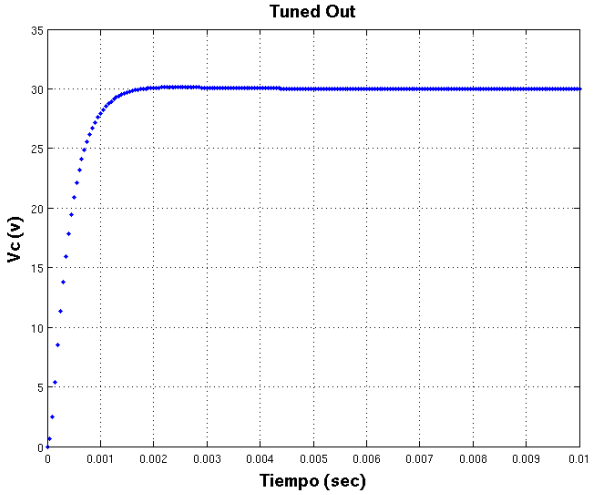

Figure 10. Tuned output (V_C) using Table I

VI. BIFURCATION DIAGRAMS

The bifurcation diagrams are defined as qualitative and quantitative variations of the system's dynamic in front of the variation of parameters, this can influence the stability of system and the characteristics at the output among other.

The bifurcation diagram is a tool for dynamic system analyzing and provides information on the stable operation limits of a dynamic system. For this system only the constant Kp has to be varied, since this affects the others.

This required the industrial form of PID.

$$PID = kp(1 + \frac{\tau_i}{s} + \tau_d s)$$

A. V_C and D Bifurcation Diagrams With Kp Variations

Figures 11 and 12, show that the operating range of Kp has an upper limit of 19 units apx, before the system becomes chaotic.

B. V_C and D Bifurcation Diagrams With T variations

Here you can see on figure 13 that for small values of T (sampling period) the system has a ONE periodic wave for high frequencies, but it begins to turn chaotic by increasing the

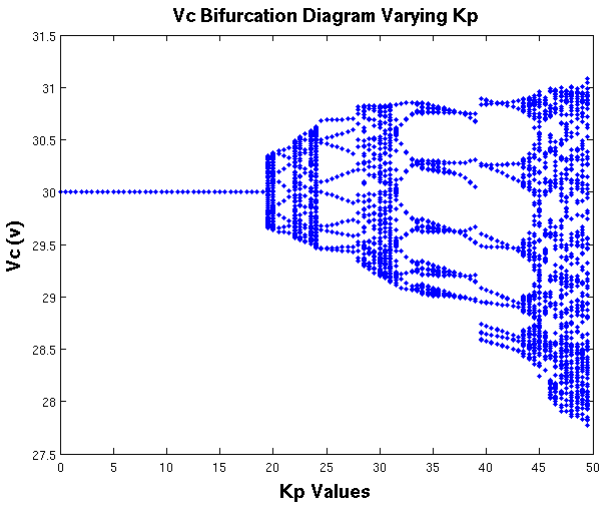

Figure 11. V_C's Bifurcations

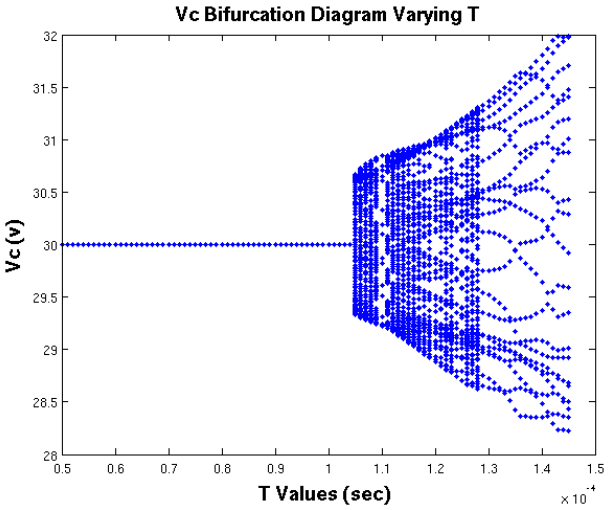

Figure 13. V_C's Bifurcation Diagram Varying T

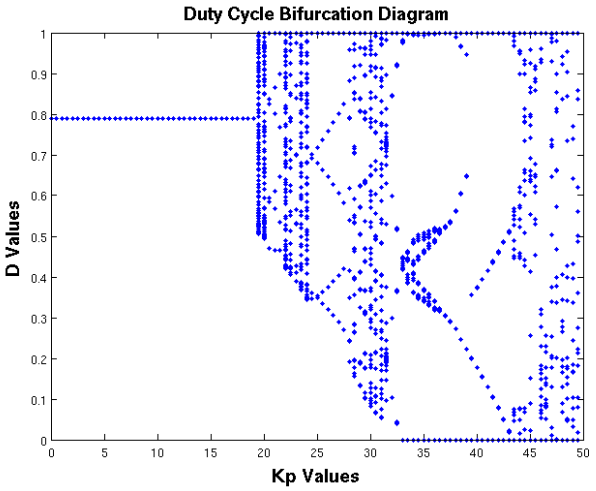

Figure 12. D's Bifurcations

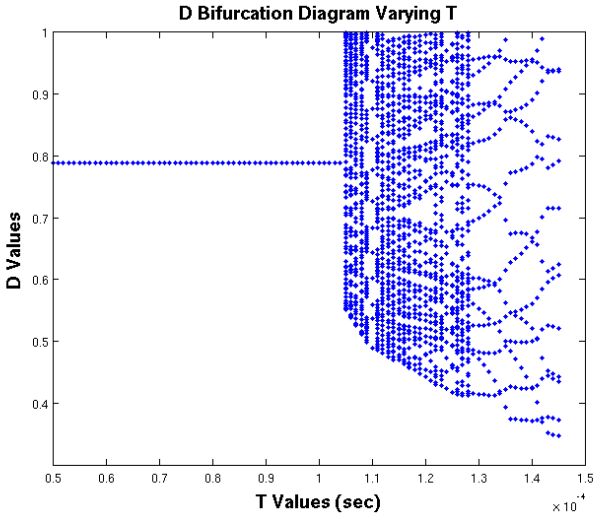

Figure 14. D's Bifurcation Diagram Varying T

sampling period that is equal to the switching period around $110\mu seg$.

VII. MATLAB/SIMULINK® SIMULATION

The next simulation performed in simulink get us closer to real time implementation performed in dSPACE, figures 15 and 16 show the circuit diagram and elements used:

In figure 17 you can see the output in open and closed loop. Reducing the sampling rate to half, the signal loses symmetry because it gets fewer sampling points and therefore the integration process begins to have problems because it adds more than needed or rests more than needed, for the same reason, that's why you can see those strong oscillations on figure 18. This effect is accentuated in the implementation.

VIII. EXPERIMENTAL RESULT

For the real-time implementation the control and development card dSPACE was used. The converter's PID controller was implemented in simulink, the program is shown in figure 19, it controls the controller implemented on hardware through the PWM generation block.

The results presented in this section were obtained with the experimental prototype and the parameters defined in table II.

Making changes of reference voltage on levels 10V, 20V and 30V, and varying the sampling and switching frequency, it shows that the real system is much more sensitive to a low sampling rate. Figure 20 corresponds to a sampling frequency of 10 kHz.

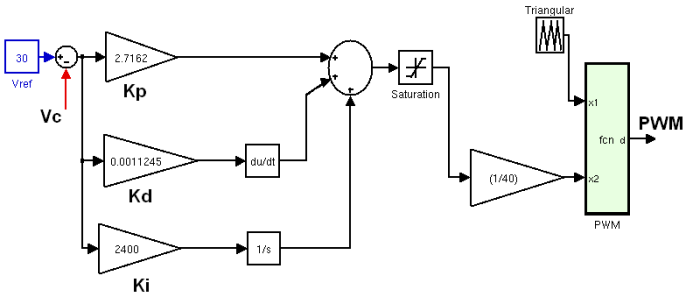

Figure 15. PID and PWM Schema

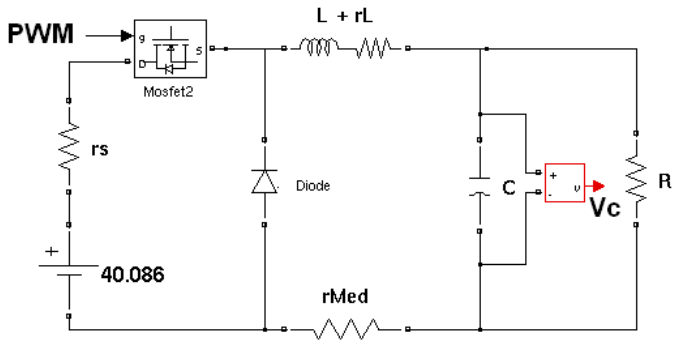

Figure 16. Buck Converter

If we increase the sampling frequency three time (30 kHz) in figure 20, it shows a little improvement in the regulated signal V_C and especially a reduction in the sound produced by the inductor due to the switching frequency growth of the transistor.

If we improve the converter's filtering by increasing significantly the value of the capacitor to $376\mu F$, we find a better answer with a lower steady-state error, even for the designed parameters shown in table II. The reason for this, is that, more capacity filters higher frequency and therefore the regulation is better, reducing considerably the system's chaos.

It can be seen in Figures 23 and 24 that if we make instant load changes going from 14.59Ω to 39.3Ω with a capacitor of $376\mu F$ and switching to 10 kHz, the system regulates too well with errors less than 2%, it shows that not only the good performance of the PID controller must be considered.

IX. Conclusions

Since the increased value of the capacitor produced a substantial improvement in the system, it is necessary to propose a detailed study of the buck converters on the market in order to determine which and what values of its elements are most appropriate to apply different control techniques and compare results. It is likely that the implemented converter has not the best features to adequately respond to PID control.

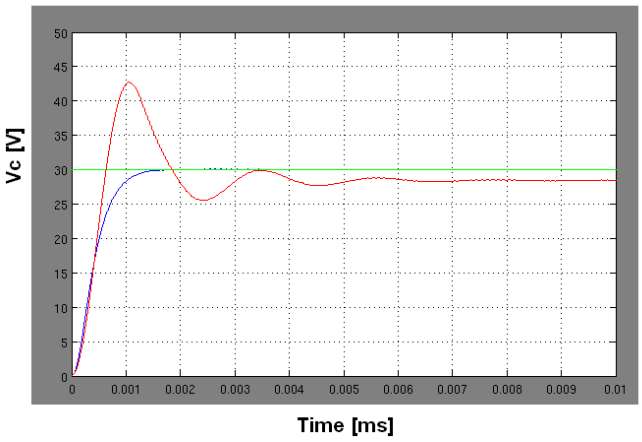

Figure 17. V_C output, open loop and closed loop with PID

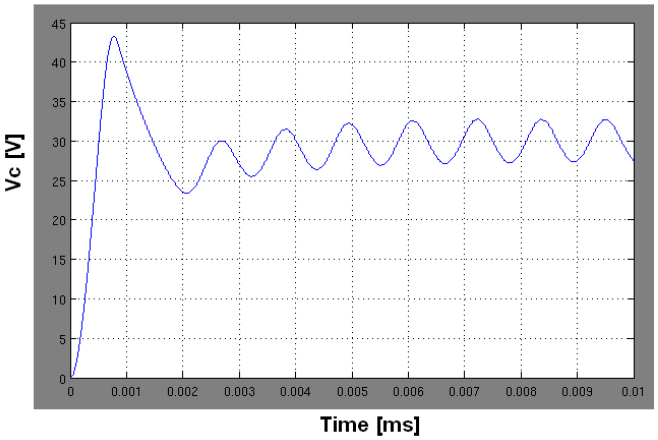

Figure 18. V_C output with a minor sample frequency

1) In some systems a continuous PID control can react in a way and when is modulated by PWM change substantially, so we shouldn't assume that what is found in continuous time, can apply without restrictions in discrete time.
2) The switching and sampling frequency affect in mayor proportion the integral because it needs to adds the higher possible amount of points to successfully complete the integration process.
3) Having a hardware that supports a high sampling and switching frequency is a very important factor when implementing a system.
4) For the implemented converter, the PID controller did not respond in the best way. It is necessary to filter or remove the derivative, and select an appropriate sampling and switching frequency.

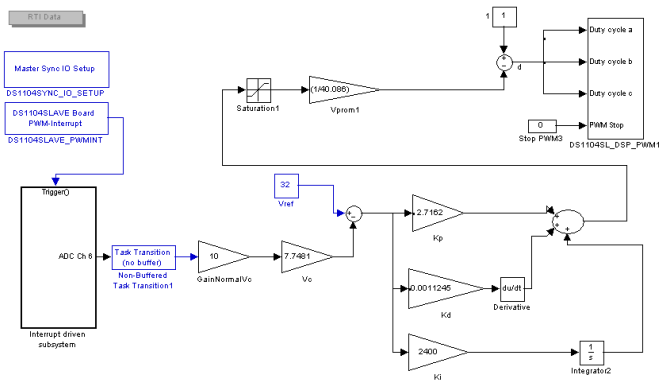

Figure 19. Rapid control prototyping to control the buck converter

Table II
EXPERIMENTAL PROTOTYPE DATA

	Parameter	Value
R:	Load resistance	39.3Ω
C:	Capacitance	46.27 and 376 μF
L:	Inductance	$2.473mH$
r_{int}:	Internal resistance of the source	0.688Ω
r_L:	Internal resistance of the inductor	1.345Ω
E:	Input voltage	$40.086V$
Fc:	Switching frequency	10 kHz and 30 kHz
Fs:	Sampling frequency	10 kHz and 30 kHz
Kp:	proportional gain	2.7162
Kd:	derivative gain	0.0011245
Ki:	integral gain	2400

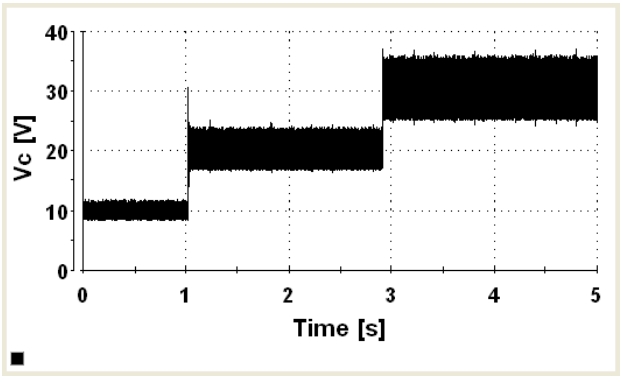

Figure 20. V_C output with C= 46μF Vc at 10 kHz

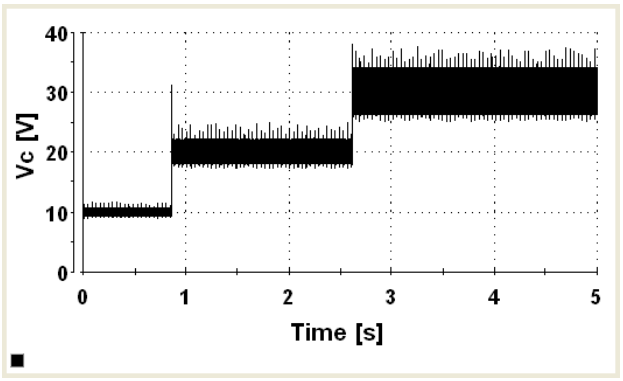

Figure 21. V_C output with C= 46μF Vc at 30 kHz

REFERENCES

[1] Gregory Chong. Kiam Heong Ang. and Yun Li. Pid control system analysis, design, and technology. *IEEE Transactions on control systems technology, Vol. 13, No. 4,*, July 2005.

[2] N. Mohan, T. Undeland, and W. Robbins. *Power Electronics: Converters. Aplications and Design*. J. Wiley, 1995.

[3] D. Hart. *Electrónica de Potencia.* Prentice Hall, Madrid, España, 2001.

[4] E. Fossas and G. Olivar. Study of chaos in the buck converter. *IEEE transactions on Circuits and Systems-I: Fundamental Theory and Applications*, 43:13–25, 1996.

[5] D.C Hamill, J.H.B. Deane, and D.J Jefferies. Modeling of chaotic dc-dc converters by iterated nonlinear mappings. *IEEE transactions on Power Electronics*, 7:25–36, 1992.

[6] G. Olivar. *Chaos in the Buck Converter. PhD thesis*. Universidad Politécnica de Cataluña. Spain, Available at: http://www.tdx.cat/handle/10803/5841, 1997.

[7] Yousefzadeh V. Haitao Hu. and Maksimovic D. Nonuniform a/d quantization for improved dynamic responses of digitally controlled dc–dc converters. *Power Electronics, IEEE Transactions on, Volume: 23 , Issue: 4, Page(s): 1998 - 2005*, 2008.

[8] Peterchev A.V. and Sanders S.R. Quantization resolution and limit cycling in digitally controlled pwm converters. *Power Electronics, IEEE Transactions on, Volume: 18 , Issue: 1 , Part: 2, Page(s): 301 - 308*, 2003.

[9] Prodic A. Hao P., Maksimovic D. and Alarcon E. Modeling of quantization effects in digitally controlled dc-dc converters. *Power Electronics, IEEE Transactions on, Volume: 18 , Issue: 1 , Part: 2, Page(s): 301 - 308*, 2003.

[10] Liu C.P. Fung C.W. and Pong M.H. A diagrammatic approach to search for minimum sampling frequency and quantization resolution for digital control of power converters. *Power Electronics Specialists Conference, 2007. IEEE, Page(s): 826 - 832,*, 2007.

[11] Zane R. Maksimovic D. and Erickson R. Impact of digital control in power electronics. *Power Semiconductor Devices and ICs, 2004. Proceedings. ISPSD '04. The 16th International Symposium on, Page(s): 13 - 22*, 2004.

[12] Maksimovic D. Prodic A. and Erickson R.W. Digital controller chip set for isolated dc power supplies. *Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE Volume: 2, Page(s): 866 - 872*, 2003.

[13] DeGusseme K. VandeSype D.M., VandenBossche A.P. DeBelie F.M.L.L., and Melkebeek J.A. Small-signal z-domain analysis of digitally controlled converters. *Power Electronics, IEEE Transactions on Volume: 21 , Issue: 2, Page(s): 470 - 478*, 2006.

[14] Maksimovic D. and Zane R. Small-signal discrete-time modeling of digitally controlled dc-dc converters. *Computers in Power Electronics, 2006. COMPEL '06. IEEE Workshops on, Page(s): 231 - 235*, 2006.

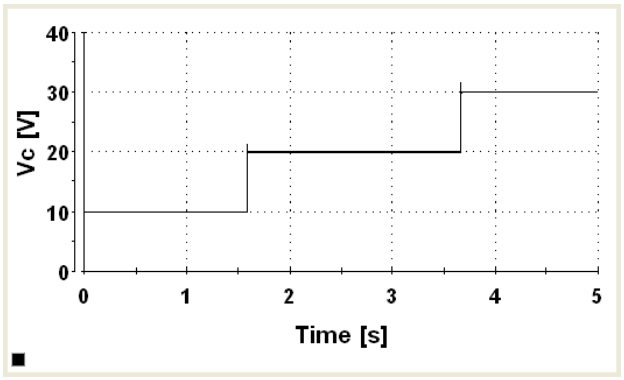

Figure 22. V_C out with C=376μF at 10 kHz

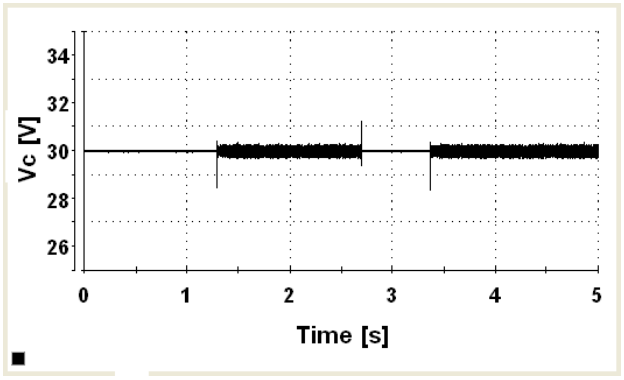

Figure 23. V_C output with load changes R with C=376μF

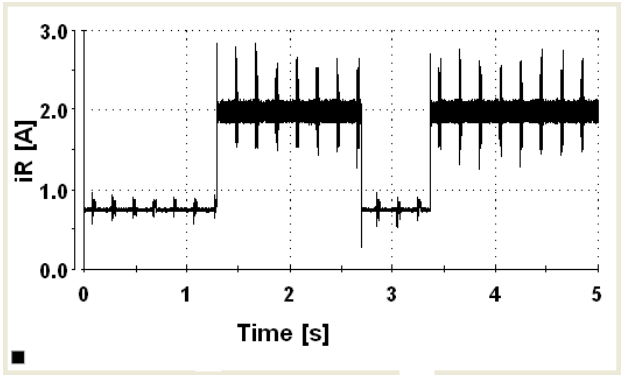

Figure 24. I load i_R with load changes R with C=376μF