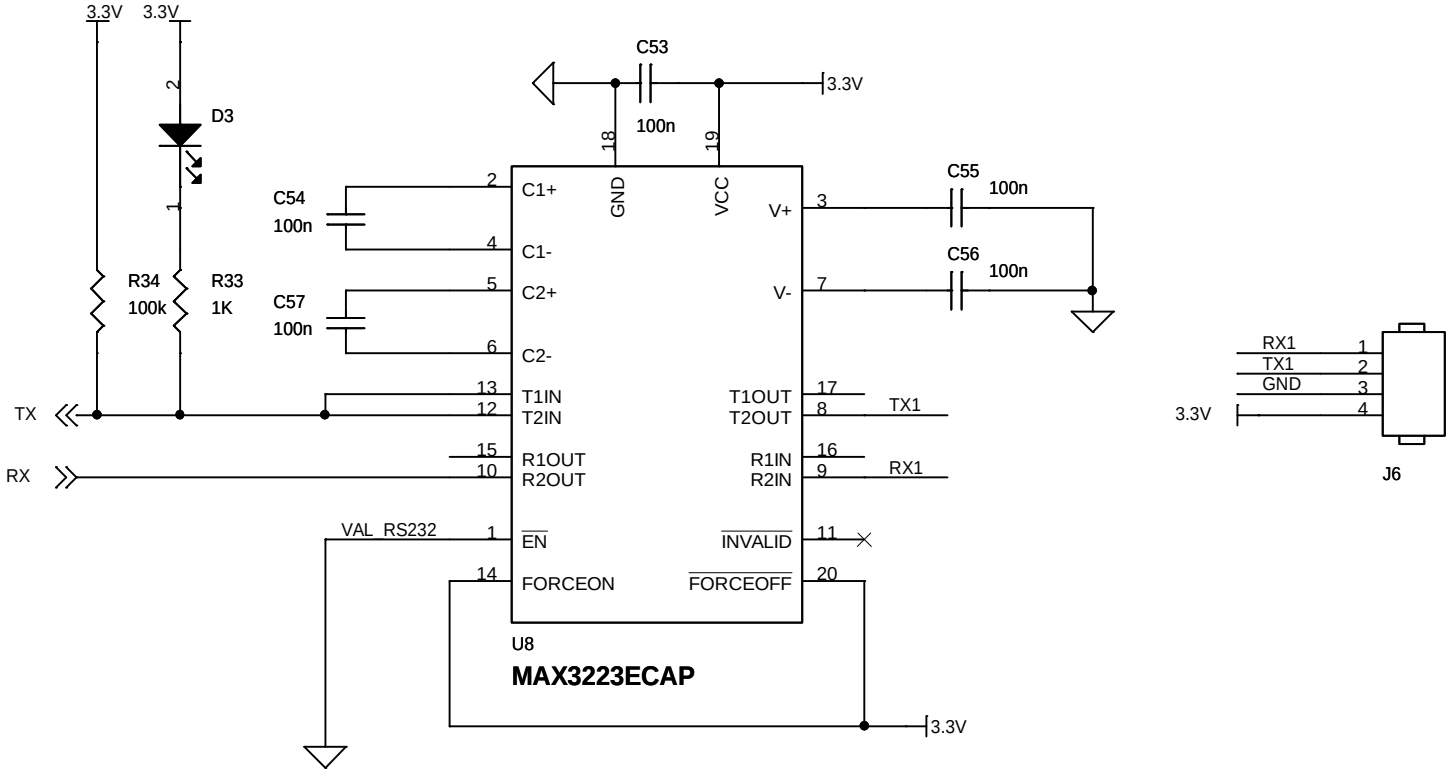
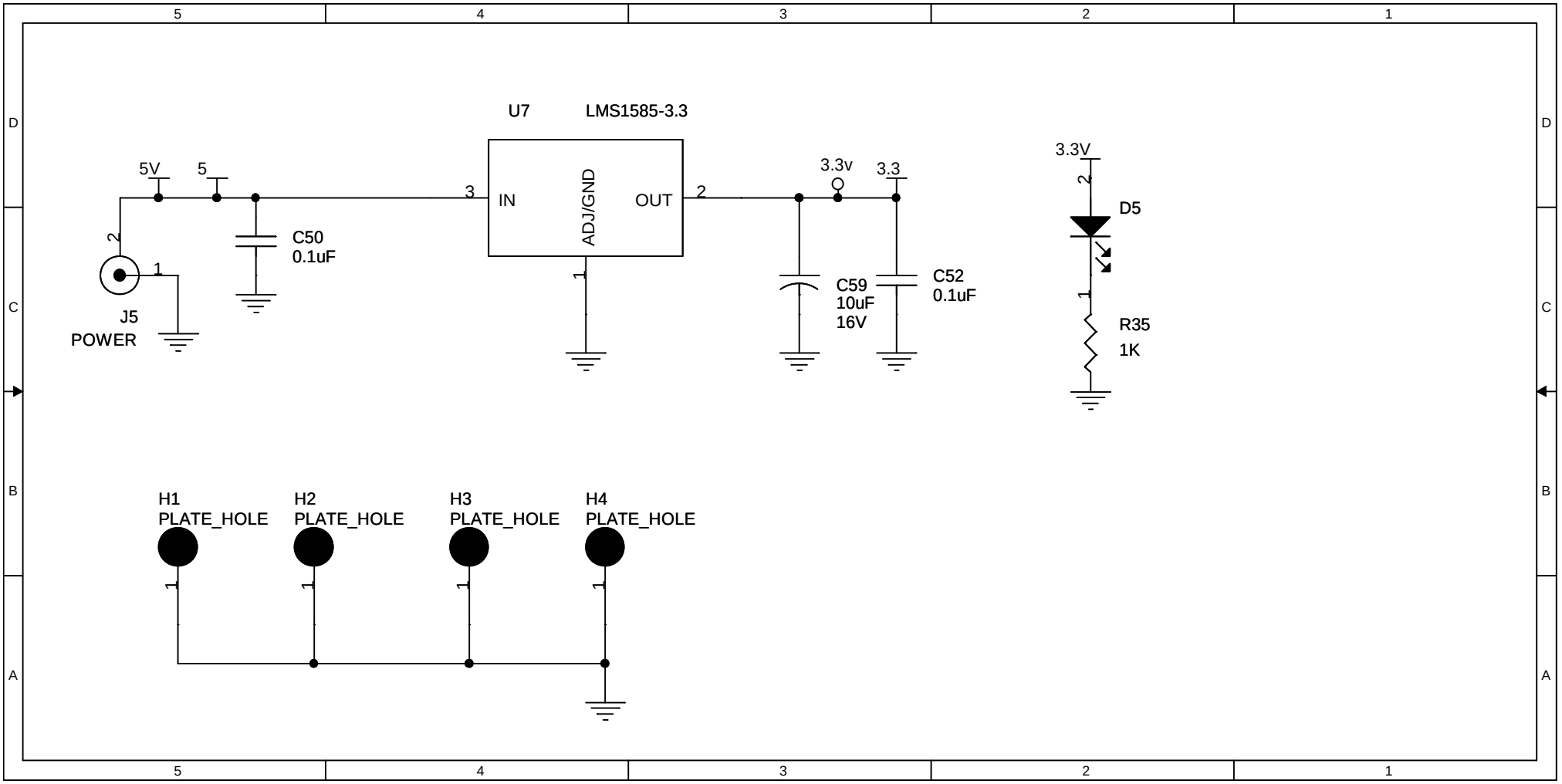
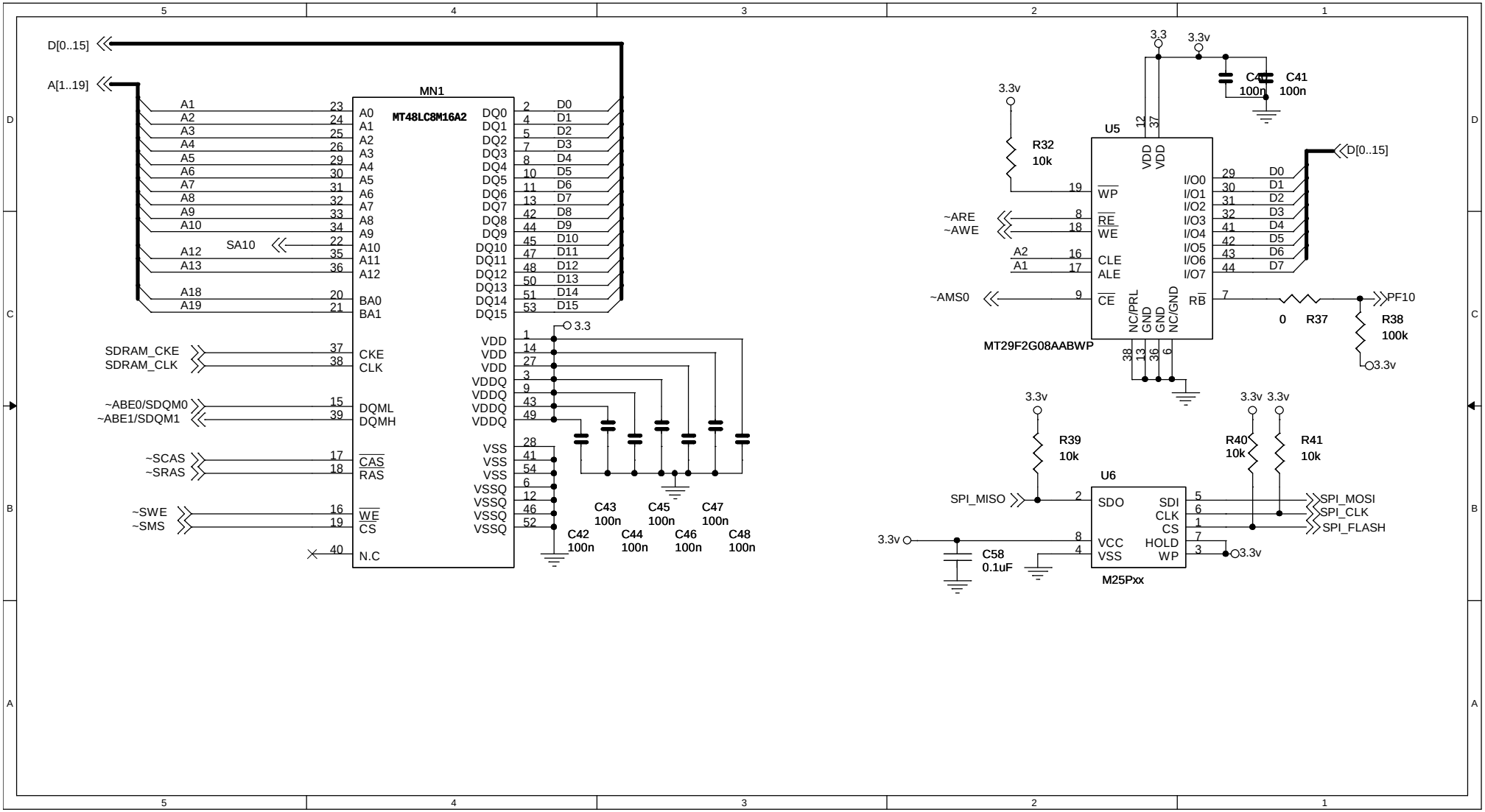
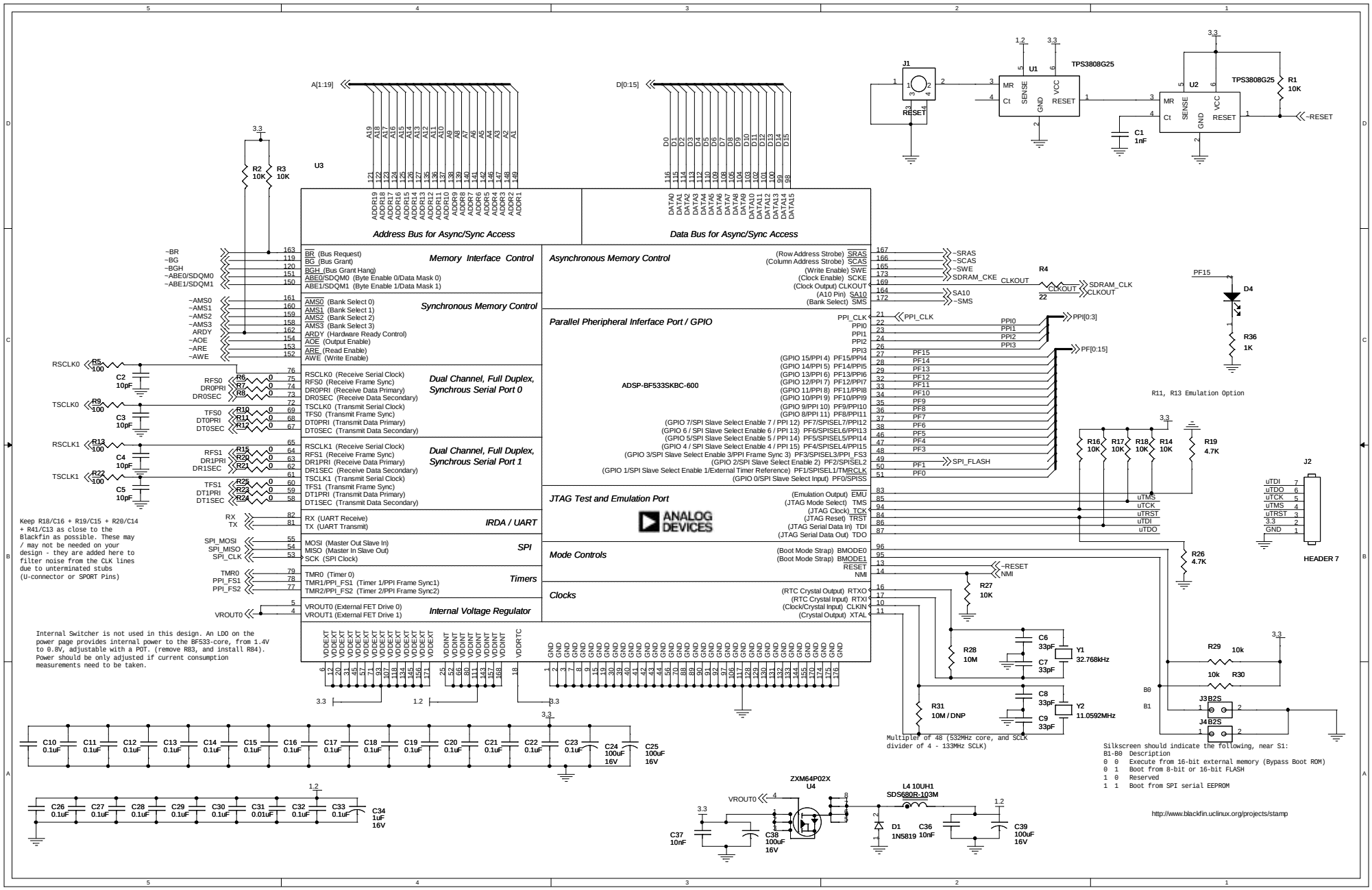
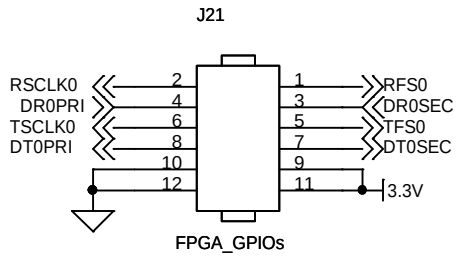
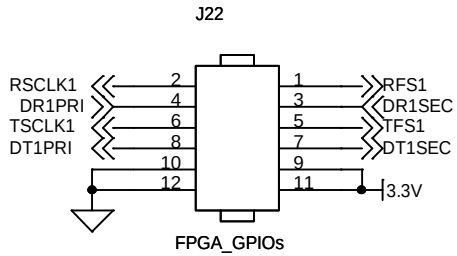

3.3V
3.3V
D3
R34
100k
R33
1K
C53
100n
3.3V
C54
100n
C57
100n
C55
100n
C56
100n
C1+
C1-
C2+
C2-
GND
VCC
V+
V-
T1IN
T2IN
R1OUT
R2OUT
EN
FORCEON
T1OUT
T2OUT
R1IN
R2IN
INVALID
FORCEOFF
TX
RX
TX1
RX1
VAL_RS232
U8
MAX3223ECAP
3.3V
RX1
TX1
GND
3.3V
J6

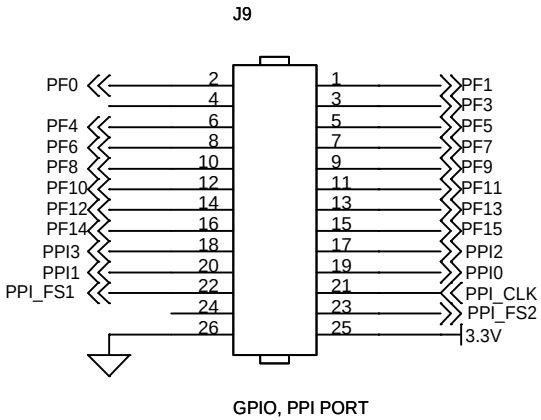

U7
LMS1585-3.3
IN
ADJ/GND
OUT
5V
5
C50
0.1uF
J5
POWER
3.3v
3.3
C59
10uF
16V
C52
0.1uF
3.3V
D5
R35
1K
H1
PLATE_HOLE
H2
PLATE_HOLE
H3
PLATE_HOLE
H4
PLATE_HOLE

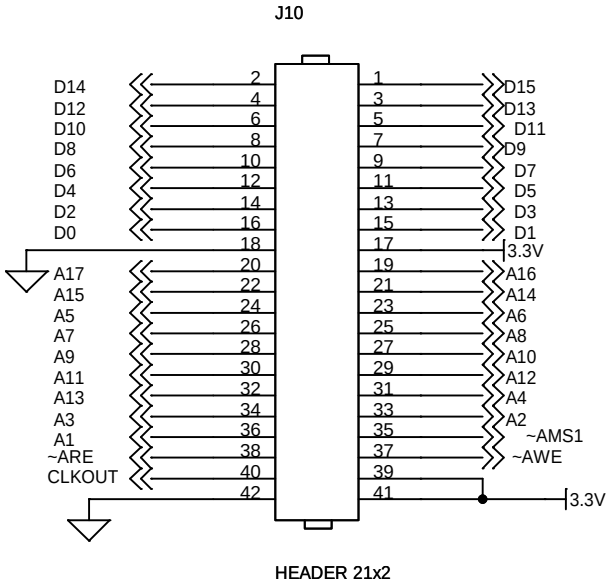

D[0..15]
A[1..19]
MN1
MT48LC8M16A2
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12
BA0 BA1
CKE CLK
DQML DQMH
CAS RAS
WE CS
N.C
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
VDD VDDQ VSS VSSQ
SA10
SDRAM_CKE
SDRAM_CLK
~ABE0/SDQM0
~ABE1/SDQM1
~SCAS
~SRAS
~SWE
~SMS
3.3
C42 100n
C43 100n
C44 100n
C45 100n
C46 100n
C47 100n
C48 100n
3.3v
R32 10k
U5
MT29F2G08AABWP
WP RE WE CLE ALE CE RB
I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7
VDD VDD
NC/PRL GND GND NC/GND
~ARE
~AWE
A2
A1
~AMS0
C40 100n
C41 100n
0 R37
R38 100k
PF10
R39 10k
U6
M25Pxx
SDO SDI CLK CS HOLD WP VCC VSS
SPI_MISO
SPI_MOSI
SPI_CLK
SPI_FLASH
R40 10k
R41 10k
C58 0.1uF

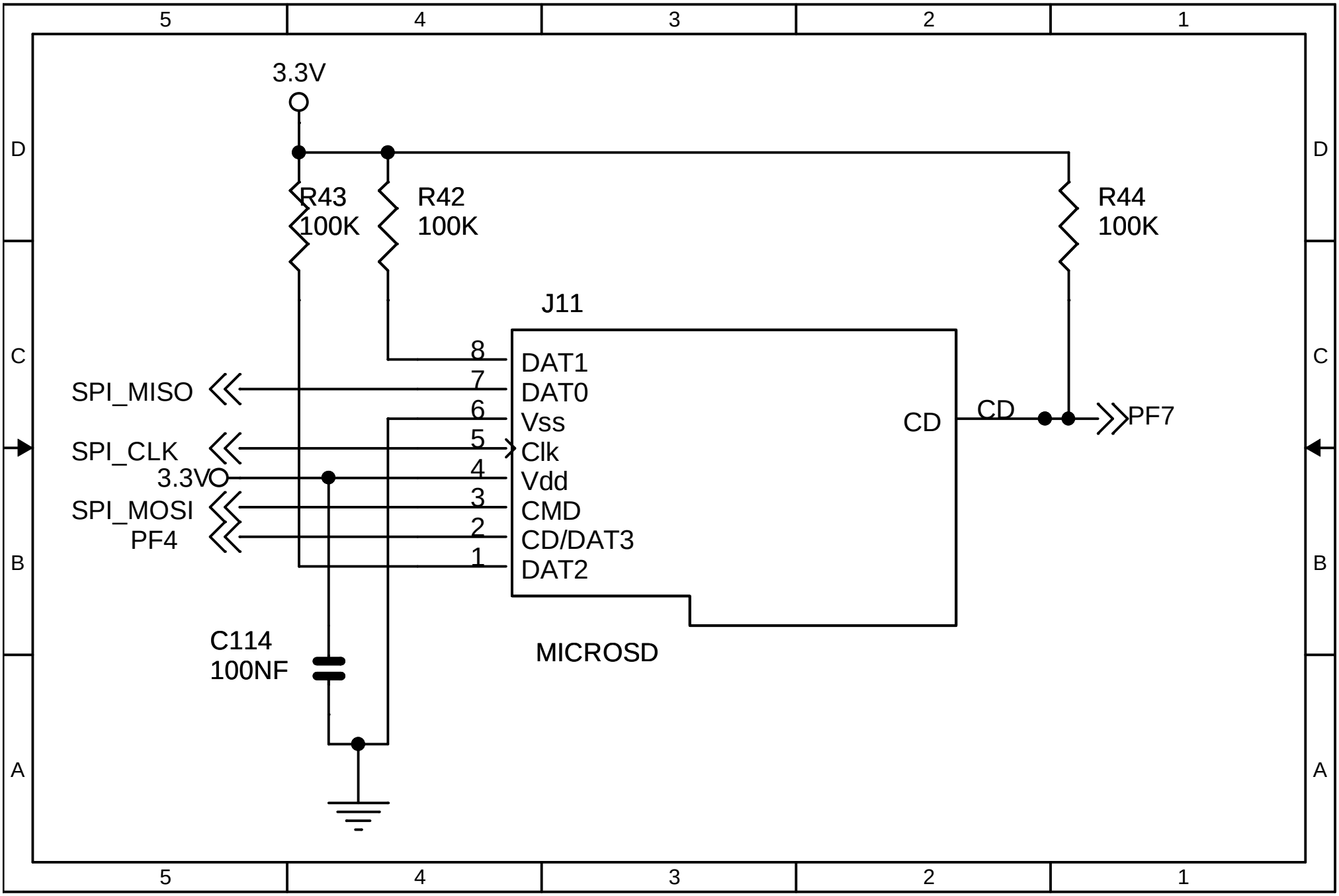

U3
ADSP-BF533SKBC-600
Address Bus for Async/Sync Access
Data Bus for Async/Sync Access
Memory Interface Control
Synchronous Memory Control
Dual Channel, Full Duplex, Synchrous Serial Port 0
Dual Channel, Full Duplex, Synchrous Serial Port 1
IRDA / UART
SPI
Timers
Internal Voltage Regulator
Asynchronous Memory Control
Parallel Pheripheral Inferface Port / GPIO
JTAG Test and Emulation Port
Mode Controls
Clocks
ANALOG DEVICES
J1
RESET
U1
TPS3808G25
U2
TPS3808G25
R1 10K
C1 1nF
R2 10K
R3 10K
R4
22
D4
R36 1K
R11, R13 Emulation Option
R16 10K
R17 10K
R18 10K
R14 10K
R19 4.7K
R26 4.7K
J2
HEADER 7
R27 10K
R28 10M
R31 10M / DNP
Multiplier of 48 (532MHz core, and SCLK divider of 4 - 133MHz SCLK)
Y1 32.768kHz
Y2 11.0592MHz
R29 10k
R30 10k
J3 B2S
J4 B2S
Silkscreen should indicate the following, near S1:
B1-B0 Description
0 0 Execute from 16-bit external memory (Bypass Boot ROM)
0 1 Boot from 8-bit or 16-bit FLASH
1 0 Reserved
1 1 Boot from SPI serial EEPROM
http://www.blackfin.uclinux.org/projects/stamp
Keep R18/C16 + R19/C15 + R20/C14 + R41/C13 as close to the Blackfin as possible. These may / may not be needed on your design - they are added here to filter noise from the CLK lines due to unterminated stubs (U-connector or SPORT Pins)
Internal Switcher is not used in this design. An LDO on the power page provides internal power to the BF533-core, from 1.4V to 0.8V, adjustable with a POT. (remove R83, and install R84). Power should be only adjusted if current consumption measurements need to be taken.
ZXM64P02X
U4
L4 10UH1
SDS680R-103M
D1 1N5819
C37 10nF
C38 100uF 16V
C36 10nF
C39 100uF 16V
C10 0.1uF
C11 0.1uF
C12 0.1uF
C13 0.1uF
C14 0.1uF
C15 0.1uF
C16 0.1uF
C17 0.1uF
C18 0.1uF
C19 0.1uF
C20 0.1uF
C21 0.1uF
C22 0.1uF
C23 0.1uF
C24 100uF 16V
C25 100uF 16V
C26 0.1uF
C27 0.1uF
C28 0.1uF
C29 0.1uF
C30 0.1uF
C31 0.01uF
C32 0.1uF
C33 0.1uF
C34 1uF 16V

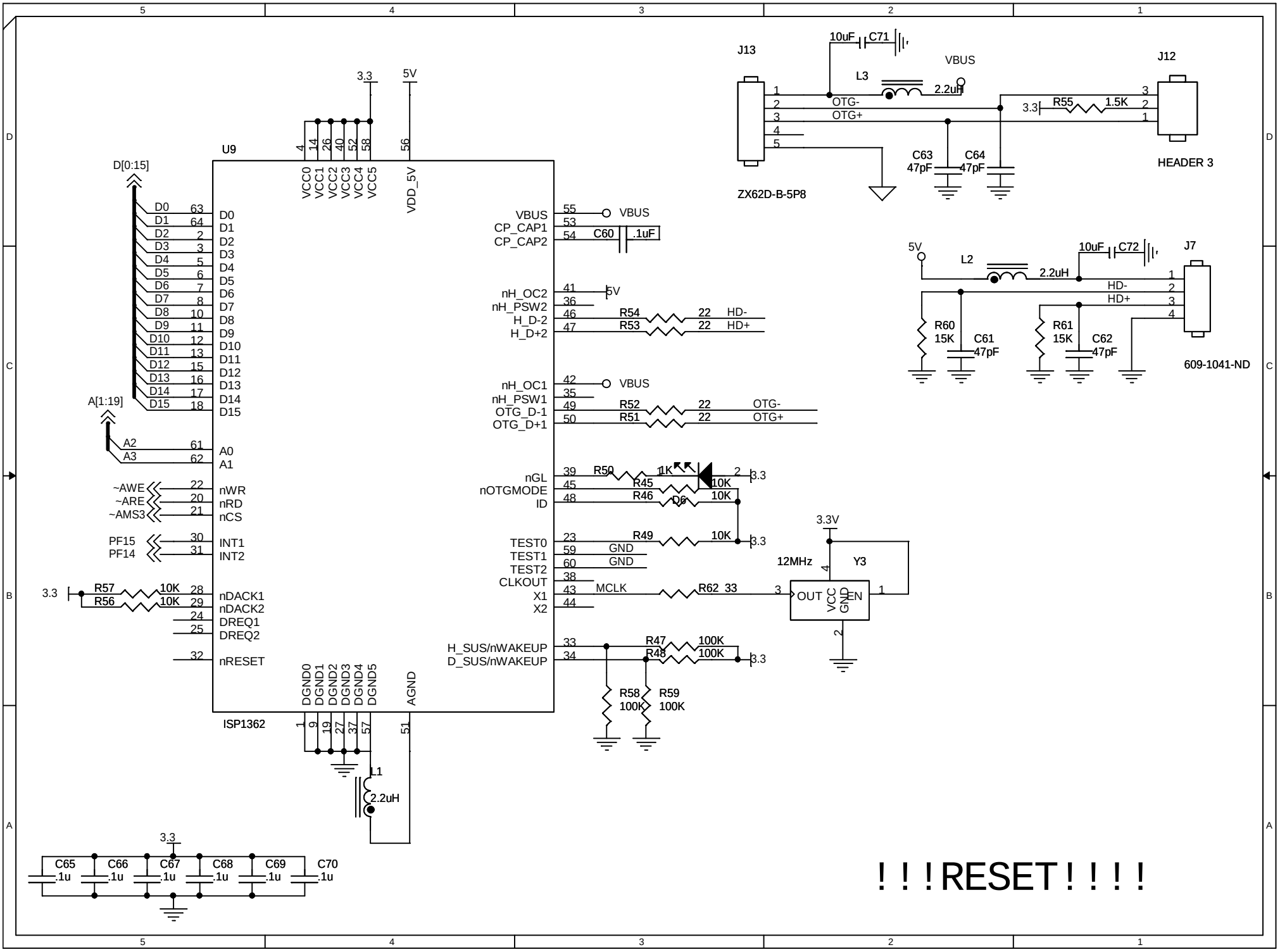

J21
RSCLK0
DR0PRI
TSCLK0
DT0PRI
2
4
6
8
10
12
1
3
5
7
9
11
RFS0
DR0SEC
TFS0
DT0SEC
3.3V
FPGA_GPIOs


J22
RSCLK1
DR1PRI
TSCLK1
DT1PRI
2
4
6
8
10
12
1
3
5
7
9
11
RFS1
DR1SEC
TFS1
DT1SEC
3.3V
FPGA_GPIOs


J9
PF0
PF4
PF6
PF8
PF10
PF12
PF14
PPI3
PPI1
PPI_FS1
2
4
6
8
10
12
14
16
18
20
22
24
26
1
3
5
7
9
11
13
15
17
19
21
23
25
PF1
PF3
PF5
PF7
PF9
PF11
PF13
PF15
PPI2
PPI0
PPI_CLK
PPI_FS2
3.3V
GPIO, PPI PORT


J10
D14
D12
D10
D8
D6
D4
D2
D0
A17
A15
A5
A7
A9
A11
A13
A3
A1
~ARE
CLKOUT
2
4
6
8
10
12
14
16
18
20
22
24
26
28
30
32
34
36
38
40
42
1
3
5
7
9
11
13
15
17
19
21
23
25
27
29
31
33
35
37
39
41
D15
D13
D11
D9
D7
D5
D3
D1
3.3V
A16
A14
A6
A8
A10
A12
A4
A2
~AMS1
~AWE
3.3V
HEADER 21x2


3.3V
R43
100K
R42
100K
R44
100K
J11
8
7
6
5
4
3
2
1
DAT1
DAT0
Vss
Clk
Vdd
CMD
CD/DAT3
DAT2
CD
CD
PF7
SPI_MISO
SPI_CLK
3.3V
SPI_MOSI
PF4
C114
100NF
MICROSD


U9
ISP1362
D[0:15]
A[1:19]
3.3
5V
VCC0 VCC1 VCC2 VCC3 VCC4 VCC5
VDD_5V
DGND0 DGND1 DGND2 DGND3 DGND4 DGND5
AGND
VBUS
CP_CAP1
CP_CAP2
C60 .1uF
nH_OC2
nH_PSW2
H_D-2
H_D+2
R54 22 HD-
R53 22 HD+
nH_OC1
nH_PSW1
OTG_D-1
OTG_D+1
R52 22 OTG-
R51 22 OTG+
nGL
nOTGMODE
ID
R50 1K
R45 10K
R46 10K
D6
R49 10K
TEST0
TEST1
TEST2
CLKOUT
X1
X2
GND
MCLK
R62 33
H_SUS/nWAKEUP
D_SUS/nWAKEUP
R47 100K
R48 100K
R58 100K
R59 100K
~AWE
~ARE
~AMS3
nWR
nRD
nCS
PF15
PF14
INT1
INT2
R57 10K
R56 10K
nDACK1
nDACK2
DREQ1
DREQ2
nRESET
L1 2.2uH
C65 .1u
C66 .1u
C67 .1u
C68 .1u
C69 .1u
C70 .1u
J13
ZX62D-B-5P8
10uF C71
L3 2.2uH
OTG-
OTG+
C63 47pF
C64 47pF
R55 1.5K
J12
HEADER 3
L2 2.2uH
10uF C72
J7
HD-
HD+
R60 15K
C61 47pF
R61 15K
C62 47pF
609-1041-ND
3.3V
12MHz
Y3
OUT
VCC
GND
EN
! ! ! RESET ! ! ! !