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Interfacing TFT LCD Panels to ADSP-BF533 Blackfin® Processors via PPI

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Introduction

ADSP-BF533 Blackfin® processors (and derivative devices such as ADSP-BF531 and ADSP-BF532 processors) have a Parallel Peripheral Interface (PPI) that allows up to 16 bits of data to be received or transmitted for every PPI clock. With the PPI, the ADSP-BF531/BF532/BF533 processors provide a glueless interface to any TFT LCD panel that accepts RGB data inputs.

This EE-Note describes the Blackfin hardware and software interface to connect to and drive the LCD panel. The focus is on the hardware and software setup. As such, a simple color bar example code is used to simplify the discussion.

Hardware Interface

The hardware used in this specific implementation of the Blackfin-to-LCD interface is as follows:

- ADSP-BF533 EZ-KIT Lite™ board
- ADSP-BF53x EZ-Extender 1 board
- SHARP LQ058T5DRQ1 (LCD panel)
- Microsemi LXM1614-14-11 (backlight inverter)
- Parlex Corporation 050-32-76BO (LCD panel to EZ-Extender board cable)

The selection of the LCD panel, backlight inverter module, and cable manufacturer are arbitrary and are not the only parts that can interface to the ADSP-BF533 processor's PPI port.

Hardware Connections

The LCD connector on the EZ-Extender board provides a simple interface to the LCD panel. This connector brings out the 16 PPI data lines, the three frame syncs, and the clock. The Parlex cable provides the connection between the LCD connector on the EZ-Extender board and the data/frame syncs input connector on the LCD panel.

Typically, TFT LCD panels will have a backlight lamp that provides the brightness to the LCD. The lamp on the SHARP LCD panel used in this application is a single, edge-driven type with a single Cold Cathode Fluorescent Tube (CCFT).

A separate backlight module is needed to drive the CCFT lamp on the back of the panel. For this specific application, the backlight module chosen is a Microsemi Cold Cathode Fluorescent Lamp (CCFL) Inverter Module. Check the data sheet of your inverter module to ensure that it is compatible with your LCD panel.

In turn, the backlight module needs to be powered via an external supply. For this particular backlight module, the required input voltage ranges from 9V to 16V. Check the data sheet of your inverter module for the required input power supply.

A block diagram of the hardware connections can be found in Figure 2 at the end of this EE-Note.

Software Interface

To successfully display color data and images on the LCD panel, the Blackfin processor must be properly configured.

ADSP-BF53x EZ-Extender

To provide maximum flexibility, the EZ-Extender board allows different sources to supply the PPI clock (an external input pin to the ADSP-BF533). In this particular application, a 25 MHz oscillator is used to drive the PPI clock pin. Through software, the EZ-Extender board is configured to accept the on-board oscillator as the PPI's input clock. The oscillator is selected when one of the flash's I/O pin (see schematics) is set. The asynchronous memory control registers must first be initialized to access the flash. In the source code provided with this EE-Note, the function that implements this configuration is called "Setup_ExtenderBoard".

Direct Memory Access (DMA)

The DMA controller provides a channel for data to be transferred between memories or between memory and DMA-capable peripherals. For this application, data transfers are needed between memory and the PPI (a DMA-capable peripheral). The different registers for which the DMA engine needs to be configured are:

- Starting Address register: This parameter specifies where in memory the DMA engine starts transferring from (for transmit operations). For this application, the data to be transmitted is placed at the start of SDRAM memory (address 0x0000).
- Count registers: The number of words the DMA engine should transfer. Since the DMA engine can transmit word sizes of 8 or 16 bits to the PPI, this specific application uses a DMA word size of 16 bits to match the bus width of the LCD panel. Therefore, "word" is used interchangeably with "pixel" for this application. The total number of words in an LCD frame is 640 pixels * 350 lines.
- Modify registers: The number of bytes by which to increment the address after each word transfer. For this application, the number of bytes by which to modify is 2, because each word is 16 bits (2 bytes) wide.
- Configuration register: This register specifies the DMA mode of operation and other details of the DMA transfer. For this application, the DMA is set to transmit data in autobuffer mode and perform a 2-D transfer of 16-bit words.

In the source code provided for this application, the function that configures the DMA controller is called "Setup_DMA_Tx."

Parallel Peripheral Interface (PPI)

The PPI provides a parallel port to which external devices (such as an LCD) can interface easily. It is a bi-directional port that can receive or transmit up to 16 bits of data.

The PPI supports two modes of operation: general-purpose (GP) and ITU-R 656. Because the LCD panel does not accept embedded frame syncs in its data stream, this application operates the PPI in general-purpose mode.

The different registers for which the PPI must be configured include the following:

- Configuration register: This register provides flexibility in specifying the PPI's mode of operation. For this application, the PPI is set to 16-bit data length, 2 frame syncs output mode, and inversion of both frame syncs 1 and 2.
- Delay register: This register sets the number of PPI clock cycles to delay after the assertion of frame sync 1 and before transmitting data out of the port. For this

application, this register is programmed to a value of 120. This is a requirement specified by this particular LCD panel's datasheet. This value may differ among LCD panels. Check your panel's data sheet to determine the appropriate value for this register.

- Count register: This register specifies the number of words to transmit per line, minus one. For this application, there are 640 active pixels per line. Therefore, the value programmed to this register is 639.

In the source code provided for this application, the function that configures the PPI port is called "Setup_PPI_Tx".

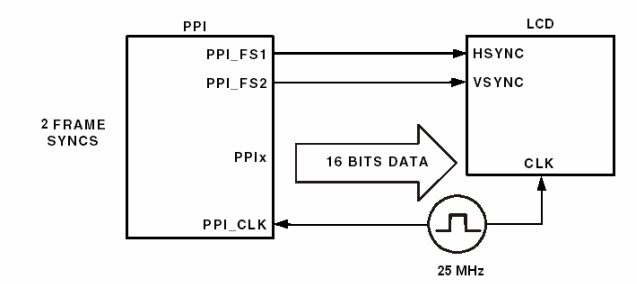

Figure 1. PPI 2 Frame Syncs Output Mode Connection

Timers

When using the PPI in 2 frame syncs mode, the TMR1 and TMR2 (Timer 1 and 2) pins become PPI_FS1 and PPI_FS2 (PPI Frame Sync 1 and 2), respectively. If the PPI is set to transmit, the timers must be configured to produce the required output frame sync pulse waveform.

Generally, in video applications, frame sync 1 represents the horizontal sync (HSYNC) signal, and frame sync 2 represents the vertical sync (VSYNC) signal.

For this application, the LCD panel requires a specific period and width for HSYNC and VSYNC. The timers are configured to meet this requirement. Different LCD panels may have different HSYNC and VSYNC timing requirements. Check your LCD panel's data sheet for the appropriate values to configure your HSYNC and VSYNC waveforms.

The three timer registers that need to be configured are:

- Timer Period registers: Sets the period of the generated waveform.
- Timer Width registers: Sets the width of the generated waveform.
- Timer Configuration registers: Specify a timer's mode of operation. For this application, the timers are set to PWM_OUT mode, a negative action pulse (to match the PPI's inverted frame sync selection), and selection of the PWM_CLK clock source to clock the timer's counter.

In the source code provided for this application, the function that configures the timers is called "Setup_Timers".

References

[1] *ADSP-BF533 Blackfin Processor Hardware Reference.* Rev 1.0, December 2003. Analog Devices, Inc.

[2] *ADSP-BF531/ADSP-BF532/ADSP-BF533 Blackfin Embedded Processor Preliminary Data Sheet.* Rev. PrC, January 2004. Analog Devices, Inc.

[3] *ADSP-BF533 EZ-KIT Lite Evaluation System Manual.* Rev. 1.0, Analog Devices, Inc.

[4] *ADSP-BF53x EZ-Extender 1 Manual.* Rev. 1.1, October 2003. Analog Devices, Inc.

[5] *SHARP LQ058T5DRQ1 TFT-LCD Module Technical Literature.* Spec. Issue Date: April 2, 2001.

[6] *Microsemi Single Lamp CCFL Inverter Module LXM1614-14-11 Data sheet.* Rev. 0.5b.

Appendix

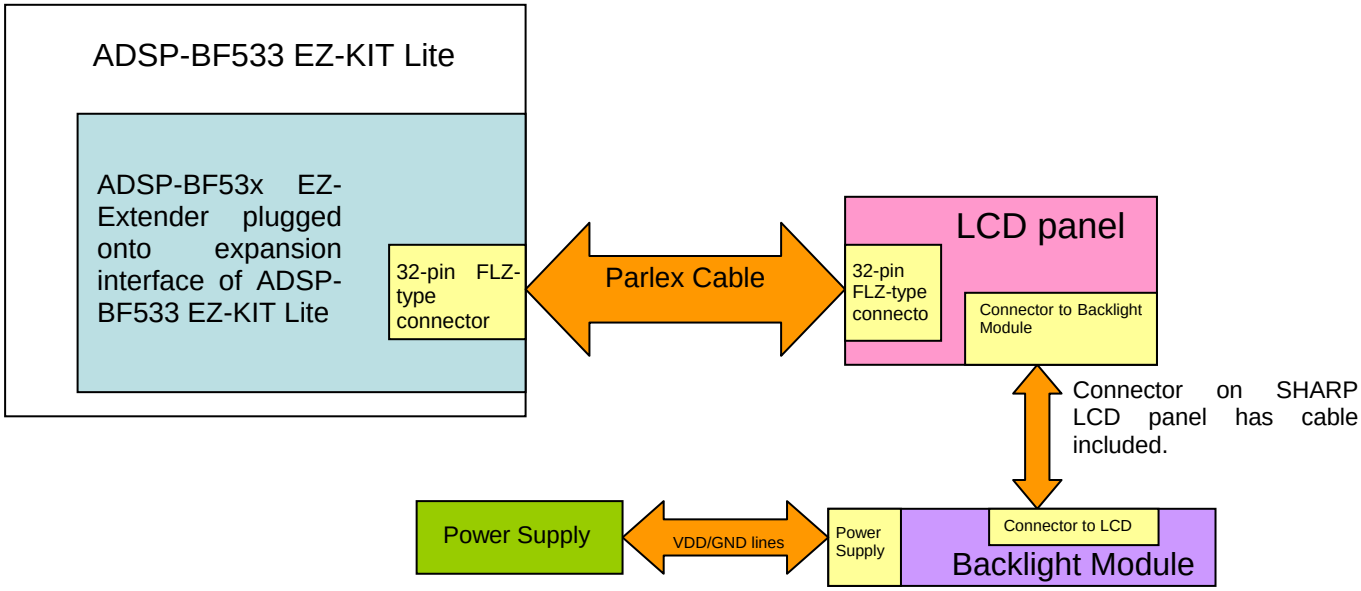

Figure 2. Block Diagram of Hardware Connections

Document History

Version	Description
Rev 1 – April 16, 2004 by C. Lam	Initial Release