What happens if multiple devices request for hot-join at a time?

If multiple Hot-Joining Targets become eligible at the same time, then they could all attempt to emit the Hot-Join Request together (i.e., at the same time). This could apply to Hot-Joining Targets using any combination of standard or passive Hot-Join methods.

In the case where multiple Hot-Joining Targets successfully emit the Hot-Join Request at the same time, it would not be necessary for each of these eligible Targets to emit separate Hot-Join Requests in succession with delays between each request. If a Hot-Join Request was successfully emitted, and if the Active Controller responds to that Hot-Join Request, then each such Target shall participate in a subsequent Dynamic Address Assignment procedure with ENTDAA that would be initiated by the Active Controller.

I3C

Presentation 3

Acronyms

- HDR : High Data Rate
- HDR-DDR : HDR Double Data Rate
- HDR-BT : HDR Bulk Transport
- ML : Multi-Lane
- CCC : Common Command Code
- CRC : Cyclic Redundancy Check
- FE : Flow Elements / Common Flow Elements
- SCL : Serial Clock
- SDA : Serial Data

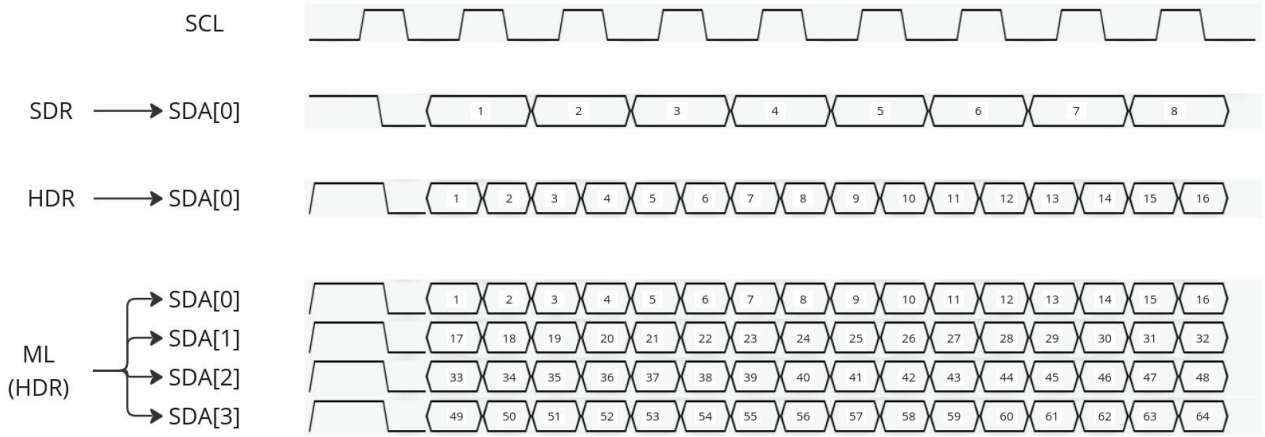
Index

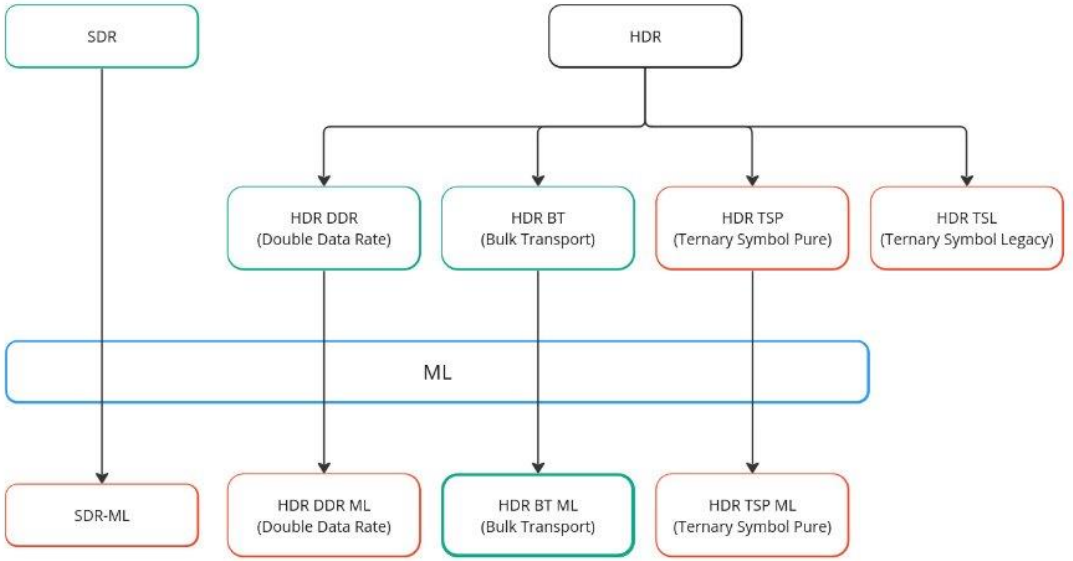
- Common HDR details.
- Basic HDR CCC transaction.
- HDR Patterns.
- CCC's support in HDR mode.
- Common Flow Elements (FE).
- Overview of HDR DDR and HDR BT features.
- Packet frames in HDR DDR and HDR BT.
- Relation between Common Flow Elements and Per mode HDR elements.
- Flow and Error Control in HDR DDR and BT.
- Performance measure HDR DDR and HDR BT.
- Introduction to Multi Lane transfers.
- Coding and Additional Data lanes.
- Schematics for coding and additional data lanes.

Is it possible to get higher data rate at same clock frequency ?

Solution

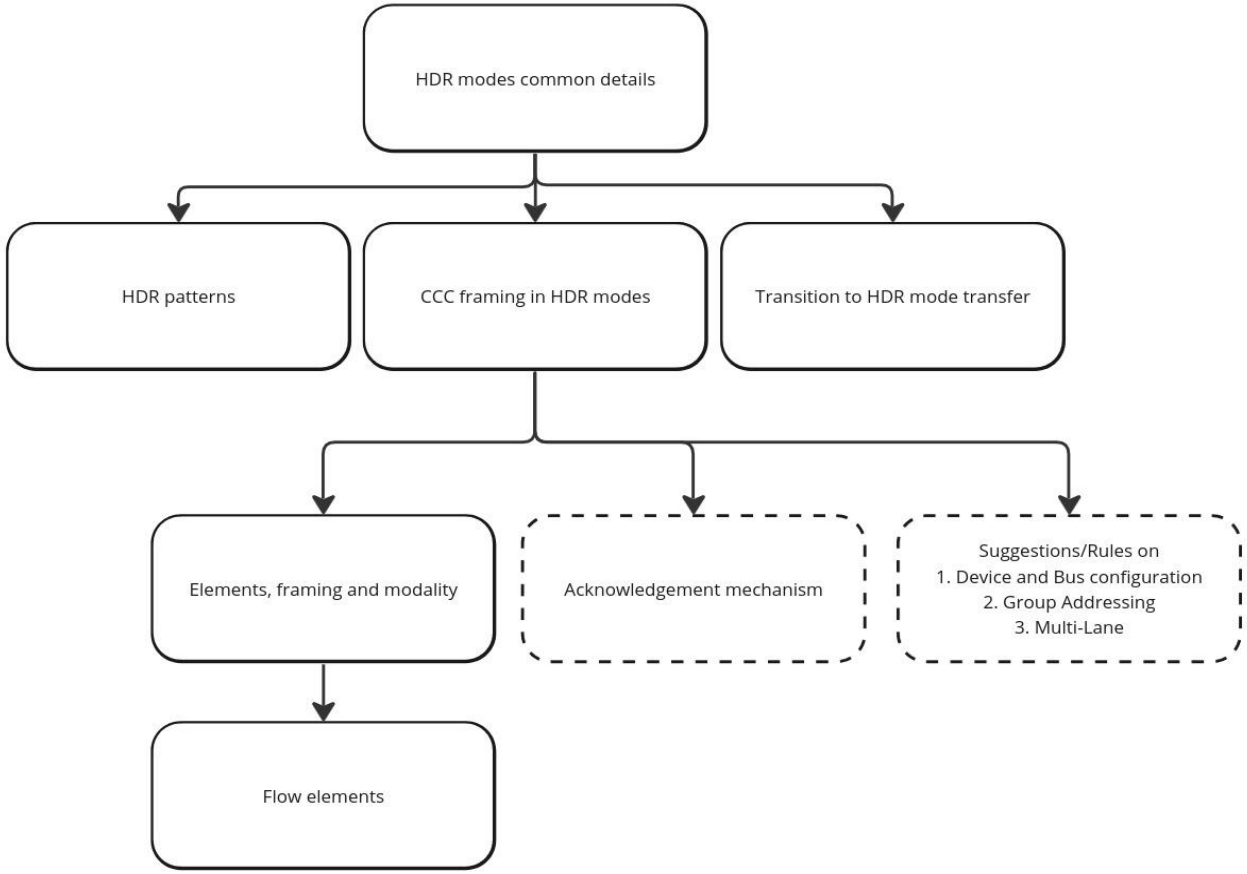
- There are two solutions.
- Effective clock utilization of the clocks
  - HDR -> High Data Rate
- Extension of data lanes for parallel transfer.
  - ML -> Multi Lane
- Also, Multi-lane transfer can be with either SDR mode or with HDR modes.





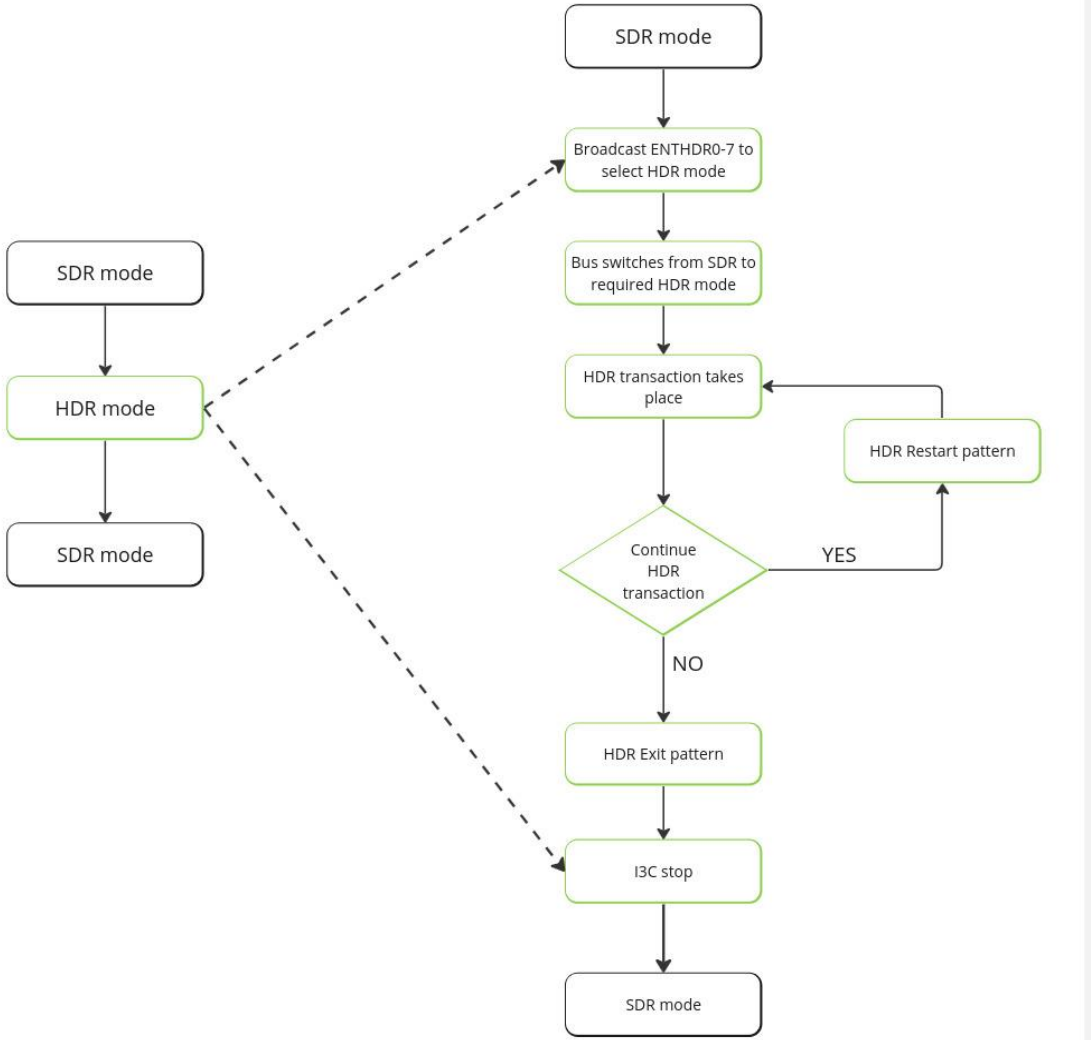
Common HDR details

- SDR is single variant.
- HDR is multi variant (4 modes).
- All HDR modes have some common "details" and "rules" which must be followed.
- HDR patterns
  - Defines about the exit and restart of HDR transaction.
- CCC framing in HDR modes
  - Generic frame structure.
  - Common ACK mechanism in HDR modes.
  - Basic support and rules in GA, MDA and ML.
- Transition to HDR mode transfer
  - Defines how SCL is transitioned from SDR to HDR.



Basic HDR CCC transaction

- SDR --> HDR --> SDR.
- ENTHDR0-7 (Enter HDR mode) CCC is used.
  - ENTHDR0 is for HDR DDR.
  - ENTHDR3 for HDR BT.
  - ENTHDR1,2 aren't supported in I3C basic.
- HDR transaction has **bus wide** effect.
- Patterns determine the HDR flow.
  - HDR exit pattern
  - HDR restart pattern.
- HDR transaction actual implementation varies with the modes.



HDR Patterns

Pattern : A unique clock signal(s) which performs specific function.

HDR Exit Pattern

- Exits from HDR and returns to SDR.
- Same exit pattern for all HDR modes.
- All I3C targets must detect and respond to Exit pattern.
- Exit pattern is always followed by I3C stop.

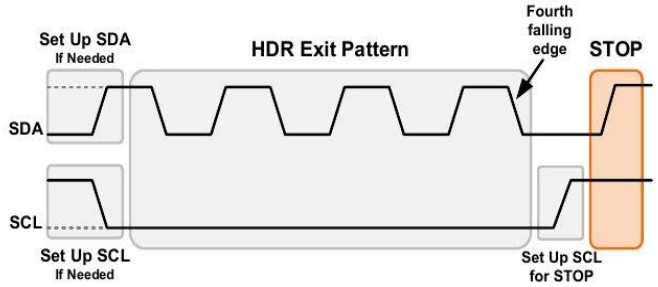


Figure 91 HDR Exit Pattern Followed by STOP

HDR Restart pattern

- Continues HDR transactions without exiting.
- Same restart pattern for all HDR modes.
- Supported I3C targets per HDR mode must detect and respond to Restart pattern.
- Restart is typically followed by Command word.

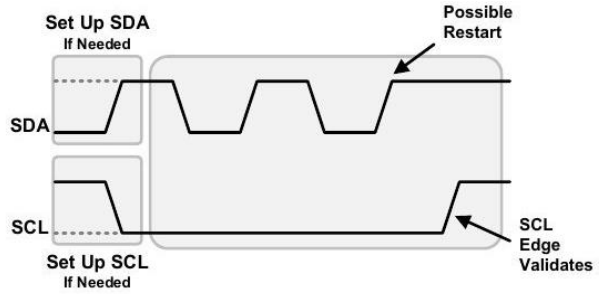
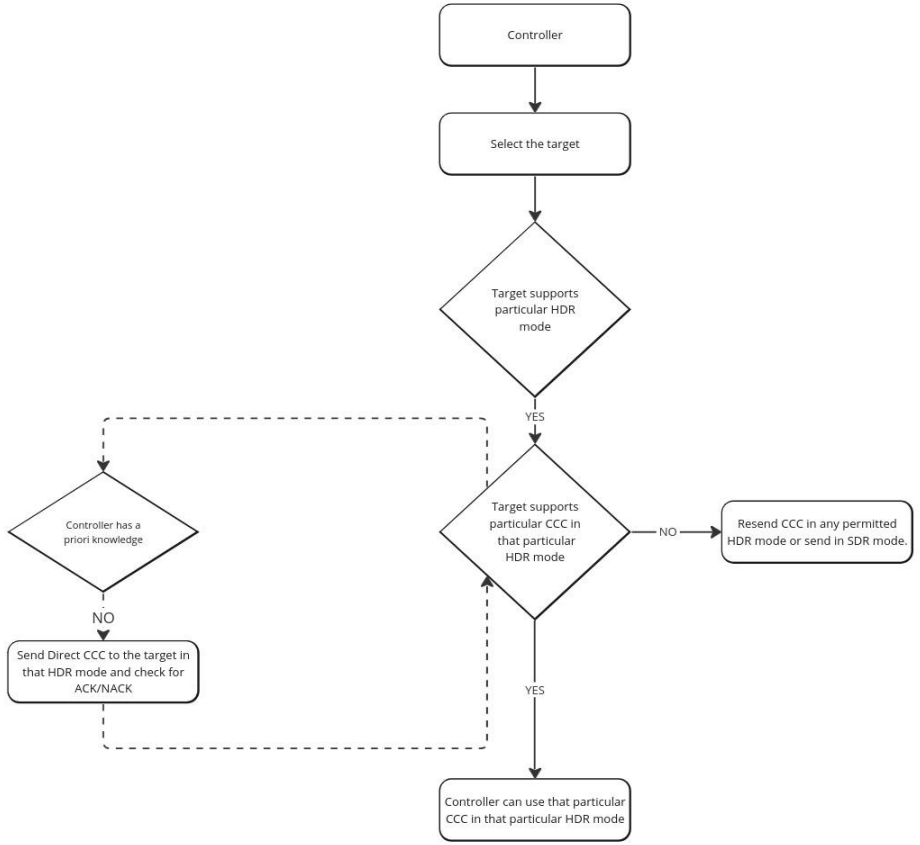


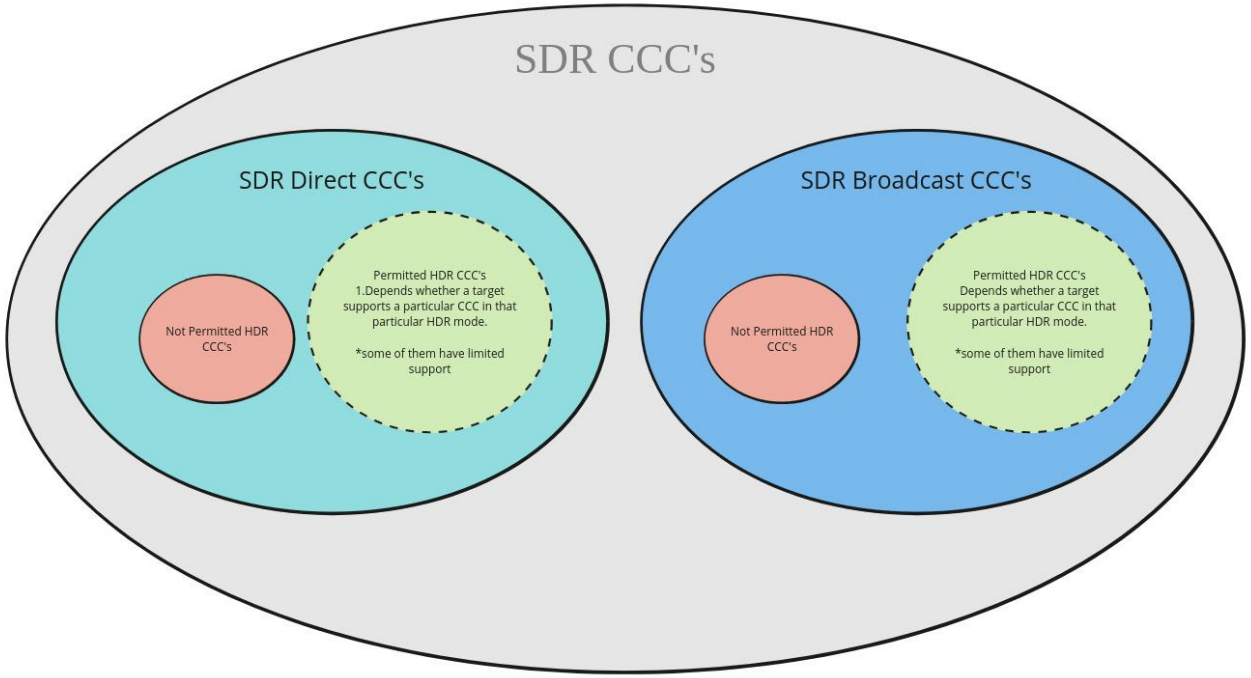
Figure 92 HDR Restart with Next Edge

CCC's support in HDR mode

Flowchart of CCC support

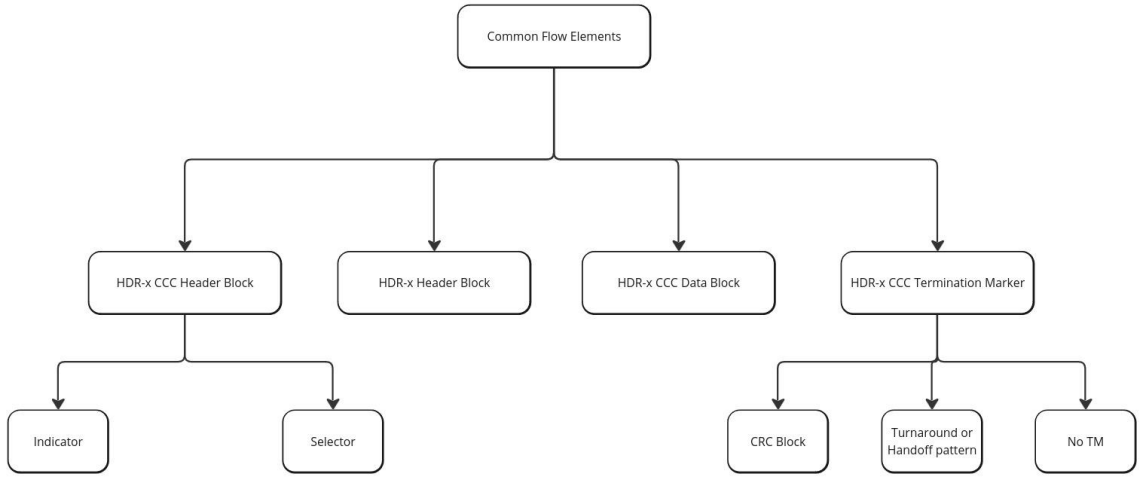


CCC's support in SDR vs HDR modes



Common Flow Elements (FE)

- Each HDR mode has its own unique framing.
- But the fundamental blocks are common in all HDR modes, called "Common Flow elements".
- There are four "Flow elements".
  - CCC Header Block.
  - Header Block.
  - Data Block.
  - Termination Marker.
- These define about generic packet frame with respect to the type of transaction.
- All HDR capable devices must understand the FE's.
- Actual behavior, position and functionality is based on per HDR mode.



- CCC header Block
  - Indicates the start of the CCC. Mandatory block
  - Two types
    - Indicator
      - Required for both Broadcast and Direct CCC's
      - Provides the broadcast address.
    - Selector.
      - Required for only Direct CCC
      - Provides the target address.

- Header Block
  - Indicates the end of CCC frame.
  - It is not same as CCC Header Block and thus neither an Indicator nor Selector.

- CCC Data Block
  - Used for data transfer and GET/SET CCC's
  - Varies based on type of transaction.
    - Sent by Controller -> Broadcast CCC
    - Sent by Controller -> Direct Write or Direct SET CCC
    - Sent by Target -> Direct Read or Direct GET CCC.

- Termination Marker
  - Used to denote the end of Data message
  - Used for denoting transition across CCC FE's
  - Used for ACK by the target.
  - Actual implementation is very specific on HDR mode and transaction type.
    - CRC Block
    - Turnaround or Handoff Pattern
    - No termination Marker
    - ACK

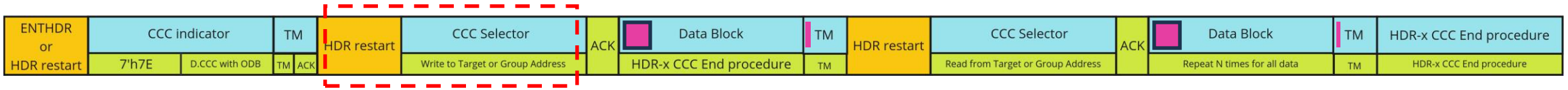
Broadcast CCC

To remain in CCC mode

Return to HDR reads or writes

End of this CCC

Direct CCC (read and write)

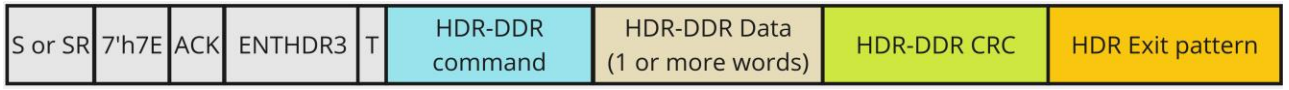


Overview of HDR DDR and HDR BT features

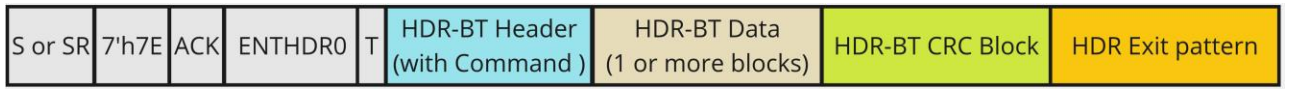
Features	Double Data Rate (DDR)	Bulk Transfer (BT)
Basic data form	Word (2 bytes)	Block (0-32) bytes
Types of words/blocks	4 (Command, Data, CRC, Res)	3 (Header, Data, CRC)
Effective data rate (12.5Mhz)	20Mbps	24Mbps
Multi-Lane support (I3C Basic)	No	Yes (x1, x2, x4)
Flow control	Only Preamble	5 bytes are present
Parity	Two bits for parity for data	No separate parity for data
CRC	CRC5	CRC16 & CRC32(optional)
SCL by target during read	Strictly not allowed	Allowed if Controller agrees
Byte-orientation	Not purely Byte oriented	Purely Byte Oriented
Decoupling Data from CCC's and Control	No, Control is implicitly attached with data	Yes, Control is separated from data
Data and SCL relation	Sampled at both Rising and Falling edges	Sampled at both Rising and Falling edges

Packet frames in HDR DDR and HDR BT

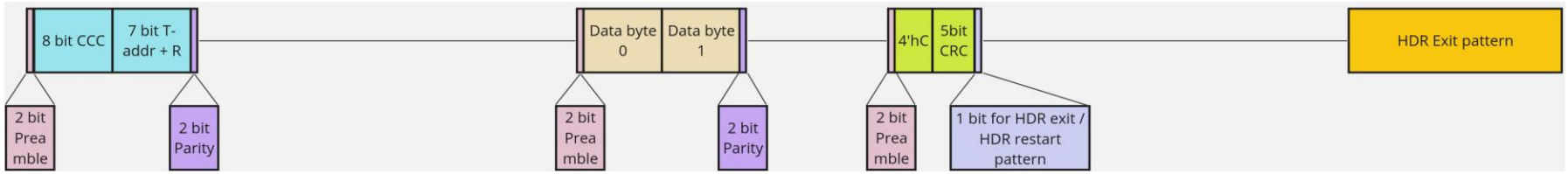
Higher level HDR DDR frame



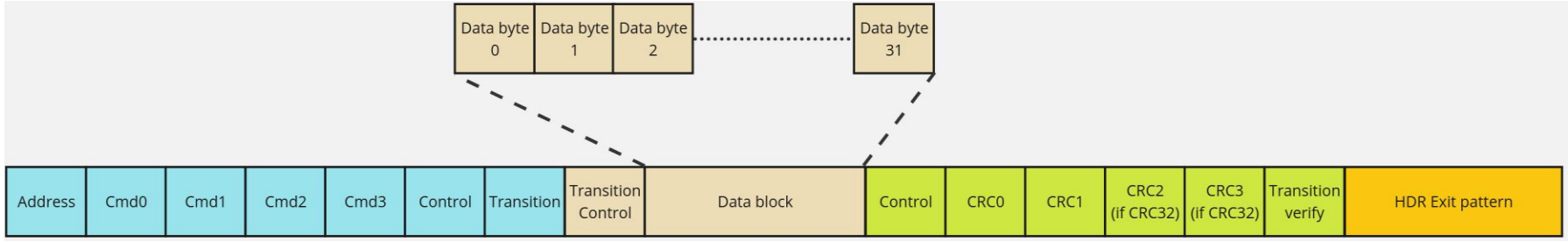
Higher level HDR BT frame



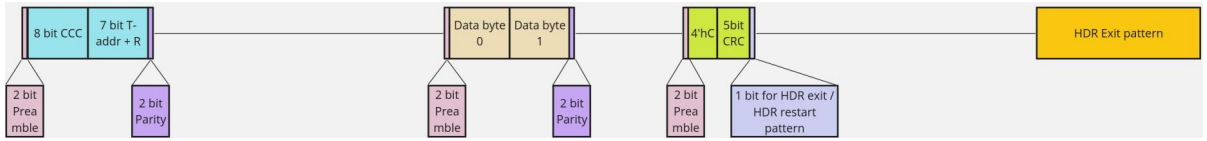
Actual HDR DDR frame



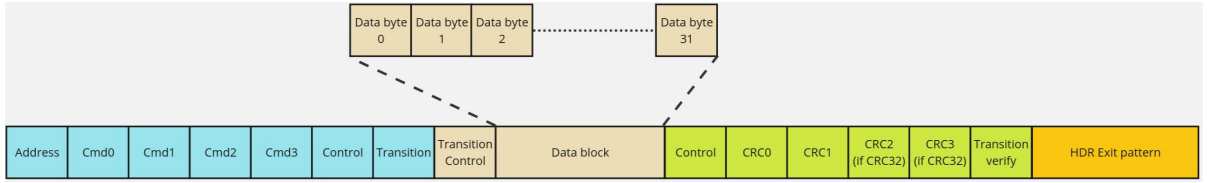
Actual HDR BT frame



Performance measure HDR DDR and HDR BT

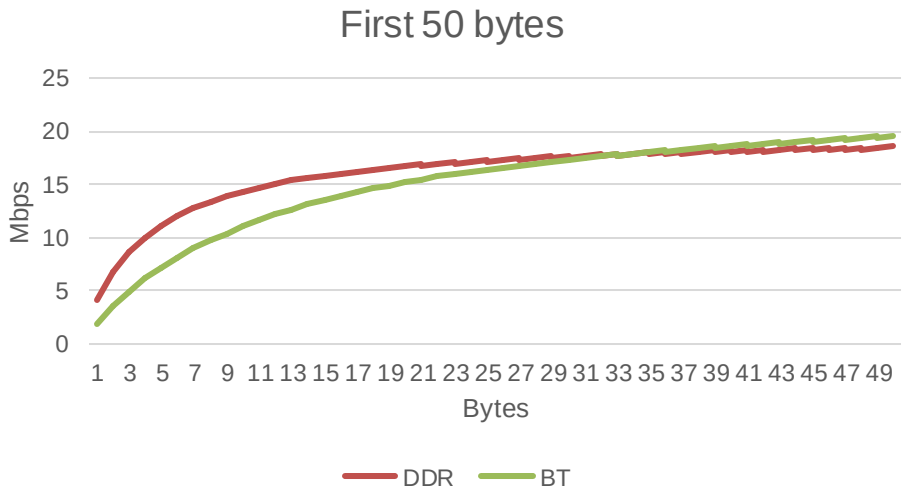


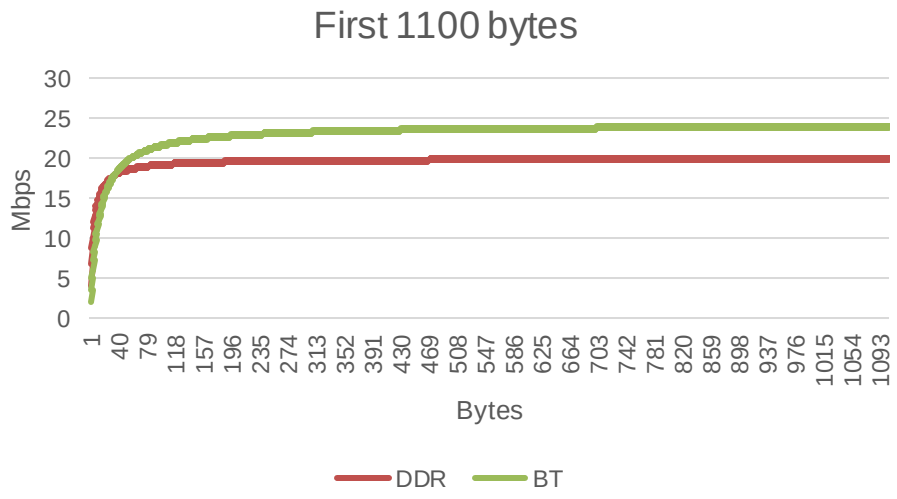
$$\left(\frac{x}{(x+header+2*(parity+preamble)+(CRC))}*\frac{Dataword}{Dataword+preamble+parity}*(freq)\right)*2 \rightarrow \left(\frac{x}{(x+4)}*\frac{16}{20}*(freq)\right)*2$$



$$\left(\frac{x}{(x+header+transition\_control+16\_CRC)}*\frac{Datablock}{Datablock+Transition\_Control}*(freq)\right)*2 \rightarrow \left(\frac{x}{(x+12)}*\frac{32}{33}*(freq)\right)*2$$

Measurement	Raw D.R	Real D.R(DDR)	Real D.R (BT)
1 byte	25 Mbps	4Mbps	1.8Mbps
1 KB message	25 Mbps	19.92Mbps	23.96Mbps
10 KB message	25 Mbps	19.99Mbps	24.21Mbps





Relation between Common Flow Elements and Per mode HDR elements

- It is important to know that Common Flow Elements and per mode HDR elements are completely different.
- In many cases the naming conventions are so similar which leads to confusion.
- A particular flow element may be implemented using multiple types of words (DDR) or blocks (BT) based on that HDR mode.
- In the subsequent slides following conventions are used.


Indicates Common Flow Element.

Indicates what information is contained in that Common Flow element.


Indicates which words/blocks are used in that HDR mode to implement the Common FE's.


Indicates the actual implementation in that HDR mode to implement the Common FE's.

Generic broadcast CCC

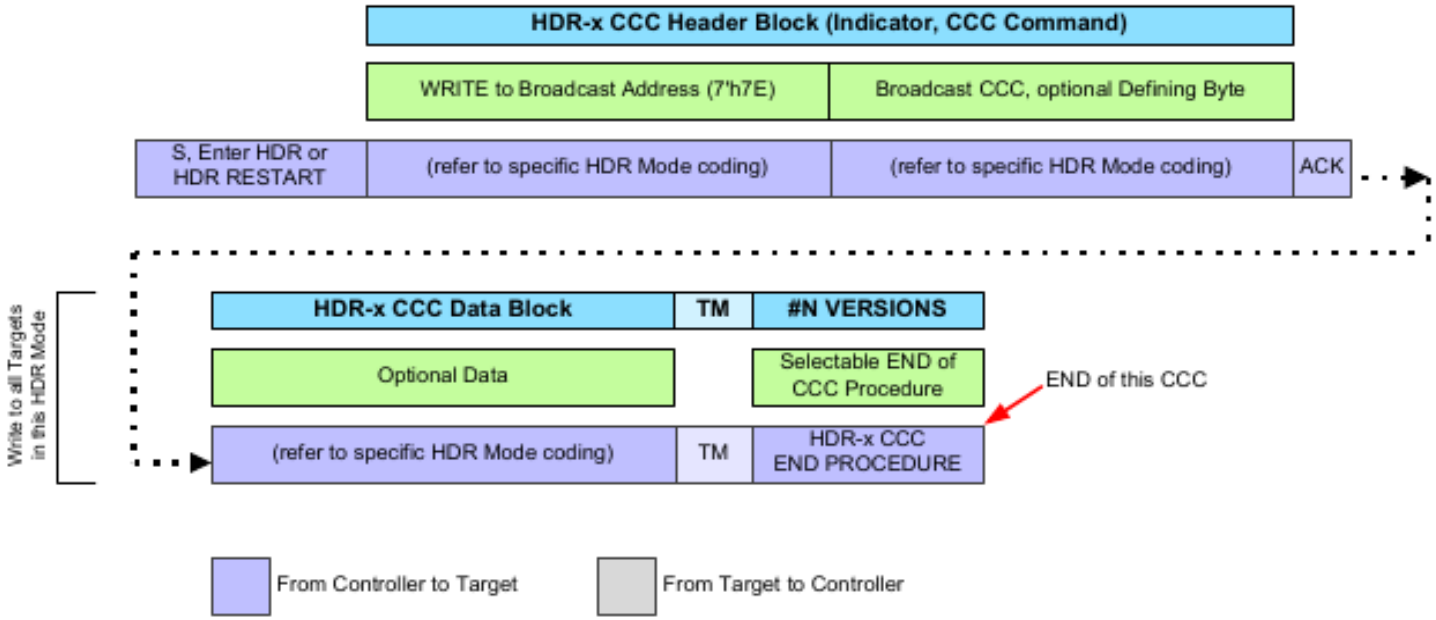


Figure 96 Begin Broadcast CCC Per HDR Mode

Generic Direct CCC

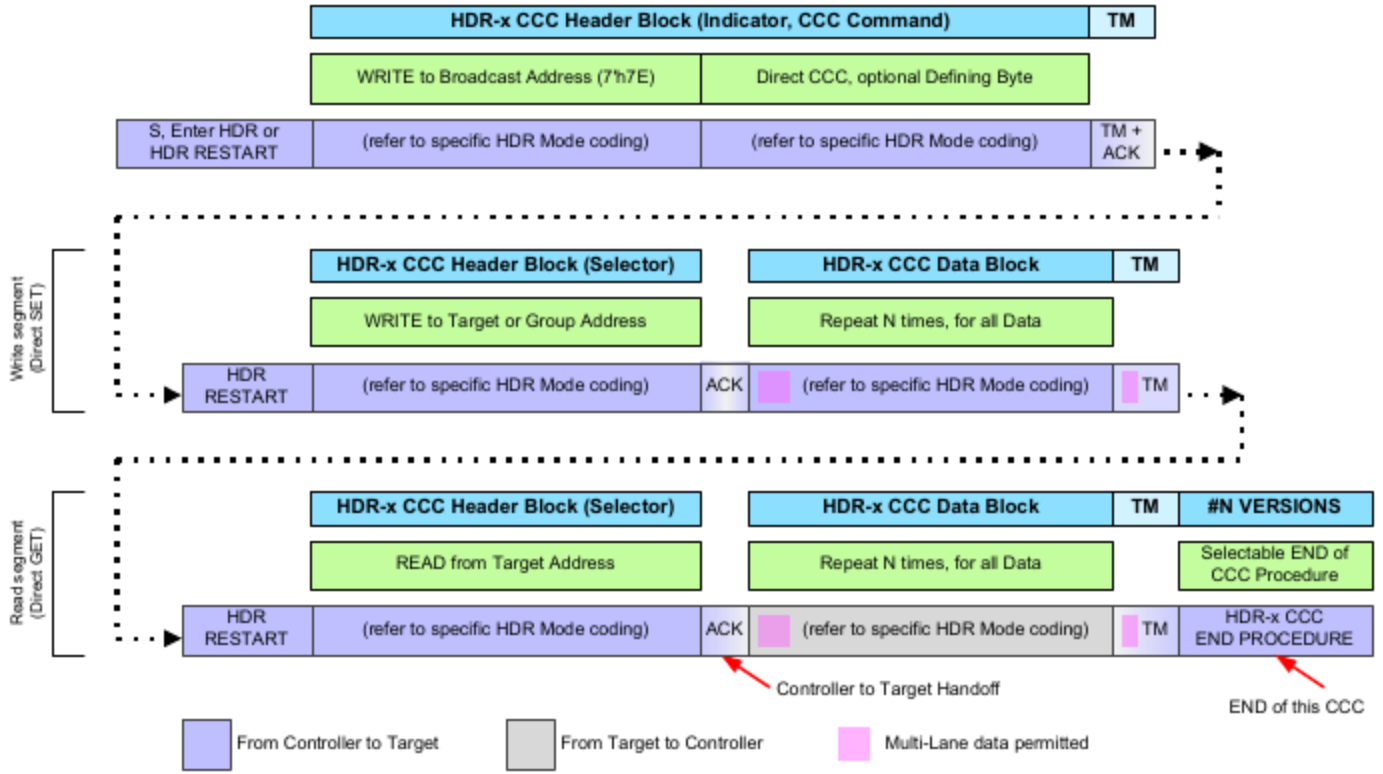


Figure 97 Begin Direct CCC Per HDR Mode

Generic CCC end procedure

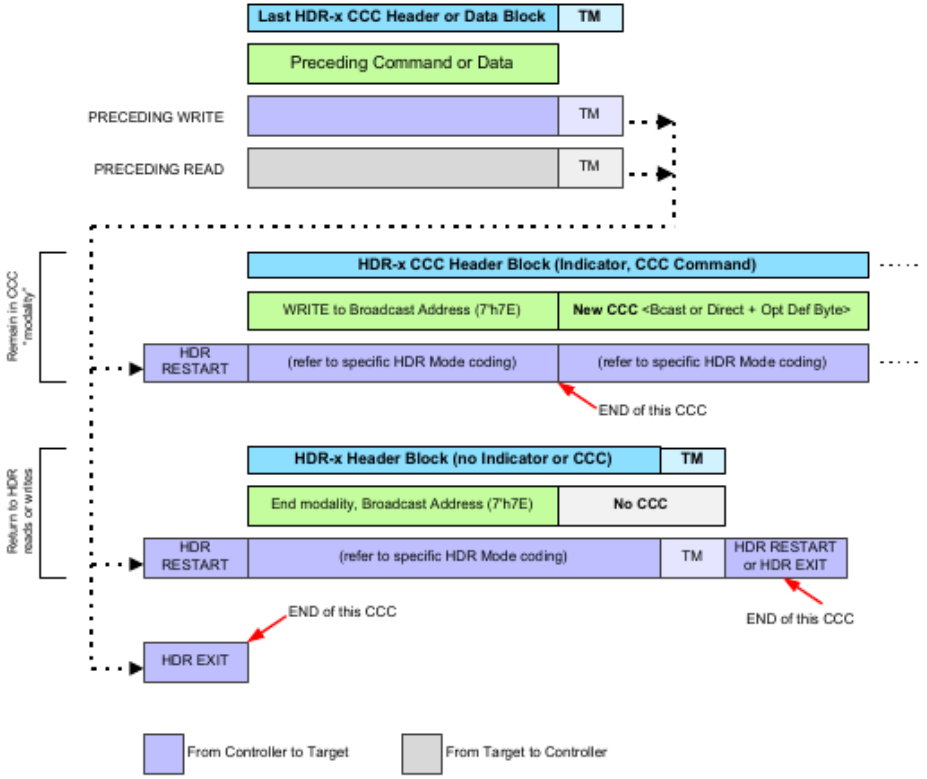


Figure 98 End of CCC Procedures Per HDR Mode

HDR Broadcast CCC

HDR DDR Broadcast CCC Format

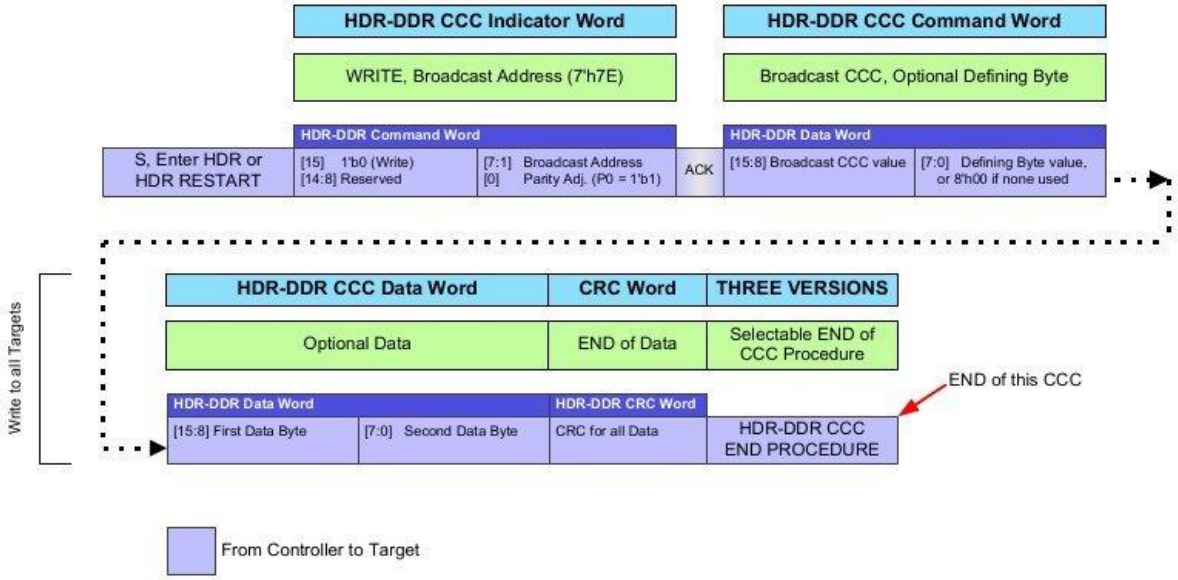


Figure 108 HDR-DDR Broadcast CCC Format

HDR BT Broadcast CCC Format

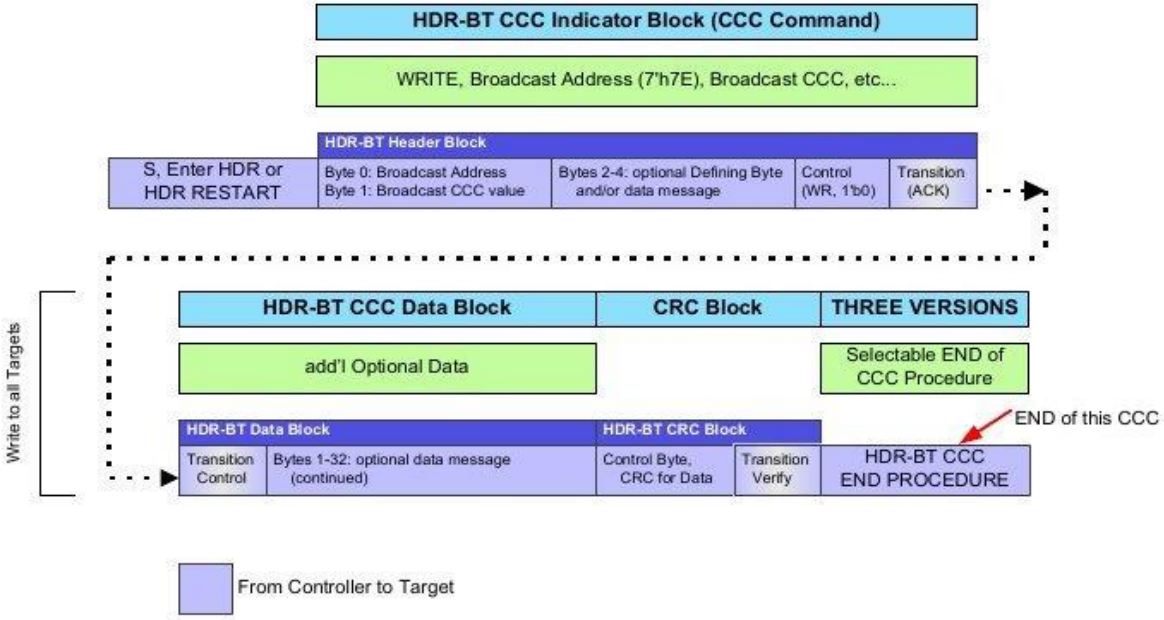


Figure 124 Begin Broadcast CCC in HDR-BT

HDR Direct CCC

HDR DDR Direct CCC Format

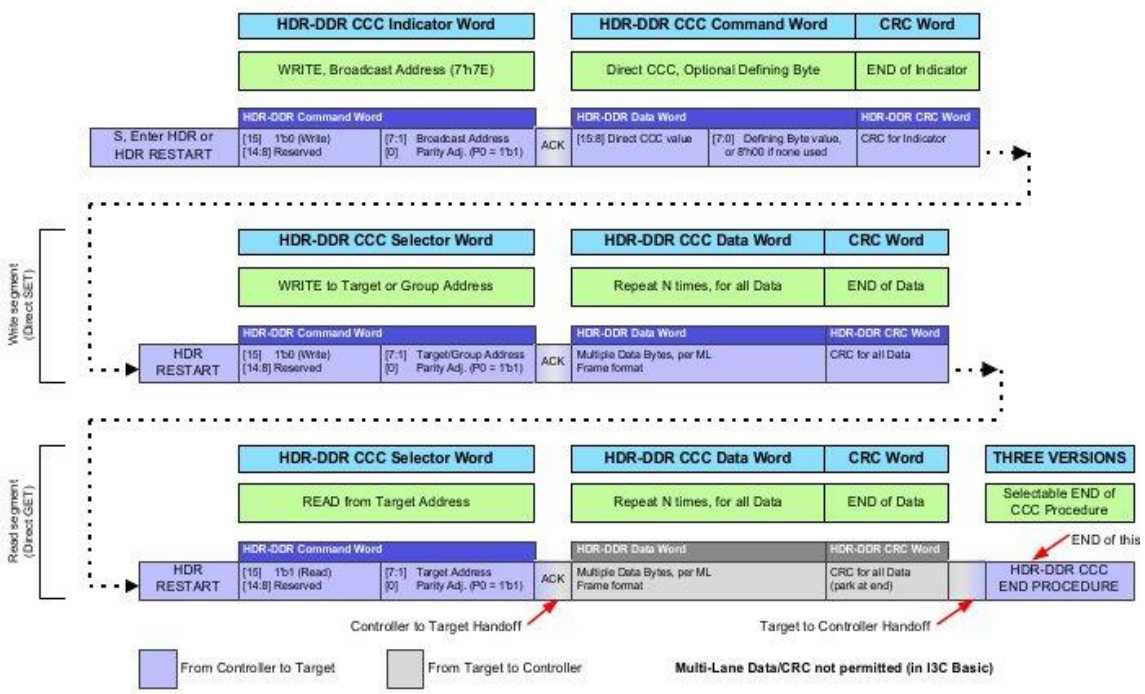


Figure 109 HDR-DDR Direct CCC Format

HDR BT Direct CCC Format

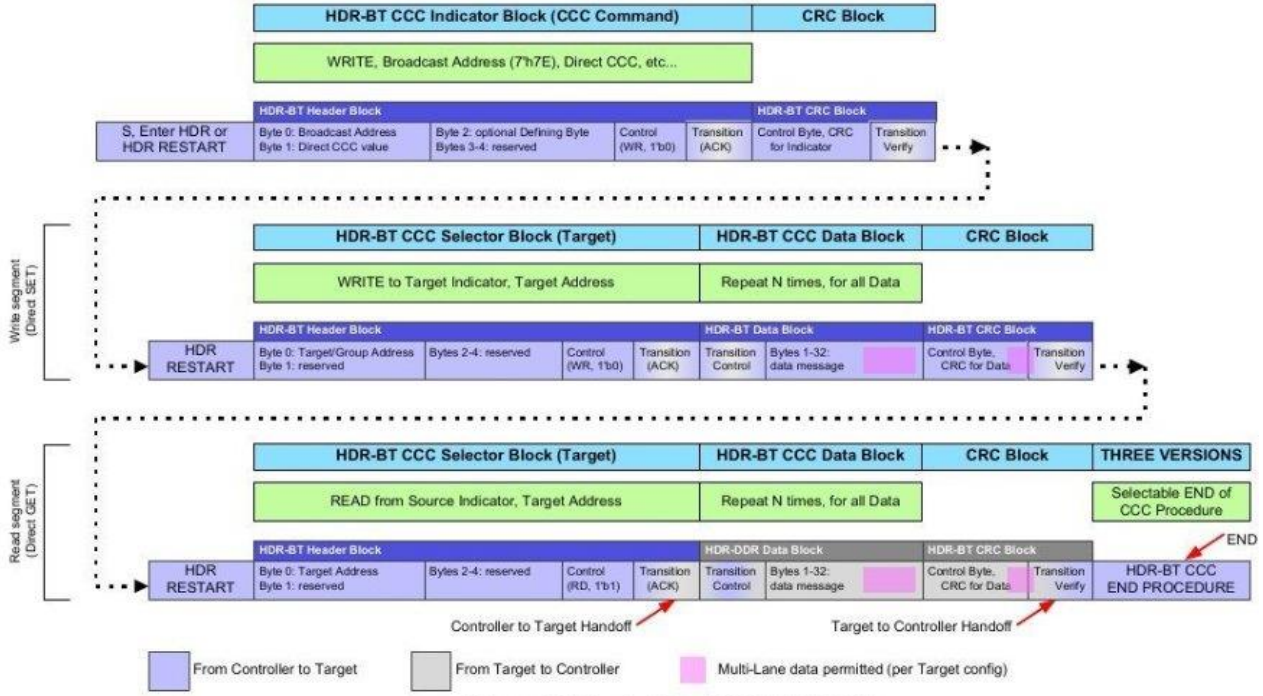


Figure 125 Begin Direct CCC in HDR-BT

HDR End Procedures

HDR DDR End Procedures

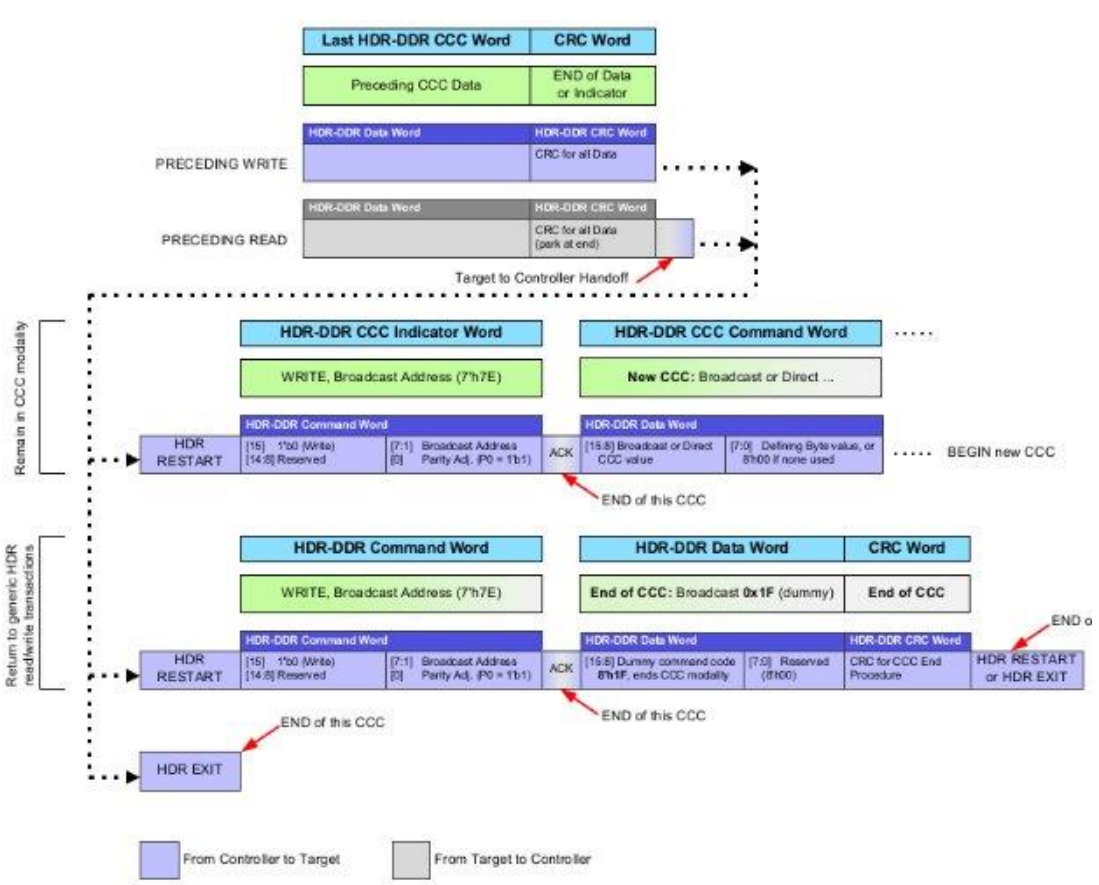


Figure 110 HDR-DDR CCC End Procedures

HDR BT End Procedures

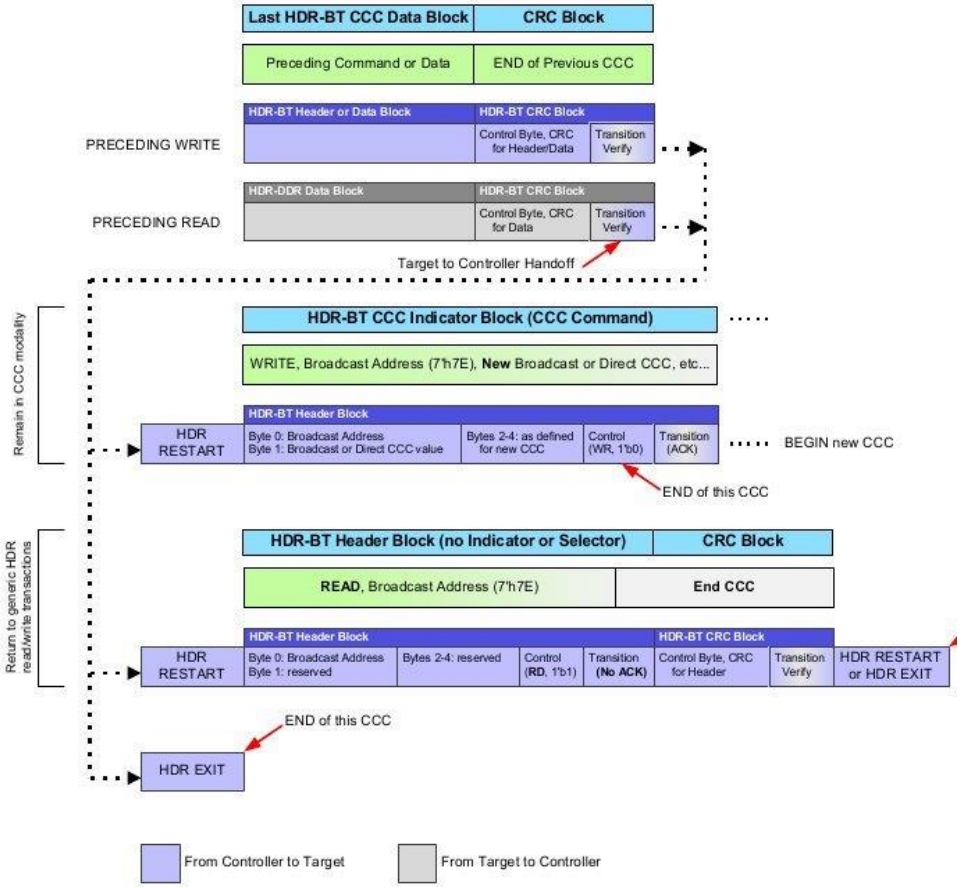
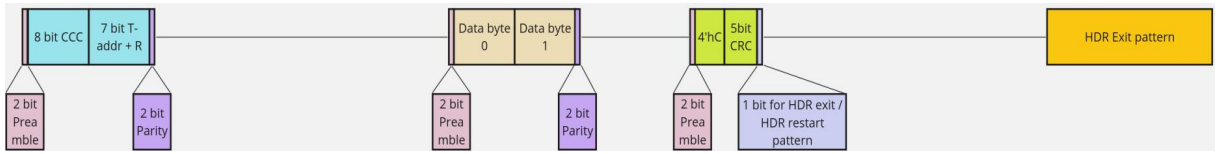


Figure 126 HDR-BT CCC End Procedure Options

Flow and Error Control in HDR DDR and BT

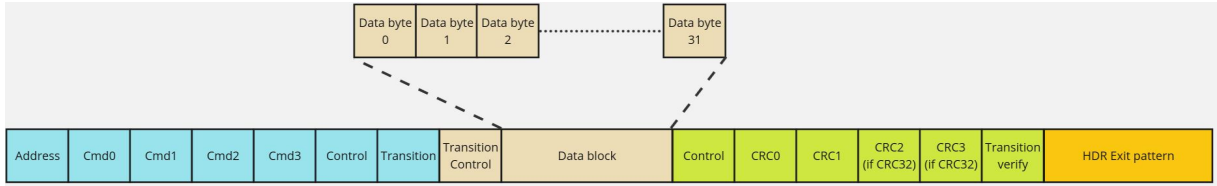
HDR DDR

- Flow and Error control in DDR is
  - SDR<DDR<BT
- Only has 2-bit preamble which has multiple purposes.
- 2-bit odd parity per word.
- Only CRC5 for entire transaction.



HDR BT

- BT has highest Flow and Error control.
- 5 bytes exclusively for flow and transition control.
  - Control -> Header
  - Transition
  - Transition Control
  - Control -> CRC
  - Transition Verify.
- Provides CRC16 or CRC32* for entire transaction.
- Provides parity for Transition Flow Bytes.



Preamble

- Most important bits in HDR-DDR.
- Interpretation is context based.
- Three responsibilities of Preamble
  - Indicates the type of data that follows i.e. Command, Data or CRC.
  - Allows the controller to terminate a Read and to determine whether target is willing to respond to a Read
  - Allows the target to request a write termination.

Table 64 HDR-DDR Preamble Values

Context	Preamble Value and Interpretation			
	2'b00	2'b01	2'b10	2'b11
After Enter HDR	Reserved for special use cases	Command Word follows	–	–
After Read CMD		–	Target ACK, Data follows	Target NACK, Aborted
After Read DATA		CRC Word follows	Controller Aborts, Target yields. *Controller drives second 0.*	Data follows. *Controller does not drive second bit.*
After Write CMD		–	Target ACK, Data follows	Target NACK, Aborted
After Write DATA		CRC Word follows	Target requests END Controller complies	Data follows

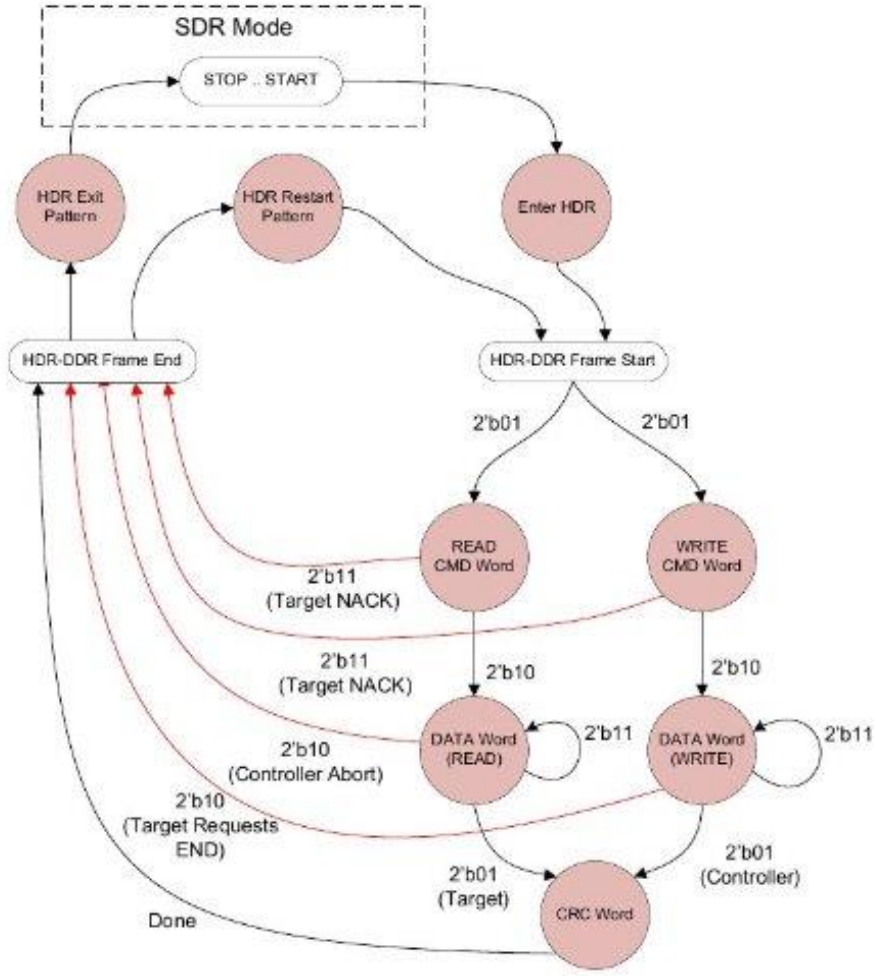


Figure 102 HDR-DDR Preamble Bits State Diagram

Park1,HighZ convention

- It is an acknowledgement mechanism followed in the I3C HDR –BT mode.
- Always the first clock is used in any lane format.
- The transmitter shall
  - SDA[0]->bit[0] -> 1 on first half clock.
  - SDA[0]->bit[1] -> High-Z on second half clock.
- The receiver shall drive it low according to the condition required.
- For read request, where target sources SCL,
  - The clock is released by controller after first half.
  - Target drives the clock from the second half.

Flow and error control bytes in HDR-BT

Control Byte (Header Block)

- Sixth byte in the 7-byte Header Block
- Indicates the type of transaction.
  - Read/Write
- Indicates who is transmitting the SCL.
  - SCL may be transmitted by anyone in Read
  - SCL is transmitted by controller in Write.
- Indicates whether the transaction is normal BT message or Direct CCC continuation.
- Contains the parity of the first six bytes of the Header Block.

Control Byte (CRC Block)

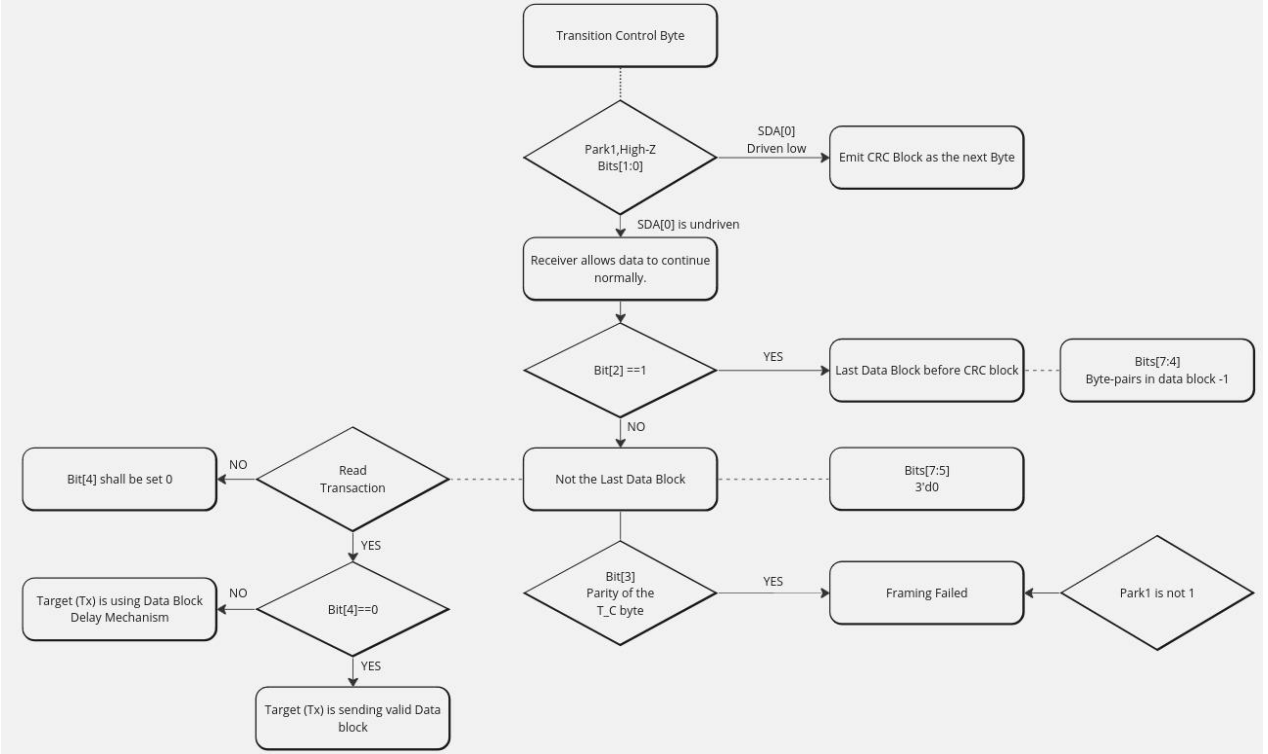
- First mandatory byte in the CRC block.
- Indicates that this is CRC block, not any Data block.
- Verifies the type of CRC for that transaction, which is selected in the Header Block.
- Informs about framing error.
- Informs whether previous Data Block was terminated or ended normally.

Transition Byte

- The last byte in the Header block.
- Follows "Park1,HighZ" convention for ACK.
  - If left undriven, then it is NACK.
- Used for bus transition and acceptance.
  - Checks whether target is accepting Write or Read from controller.
  - During Read, if target sources clock, release SCL to target.
- Indicates whether target can use Data Block Delay mechanism
  - It allows Targets to get additional time when returning Read data.
  - There is a limit of max number of delay bytes can be sent (tBT_DBD).

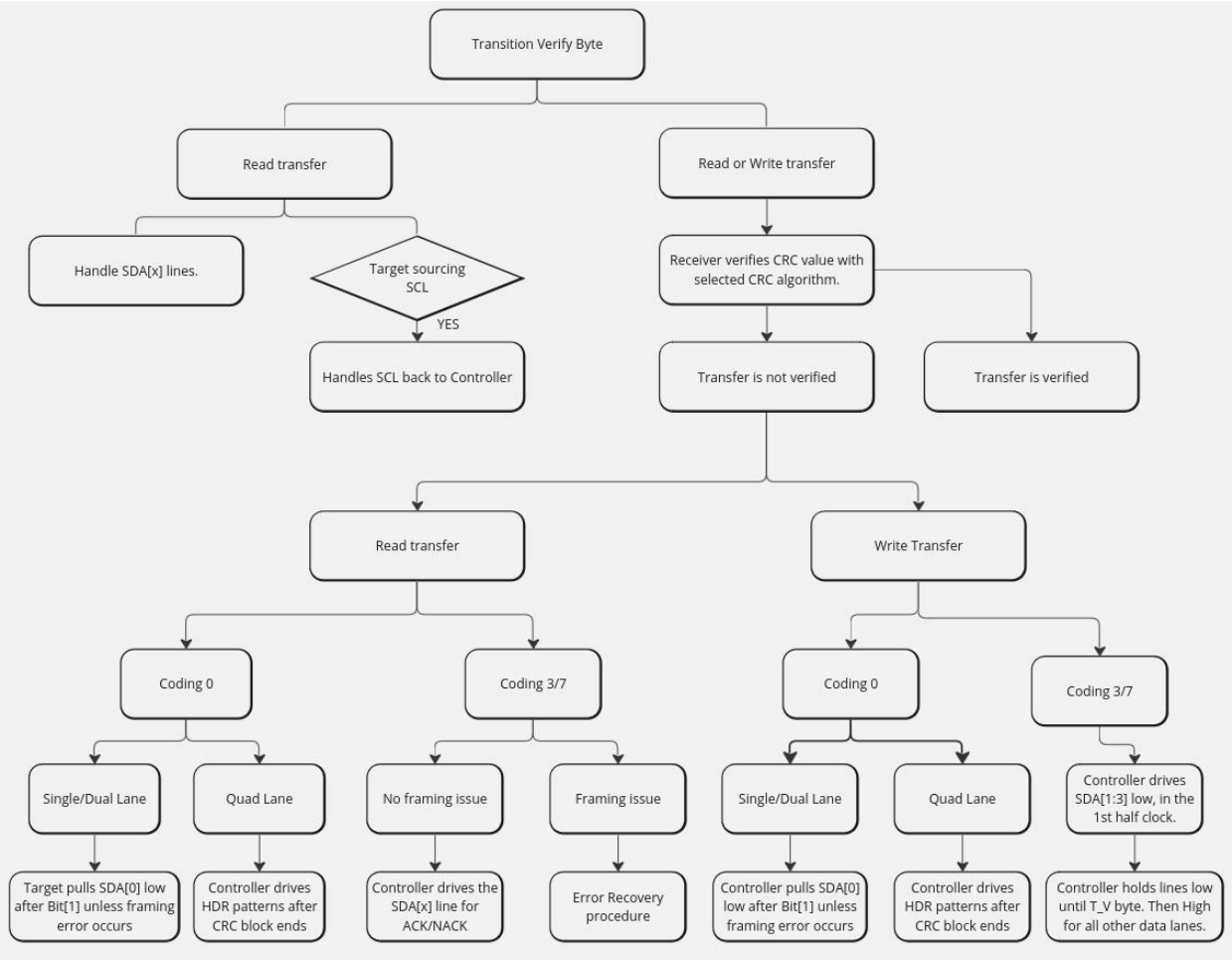
Transition Control Byte

- The first mandatory byte in the multi byte Data Block.
- Allows Receiver to control the receiving flow of data for that particular block.
- Follows Park1,High-Z for termination of Data block by receiver.
- Verifies parity for Transition Control byte.
- Checks for Last Data Byte.
- Checks whether the Target is sending a Delay byte or not.



Transition Verify Byte

- Serves two purposes
  - During read, Hands SDA[x] lines and SCL line (if target sources SCL) back to the controller.
  - During Read/Write CRC field is verified by the receiver.
- Park1,High-Z convention is used for completion by the receiver.
- If CRC verification fails, depending upon the type of transfer, subsequent actions are taken.



Transition Flow Control

Flow control is achieved using

- Transition byte
- Transition Control byte
- Transition Verify byte

- Read transfer flow control examples include
  - Target that does not accept the Read transfer.
  - Target that accepts the Read transfer and sends all Data Blocks (i.e., without any delay or termination)
  - Target that handles the Controller terminating the Read transfer, and subsequently provides the CRC Block after the last Data Block that it sent
  - Target that uses the Data Block Delay mechanism before sending the first Data Block.

- Write transfer flow control examples include
  - A Target that does not accept the Write transfer
  - A Target that accepts the Write transfer and receives all Data Blocks.
  - A Target that terminates the Write transfer before the Controller has sent all Data Blocks
  - A Target that indicates a CRC mismatch (or other error) after it has received the Data Blocks

Introduction to Multi Lane transfers

- In multi-lane data transfer additional physical wires are used to increase the data rate.
- Up to three additional lanes can be used.
  - Thus x1, x2, x4 speeds are supported.
- Multi-Lane is an enhancement of SDR or HDR data modes.
- Only HDR-BT ML is allowed in I3C basic.
- Extensive rules are followed for ML devices with Group addresses and multiple dynamic addresses.
- Two important terms
  - Additional Data Lanes or Data lanes -> depends on the context
  - Coding
- The combination of Coding and Additional data lanes ensure the inter-operability of ML data transfer.
- Default coding is "Coding0" and lane configuration is "Single Lane". It is supported by all targets (ML capable and non-ML capable)

Coding and Additional Data lanes

Coding

- Determines the format how each device shall interpret Header block and all HDR-BT CCC flows.
- Two types are present
  - Compatible mode -> Coding 0
  - Alternate mode -> Coding 3 and Coding 7
- Once assigned, coding shall remain same throughout the transaction.
- Determined by the least number of data lanes where all devices are connected.
- Extensive rules are followed for coding change.
- Higher order coding doesn't allow lower order data lanes.

Data lanes

- Determines the format how particular device shall interpret the Data block and TM.
- Three types are present
  - Single lane -> SDA[0]
  - Dual lane -> SDA[0] and SDA[1]
  - Quad lane -> SDA[0], SDA[1], SDA[2], SDA[3]
- ML format is per dependent on device, remains same per transaction to that device.
- Easy configuration of ML data transfer.
- Always recommended to use the highest possible multi lane configurations.

THANK YOU