

Linyu Zhu

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Education

2022 – 2025 📖 M.S. ECE, Shanghai Jiao Tong University

2018 – 2022 📖 B.S. ECE, Hunan University.

Research Publications

Conference Proceedings

- 1 Y. Cai, **L. Zhu**, and X. Guo, “Revisit mbff: Efficient early-stage multi-bit flip-flops clustering with physical and timing awareness (submitted),” in *2025 30th Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2025.
- 2 Q. LI, Y. Luo, Z. Li, *et al.*, “Sarcasm-vllm: An advanced vision-large language model for multimodal sarcasm detection (submitted),” in *Proceedings of the AAAI Conference on Artificial Intelligence (AAAI)*, 2025.
- 3 **L. Zhu** and X. Guo, “Spatial-temporal collaboration: The ultimate solution for electronic design automation prediction (submitted),” in *Proceedings of the AAAI Conference on Artificial Intelligence (AAAI)*, 2025.
- 4 X. Guo, X. Zhao, and **L. Zhu**, “Integration of shift-left updates into logic synthesis and macro placement,” in *2024 Conference of Science and Technology for Integrated Circuits (CSTIC)*, 2024, pp. 1–3.
🔗 DOI: 10.1109/CSTIC61820.2024.10531906.
- 5 **L. Zhu**, Y. Cai, and X. Guo, “One-for-all: An unified learning-based framework for efficient cross-corner timing signoff,” in *2024 IEEE/ACM International Conference on Computer Aided Design (ICCAD) (Accepted)*, 2024.
- 6 **L. Zhu** and X. Guo, “Elastic eda: Auto-scaling cloud resources for eda tasks via learning-based approaches,” in *2024 IEEE 42st International Conference on Computer Design (ICCD) (Accepted)*, 2024.
- 7 **L. Zhu**, Y. Gu, and X. Guo, “Rc-gnn: Fast and accurate signoff wire delay estimation with customized graph neural networks,” in *2023 IEEE 5th International Conference on Artificial Intelligence Circuits and Systems (AICAS)*, 2023, pp. 1–5.
🔗 DOI: 10.1109/AICAS57966.2023.10168562.
- 8 **L. Zhu** and X. Guo, “Delay-driven physical-aware logic synthesis with reinforcement learning,” in *2023 CCF 4th Integrated Circuit Design and Automation Conference (CCF-DAC)*, 2023.
- 9 **L. Zhu** and X. Guo, “Delay-driven physically-aware logic synthesis with informed search,” in *2023 IEEE 41st International Conference on Computer Design (ICCD)*, 2023, pp. 327–335.
🔗 DOI: 10.1109/ICCD58817.2023.00057.
- 10 A. Zhang and **L. Zhu**, “A promising way of energy harvesting for implantable medical devices – thermoelectric generator (teg),” in *2021 International Conference on Smart City and Green Energy (ICSCGE)*, 2021, pp. 22–25.
🔗 DOI: 10.1109/ICSCGE53744.2021.9654315.

Books and Chapters

- 1 X. Guo, **L. Zhu**, and C. Yichen, *AI-Enabled Electronic Circuit and System Design - From Ideation to Utilization (Accepted, will publish soon)*. Springer, 2024.

Patents

- 1 X. Guo and **L. Zhu**, "A layout-driven logic synthesis technology for timing optimization."
- 2 X. Guo and **L. Zhu**, "Signoff-level interconnection delay estimation method and system based on graph learnin."
- 3 X. Guo and **L. Zhu**, "Signoff-level timing prediction methods and systems across process corners," ZL 2023 1 1787034.5.

Journal Articles

- 1 **L. Zhu** and X. Guo, "Pata-rec: Physically aware technology mapping with wire delay prediction (submitting)," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2024.
- 2 **L. Zhu** and X. Guo, "Physically aware learning-based shift-left paradigm in logic synthesis (submitting)," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2024.

Skills

Research	🔖	My research interest includes AI for EDA. Especially, AI based shift-left in Logic Synthesis, Technology Mapping, Sign-off, et al. Currently, I am also interested in EDA on cloud, Quantum circuit design automation and chip reliability design.
EDA	🔖	Commercial and open source EDA flow in advanced technology nodes (7nm, 28nm, 45nm).
Languages	🔖	IELTS grade: reading 9.0, listening 7.0 , writing 6.0 and speaking 6.5. GRE grade: Q166 V149 AW2.0. Native speak Mandarin Chinese.
Coding	🔖	C, C++, Java, Python, shell, tcl, matlab, R, \LaTeX , ...
Misc.	🔖	Academic research, teaching, training, consultation, \LaTeX typesetting and publishing.

Miscellaneous Experience


Awards and Achievements

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|------|---|---|
| 2018 | 🔖 | 2018 Second Prize Scholarship, HNU. |
| 2019 | 🔖 | 2019 Second Prize Scholarship, HNU. |
| 2020 | 🔖 | 2020 Second Prize Scholarship, HNU. |
| 2021 | 🔖 | 2021 Second Prize Scholarship, HNU. |
| | 🔖 | Recommended to SJTU for M.S. degree without entrance exam (GPA top 10%), HNU. |
| 2022 | 🔖 | Third Prize from the 4th Annual Integrated Circuits EDA Elite Challenge |
| 2023 | 🔖 | 2023 IC EDA Design Elite Challenge Finals Academic Enterprising Award Prize |

Certification

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| From 2018 | 🔖 | English Certification College English Test 4/6 (CET4/6), IELTS, GRE. |
| 2023 | 🔖 | IC summer School on Advanced EDA. Awarded by Peking University. |

Employment History

From 2023  **Reviewer** Invited as reviewer of ICCD, ISCAS, AICAS.

From 2022  **IEEE Student Member.**

 **M.S. candidate and researcher** in ICAS Lab, SJTU, supervised by Prof.Xinfei.Guo.

 **Lab server manager** in ICAS Lab, SJTU.