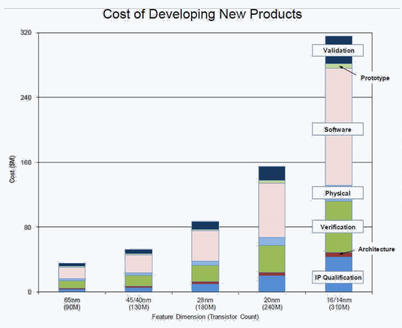
Learning-based Predictions for EDA Shift-left Paradigm

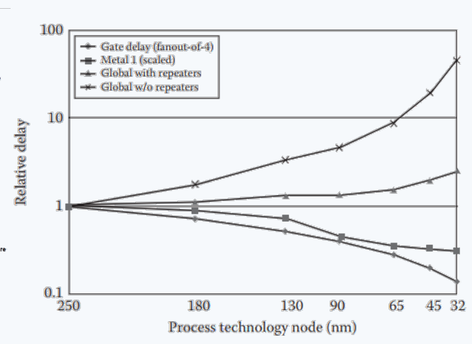
Linyu Zhu, Xinfei Guo
Shanghai Jiao Tong University, Shanghai

Overview

Why shift Left in EDA?

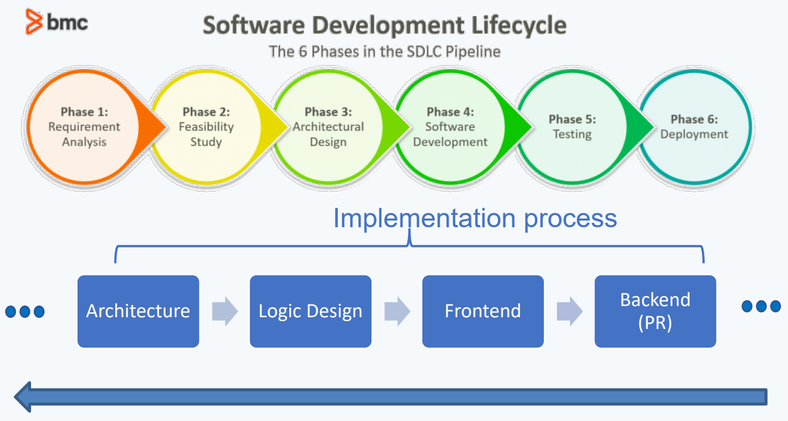
- Time to market pressure.
- Cost increases exponentially.
- Chips become more complex in general.
- New technology nodes introduce “new surprises”.





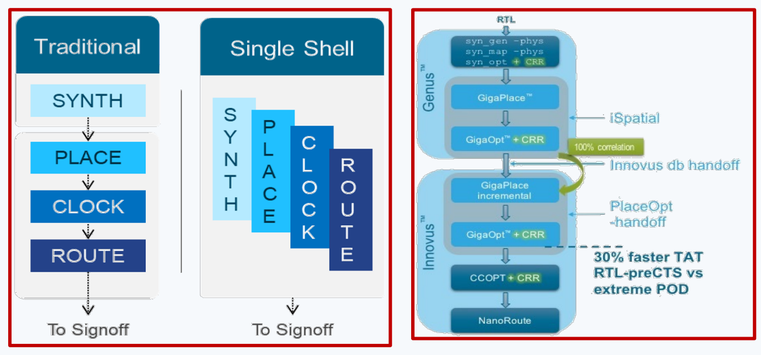
Previous Solutions

- Industry Tools.
- ML based timing, power prediction.
- Do optimization in previous stage.



This Dissertation

- Shift left in Logic Synthesis
- Shift left in single corner Timing Signoff
- Shift left in multi corners Timing Signoff



Shift left in Logic Synthesis [ICCD ’23]

Main Idea

- Each stage of EDA flow could be formulated as search problem.
- Employ A* inform search, we apply each node an inform value T(n).
- T(n)=total slack given by current stage (mirroring the cost-so-far to reach node) + total slack changed after P&R (estimated cost-to-go from current node).

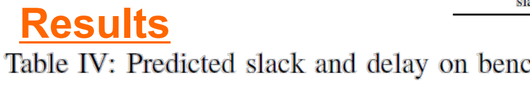
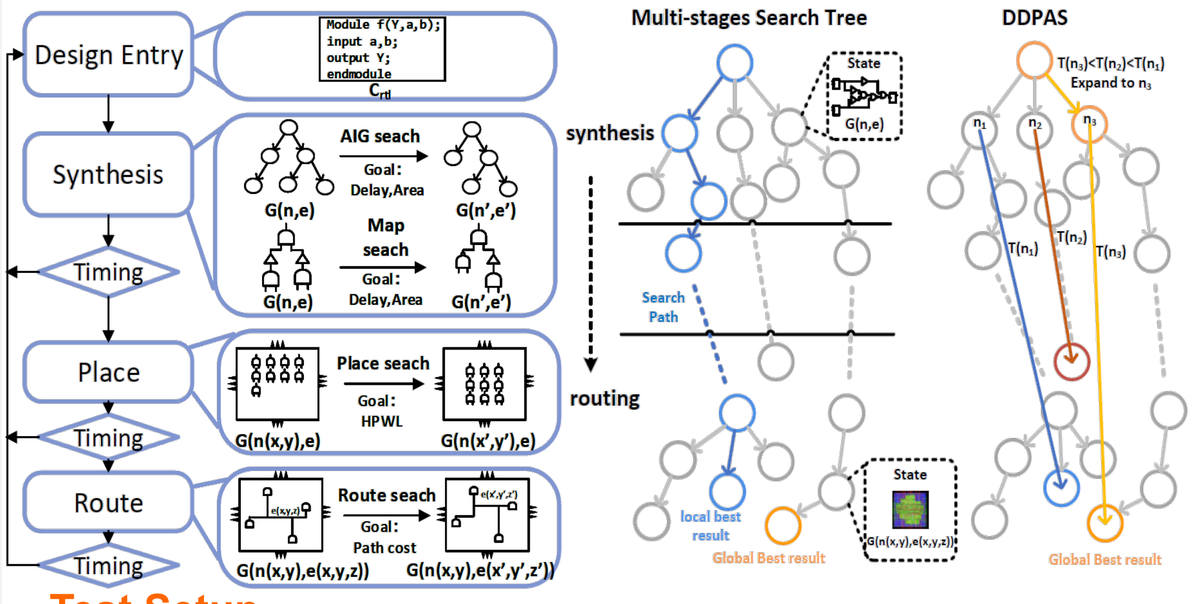


Table II: Feature list for NLP-based timing prediction

Gate Features		
Feature	**Source**	**Size (Type)**
Gate delay	STA timing report	1 (float)
Gate load	STA timing report	1 (float)
Slew	STA timing report	1 (float)
Arrival time	STA timing report	1 (float)
Fanout	STA timing report	1 (int)
Global Features		
Feature	**Source**	**Size (Type)**
Max path delay between 2 reg	STA timing report	1 (float)
Max path depth between 2 reg	STA timing report	1 (float)
Die area	SDC file	1 (float)
Clock period	SDC file	1 (float)
Clock period × die area	SDC file	1 (float)



Test Setup

- Open-source 45nm.
- Open-source Tools.
- Open-source Designs.

Results

Table V: Comparison of prediction accuracy (best R^2 from each work)

		Proposed	ICCAD22 [5]	MICPRO22 [7] (TabMLP Model)	MICPRO22 [7] (MPNN Model)	TCAD22 [6]
R^2	delay	**0.996**	0.956	0.79	0.87	0.91
	slack	**0.995**				

Table IV: Predicted slack and delay on benchmark designs with the proposed NLP-based model

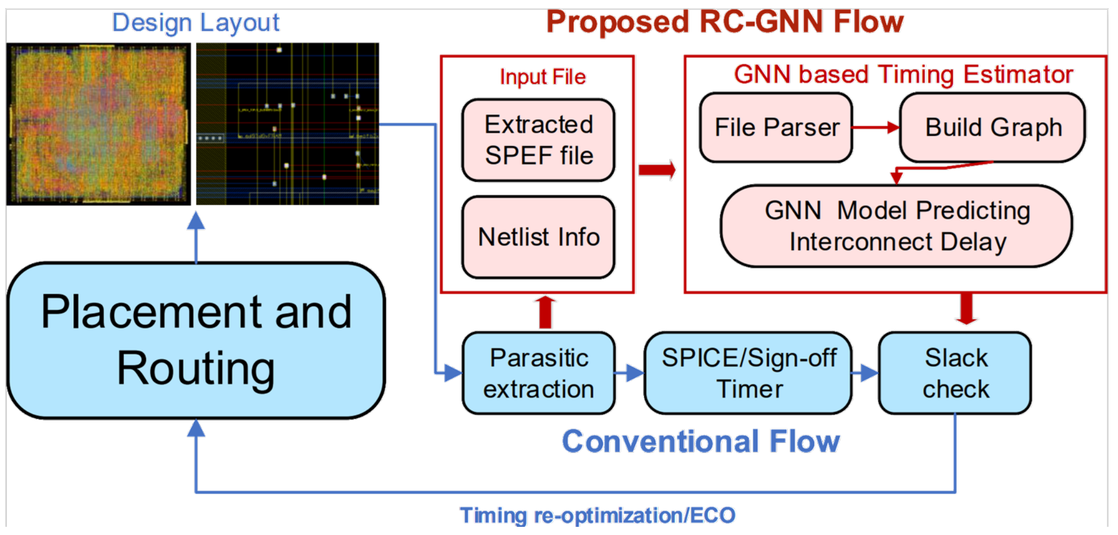
Design	Slack (ns)						Delay (ns)					
	MAE	R^2	MSE	ME	EVS	MedianAE	MAE	R^2	MSE	ME	EVS	MedianAE
AES	0.016	0.992	0.0005	0.078	0.9923	0.0118	0.012	0.994	0.0003	0.0627	0.994	0.0089
gcd	0.0025	0.9988	1.157e-5	0.0117	0.9989	0.0021	0.0018	0.9986	5.09e-6	0.0046	0.9986	0.0014
TinyRocket	0.0264	0.9959	0.0013	0.169	0.9959	0.0189	0.023	0.9954	0.0012	0.1616	0.9954	0.0135
ibex	0.018	0.9977	0.0009	0.2699	0.9977	0.01	0.0156	0.9976	0.0007	0.1467	0.9976	0.0067
jpeg	0.0319	0.979	0.0024	0.211	0.9794	0.0163	0.0284	0.9751	0.0022	0.2349	0.9752	0.0118
Average	0.03	0.9947	0.0017	0.241	0.9947	0.0213	0.0262	0.996	0.0015	0.244	0.996	0.0165

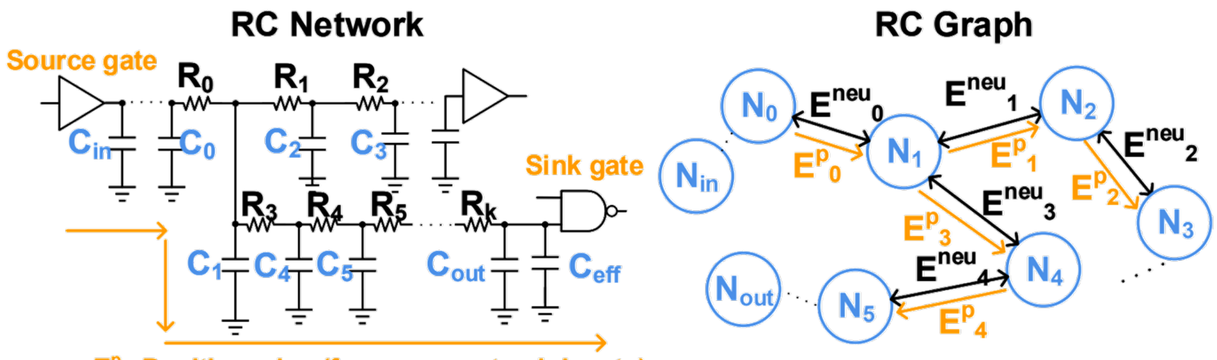
		DDPAS-G					NPAS				
Search Layer	Design (clk in ns)	TNS (ns)	WNS (ns)	Design Area (um^2)	Utilization (%)	Power (mW)	TNS (ns)	Worst Slack (ns)	Design Area (um^2)	Utilization (%)	Power (mW)
5	gcd (clk=0.45)	**-2.33**	-0.131	**722**	**20%**	**21.7**	-2.457	-0.131	738	21%	22.5
	dynamic node (clk=1.0)	**-3.465**	-0.139	29856	16%	39.3	-4.820	**-0.131**	**29559**	16%	**38.8**
	AES (clk=0.9)	**-0.134**	**-0.044**	25256	**8%**	66.7	-1.096	-0.075	**23318**	8%	**57.9**
	gcd (clk=0.5)	**-1.181**	**-0.077**	**736**	**21%**	**19.7**	-1.238	-0.085	770	22%	20.9
	APU (clk=1.0)	**-1.175**	**-0.07**	6652	9%	**9.11**	-2.227	-0.173	**6345**	**8%**	9.36
	BM64 (clk=2.0)	**0**	**0.074**	**29321**	3%	**22.8**	-0.842	-0.061	31067	3%	26.7
	picorv32 (clk=1.1)	**0**	**0.009**	21295	9%	**27.1**	-9.291	-0.545	**20839**	9%	28.1
	PPU (clk=1.0)	**-124.512**	-0.427	31912	3%	38.1	-523.987	-0.402	**30239**	3%	**36.4**
	salsa20 (clk=1.0)	**-441.337**	-1.254	53057	6%	121	-702.678	**-1.137**	**50978**	**5%**	**116**
	usb2p0 core (clk=0.6)	**0**	**0.029**	2425	1%	**7.27**	-0.008	-0.008	**2413**	1%	7.38
	wbqspiflash (clk=1.0)	**0**	**0.03**	4961	2%	**31.6**	-0.325	-0.036	**4648**	2%	35.6
	xtea (clk=1.0)	**-8.301**	**-0.285**	**6032**	3%	**17.7**	-11.034	-0.289	6339	3%	18.8
	yhuff (clk=1.0)	**-25.818**	**-0.187**	31346	14%	**34.1**	-4960.321	-3.676	**27882**	**12%**	36.8
	dynamic node (clk=1.1)	0	**0.08**	29752	16%	30.7	0	-0.043	**29541**	16%	**30.5**
10	gcd (clk=0.45)	**-2.33**	**-0.129**	**722**	**20%**	**21.7**	-2.457	-0.131	738	21%	22.5
	dynamic node (clk=1.0)	**-0.028**	**-0.011**	29856	16%	**33.9**	-4.82	-0.131	**29559**	16%	38.0
	AES (clk=0.9)	**-0.136**	**-0.036**	24754	**8%**	66.8	-0.266	-0.04	**23251**	8%	**64.1**
	gcd (clk=0.5)	**-1.089**	**-0.073**	**736**	**21%**	**18.7**	-1.238	-0.085	770	22%	20.9
	APU (clk=1.0)	**-1.175**	**-0.07**	6652	9%	**9.11**	-1.565	-0.119	**6538**	**8%**	9.33
	BM64 (clk=2.0)	**0**	**0.074**	**29321**	3%	**22.8**	-0.842	-0.061	31067	3%	26.7
	picorv32 (clk=1.1)	0	0.013	21271	9%	27.2	0	**0.099**	**20557**	9%	**26.7**
	PPU (clk=1.0)	**-124.512**	-0.427	31912	3%	38.1	-523.987	**-0.402**	**30239**	3%	**36.4**
	salsa20 (clk=1.0)	**-213.155**	**-0.969**	53057	6%	**103**	-702.678	-1.137	**50978**	**5%**	116
	usb2p0 core (clk=0.6)	**0**	**0.029**	2425	1%	**7.27**	-0.008	-0.008	**2413**	1%	7.38
	wbqspiflash (clk=1.0)	**0**	**0.03**	4961	2%	**31.6**	-0.154	-0.019	**4666**	2%	36.6
	xtea (clk=1.0)	**-8.301**	**-0.285**	**6032**	3%	**17.7**	-11.034	-0.289	6339	3%	18.8
	yhuff (clk=1.0)	**-25.818**	**-0.187**	31346	14%	**34.1**	-4960.321	-3.676	**27882**	**12%**	36.8
	dynamic node (clk=1.1)	**0**	**0.099**	**29541**	16%	**30.6**	-0.019	-0.019	29752	16%	35.6

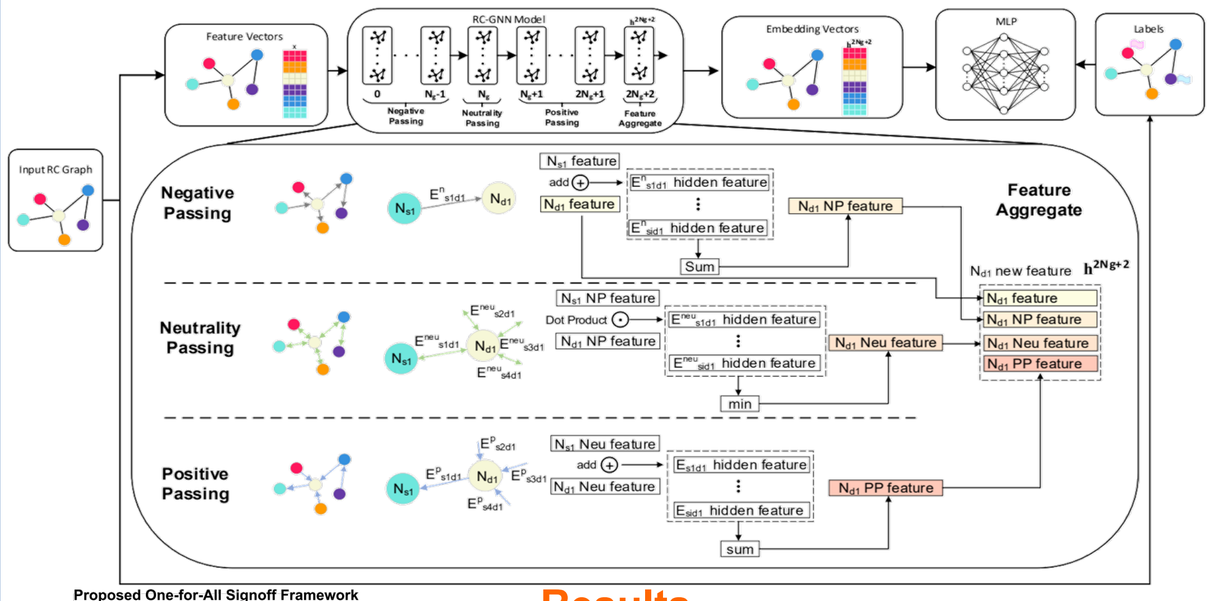
Shift left in single corner Timing Signoff [ICCAD ’24, AICAS ’23]

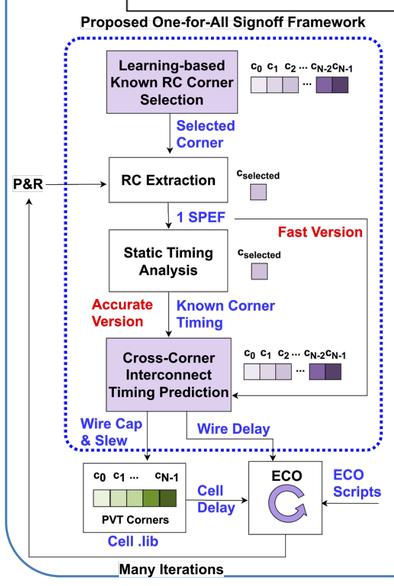
Main Idea

- Timing Signoff Challenges: High runtime, Many ECO iterations.
- From RC Network to RC Graph.
- RC-GNN Model.
- Integrated with ECO flow.









Results

	Iteration #1			Iteration #2		
Benchmark	fa	acc	Traditional ECO	fa	acc	Traditional ECO
B19	53	169	1574	53	172	1608
PCI_BRIDGE	70	147	1354	50	126	1154
DES_PERT	43	79	697	42	69	588
AES-128	42	112	1009	47	107	962
SALSA	53	127	1582	54	161	1502
GFX	50	100	1285	49	134	1228
Average	**51.83**	**122.33**	**1250.17**	**49.17**	**128.17**	**1173.67**