6.6kW Three-Phase Interleaved Totem Pole PFC Design with 98.9% Peak Efficiency for HEV/EV Onboard Charger

Xun Gong
System Engineer
Texas Instruments
Freising, Germany
x-gong@ti.com

Gangyao Wang
System Engineer
Texas Instruments
Cary, USA
gangyao-wang@ti.com

Manish Bhardwaj
System Engineer
Texas Instruments
Houston, USA
mbhardwaj@ti.com

***Abstract*—This paper presents the design and performance of a 6.6kW, three-phase interleaved, high density Totem Pole (TTPL) Power Factor Correction (PFC) based on SiC MOSFETs. The converter is operated at 100 kHz and in Continuous Conduction Mode (CCM). Key design features, components selection, and control scheme are discussed in detail. The digital controller enables phase shedding and adaptive dead-time control to improve the efficiency and power factor at light load. The SiC isolated gate driver is designed to have 4 A peak and 6A sink current and contains the two-level turn-off circuit for short-circuit protection. Experimental results from the 6.6kW design show that very high peak efficiency of 98.9%, and less than 2% THD are achieved at high line (240 V) AC input with 400 V DC output.**

Keywords—Totem Pole, PFC, SiC, CCM, OBC

I. INTRODUCTION

All plug-in hybrid electric vehicles (PHEVs) require an onboard charger (OBC) which connects to the power grid and delivers power to charge the high-voltage battery pack located inside the vehicle. Implementing a power factor correction (PFC) converter is mandatory [1] for reducing the current harmonics and maximizing the real power that flows to the downstream DC/DC converters. The PFC stage converts the single-phase AC voltage from power grid to a regulated DC voltage.

Before the emergence of wide-band-gap transistors, Si devices were the state-of-the-art power devices for PFC converters where passive diode bridge is used for rectification. The advantages of these diode based converters are: simple design, reliability, fast-system control loop, and low cost. However, the disadvantages are also very obvious: the passive components are bulky with a low-power factor and generate significant power losses. Investigation shows that an input bridge consumes approximately 2% of the input power at the low line of a wide input voltage application. If the designer can suppress one of the series diodes, then they can save 1% of the input power. Moreover, due to the poor reverse recovery property of Si super junction MOSFETs, current in reverse direction causes high losses , negative spikes and severe oscillations. As a result, the trend is to move towards bridgeless architecture with the elimination of the traditional diode bridge. The TTPL PFC gains significant popularity [2-6]. The biggest advantage is the reduced power losses in the conduction path. The superior performances of Silicon-carbide (SiC) MOSFET in terms of high voltage capability, very low reverse recovery, and decreased R_{dson}, position it the ideal power transistor candidate in this topology. A device comparison between the conventional bridged PFC and TTPL bridgeless PFC is shown in Table 1. As can be seen TTPL PFC conduction path concludes significantly reduced conduction losses.

TABLE I. DEVICE COMPARISON BETWEEN CONVENTIONAL BRIDGED PFC AND TTPL BRIDGELESS PFC

Parameter	*LF Diodes*	*HF Diodes*	*HF Switches*	*Conduction Paths*
Conventional bridged PFC	***Four***	***One***	***One***	***Two low-speed diodes + one switch or (two low-speed diodes + one high-speed diode)***
TTPL bridgeless PFC	***Two***	***Zero***	***Two***	***One high-speed SiC switch + one low-speed Si (or SiC) MOSFET***

This paper presents a 6.6 kW, three-phase interleaved Totem-pole PFC design based on SiC MOSFET and the C2000 Piccolo MCU (TMS320F280049). The design implements three phase interleaving, and operates in continuous conduction mode (CCM), achieving 98.6% efficiency at 240V input voltage and 6.6kW full power. The high-frequency SiC MOSFETs operate at a 100-kHz switching frequency and another pair of SiC MOSFETs operates at the line frequency (approximately 45Hz to 60Hz). Advanced techniques such as three phase interleaving, phase shedding and adaptive dead-time control are used to improve the efficiency and current ripple. The DC output voltage can be regulated in the range from 400V DC to 600V DC allowing for improved DC/DC converter efficiency at downstream of the OBC.

II. SYSTEM ARCHITECTURE AND HARDWARE DESIGN

System block diagram of the 6.6kW three-phase interleaved PFC design is shown in Figure.1, and following elements are included:

- Power switches G1-G6 are high-frequency SiC MOSFETs, for which there is a 120° phase shift between each two half bridge legs. G7 and G8 form the low-frequency (45-Hz to 60-Hz) synchronous rectifier bridge which virtually has no switching loss; a low conduction loss feature is desirable for these two devices.
- TMS320F280049M C2000 Piccolo controller functions as the controller, which has all the voltage and current sensor inputs and generates the correct PWM signals for G1-G8. The controller also reads any fault signal from the gate driver boards and shuts down the system if a fault occurs.

The reset function is used during start-up or when a fault is cleared.

- Hall sensors have been used to sense input total current and current for each channel. Voltage dividers are used to sense input line and neutral voltages as well as output DC bus voltages.
- The dual-channel isolated gate drivers to drive the SiC switches G1-G8 in half-bridge configuration. The gate driver features reinforced isolation, and provides more than 100 V/ns Common Mode Transient Immunity (CMTI). The driver contains the two-level turn off circuit, which protects the MOSFET from voltage overshoot during a short-circuit turn off scenario. The driver board includes two push-pull bias supplies which provide 15 V and –4-V output voltage and 1-W output power for driving the top and bottom SiC MOSFETs respectively.

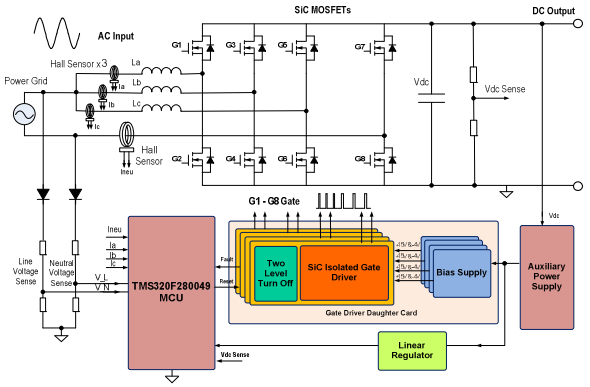


Fig. 1. 6.6kW three phase interleaved Totem-pole PFC block diagram

TABLE II. 6.6KW TTPL PFC SYSTEM SPECIFICATIONS

Parameter	Specifications
Input	• *Single phase AC gird* • *Voltage: ≈ 85-V AC_{RMS} to 265-V AC_{RMS}* • *AC line frequency range: 47 Hz to 63 Hz* • *Input current: 32 A_{RMS_MAX} at 240 V, 32 A_{RMS_MAX} at 120 V* • *Power factor: ≥ 0.99* • *Power line harmonics: < 2% at 240-V AC, full load*
Output	• *PFC output: ≈ 400 V to 600 V (adjustable)* • *Output power: 6.6 kW at ≈ 400 V to 600 V* • *Output capacitance: 900 µF* • *Output ripple: < 65 V* • *Peak efficiency: 98.86%*
Performance	• *PFC stage for high-voltage li-ion battery OBC* • *Three Phase Interleaving Power Stage* • *Switching frequency: 100 kHz* • *Isolation: Reinforced* • *Input AC sensing* • *PFC output voltage sensing*
Protection	• *Over temperature: > 75℃, stop work, and restores to work when < 75℃* • *Short-circuit protection* • *Overcurrent protection* • *Under-voltage protection at 80-V AC* • *Overvoltage protection at 265-V AC*
Working Environment	• *Ambient temperature: ≈ –40℃ to +85℃*

Key system specifications of the 6.6kW PFC is listed in Table 2. It implements three-phase interleaved power stage with phase shedding control for increased efficiency and operates in CCM mode, achieving a 98.60% efficiency at a 240-V input voltage and 6.6-kW full power. The output voltage is from 400V to 600V adjustable to interact with downstream OBC DC/DC converter.

A. SiC MOSFETs and Selection of Three phase Interleaving

The vehicle battery voltage ranges from 250 V to 450 V and the narrow DC gain variance is desired for the charger DC-DC stage, which typically uses a CLLC topology. Therefore, the output DC bus voltage has been selected as 400 V to 600 V for this PFC stage. The maximum DC voltage is 600 V plus approximately 20 V of ripple, which totals to 620 V. A 900-V or 1-kV rated power switch is also required. A 1-kV, 65-mΩ SiC MOSFET (C3M0065100K) has been selected as the high-frequency switching device to account for the reduced switching loss from the TO-247-4 package.

Multi-phase interleaving can both reduce the input current ripple and the conduction losses. To determine how many phases is an optimum solution, the PLECS simulation tool is used to simulate the power losses of the high-frequency power devices for different options. First, a loss model is developed based the characteristics of C3M0065100K which includes both conduction loss model and switching loss model over temperature. Secondly, full totem-pole PLECS simulation circuit is built and uses the previous model, then the power device losses can be simulated. The simulation is performed and compared for three cases: two-phase interleaving, three-phase interleaving and four-phase interleaving separately. The switching frequencies are chosen as 150kHz, 100kHz and 75kHz which gives the same 300kHz frequency for the input current ripple.

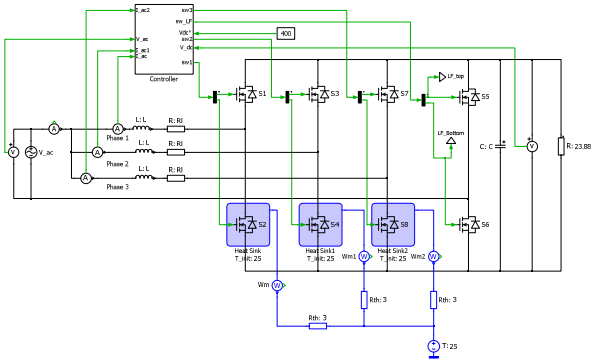


Fig. 2. Simulation model for Power Losses

TABLE III. SIMULATED TOTAL POWER DEVICE LOSSES

Output Voltage	*400V*	*500V*	*600V*
2 Phases Interleaving	*55.4W*	*66.8W*	*78W*
3 Phases Interleaving	*40.2W*	*49.5W*	*60W*
4 Phases Interleaving	*33.6W*	*43.2W*	*52.8W*

Table 3 summarizes the total device losses for the above three cases with output DC voltage as 400V, 500V and 600V respectively. It can be observed that the use of more phases reduces the total loss, but the difference between 3 phases and 4 phases interleaving is not significant, hence 3 phases interleaving design is selected for a good comprise of system efficiency and cost.

B. Inductor Calculation

The inductor plays important role in affecting system efficiency, current ripple, and overall size. The selection is always a balance between the efficiency and the power density. The inductance value is calculated based on the input voltage, output voltage, and worst case ripple. Calculation of the current ripple into inductor can be distinguished into three periods.

$$\begin{cases} I_{ripple} = [\frac{V_{in}}{L} - 2\times\frac{(V_{out}-V_{in})}{L}]\times D\times\frac{1}{F_{sw}} & \Leftarrow \quad when \quad 0 < D \le \frac{1}{3} \\ I_{ripple} = [\frac{2\times V_{in}}{L} - \frac{(V_{out}-V_{in})}{L}]\times (D-\frac{1}{3})\times\frac{1}{F_{sw}} & \Leftarrow \quad when \quad \frac{1}{3} \le D < \frac{2}{3} \\ I_{ripple} = (\frac{3\times V_{in}}{L})\times (D-\frac{2}{3})\times\frac{1}{F_{sw}} & \Leftarrow \quad when \quad \frac{2}{3} \le D < 1 \end{cases} \quad (1)$$

Where: I_{ripple} is the target input current ripple; V_{out} is the output voltage; V_{in} is the input voltage; D is the duty cycle; F_{sw} is the switching frequency; As the result, the inductance is calculated as 126µH at 12A RMS current.

C. Auxiliary Power Supply Design

The auxiliary power supply is powered from the PFC output. It is a flyback power supply based on UCC28700-Q1 that provides accurate constant voltage and constant current regulation with primary-side feedback, eliminating the need of opto-coupler which is not preferred in automotive environment. The controller operates in DCM with valley switching to minimize switching losses. The modulation scheme is a combination of frequency and primary peak current modulation to provide high conversation efficiency across the load range. Design parameters are shown in Table 4. The turn ratio of the transformer is calculated as:

$$N_{PS} = \frac{D_{MAX}\times V_{DC\_\min}}{D_{MAGCC}\times (V_{out}+V_F)} = 22.5 \quad (2)$$

Where: D_{MAX} is the maximum duty cycle, V_{DC_min} is the minimum input voltage, D_{MAGCC} is the conduction duty cycle of the secondary diode. V_F is the secondary diode voltage drop. N_{ps} is determined by the targeted maximum switching frequency at full load, at the minimum input bulk voltage, and the estimated Quasi Resonant (QR) time which is around 2µs. The resonant switching frequency is around 500 kHz.

D. Current and Voltage Sense

Hall-effect sensor is used for the total input current sensing, as shown in Figure 3. The operational amplifier circuit tunes the low output voltage of the sensor to higher level and sends to the controller Analog-to-Digital Converter pin. The three individual channels are sensed by the hall effect sensor ,which is intended for implementing load balancing scheme. The output voltage from the signal conditioning circuit is scaled to match the ADC range and calculated as:

$$I_{out} = \frac{R_f}{R_e}(I_{inv}\times\frac{V_{no\min al}}{I_{no\min al\_\max}} + V_{offset}) \quad (3)$$

TABLE IV. SPECIFICATIONS OF THE AUXILIARY POWER SUPPLY

PARAMETER		MIN	TYP	MAX	UNIT
INPUT					
V_{IN}	Input voltage	120	325	625	VDC
OUTPUT					
V_{OUT}	Output voltage(Non-Isolated)	4.75	5	5.25	VDC
P_{OUT}	Output Power		5		W
	Line Regulation (165V-400VDC)			<2%	
	Load Regulation (10% - 100% load)			<2%	
F_{MAX}	Maximum desired switching frequency			120	kHz
η	Targeted peak efficiency		86%		

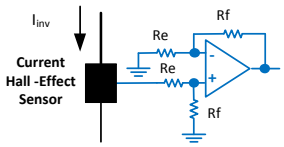


Fig. 3. Hall Effect Sensor Signal Conditioning Circuit

The input AC voltage is sensed differentially by sensing line and neutral inputs refer to the control ground separately with two voltage dividers. Since the control ground is the DC link negative terminal, the DC bus voltage can be sensed with a single voltage divider.

E. SiC Isolated Gate Driver Design

The gate driver needs to deliver high peak current in order to fully exploit the fast switching speed of the SiC MOSFETs. Negative gate-source voltage is required to safely turn it off. Besides, the driver requires high isolation between primary and secondary sides to avoid catastrophic failure. From layout point of view, the driver must be very tight and placed close to the SiC MOSFET to mitigate surge voltages, spike currents, and parasitic ringings[7-8].

The system implements isolated dual-channel gate driver with 4-A source and 6-A sink peak current capability [9-10]. The input side is isolated from the two output channels by a 5.7-kVRMS reinforced isolation barrier, with a minimum of 100-V/ns common-mode transient immunity (CMTI). A two-level turn-off feature is built up with discrete circuits, which protects the MOSFET from voltage overshoot during the short-circuit turn-off scenario. The desaturation (DESAT) detection threshold and the delay time for second stage turn-off are configurable.

The SiC isolated gate driver circuit is shown in Figure 4. The process of short-circuit protection mainly consists of three sub-periods: the blanking time, the delay and the two level turn-off. At the starting of the short circuit, the current flowing in the MOSFET channel increases dramatically until

saturation, and the voltage from drain to source also increases and can reach up to the DC bus voltage. During this transient, the SiC MOSFET is turned-on, and the lower section of the resistive divider (R18, and R26 as shown in Figure 4) is connected between the drain and source. The detection threshold is reached once the voltage at the Cathode of D6 is higher than its Anode and causes D6 in blocking direction. Then C34 starts being charged by the current which flows from the +15V power supply via the resistors R15 and R18. As the result, the values of R15, R18 and C34 determine the interval of the blanking time. The built-up voltage across C34 is compared with the voltage reference which is set by the precision shunt regulator TL431A-Q1. Once the voltage becomes higher than the reference, the comparator U8A sends the flag out and triggers the protection stage

After short-circuit is detected, the two level turn-off process starts. Once the voltage threshold is triggered, the 1st comparator (U8A) turns on Q2. Hence +5V is seen on the gate of Q1, and Q1 is conducted. The gate capacitor starts discharging exponentially through R13 and C25. The second level turn-off process is triggered by the output of the 2nd comparator U8B. This signal first goes through a delay time which is set by R22 and C36. After the delay time U8B is triggered. The U8B output is connected to the Enable pin of the UCC21521-Q1 gate driver. As the result the gate driver output is pulled down to the -4V and the SiC MOSFET gate is discharged to the same voltage level.

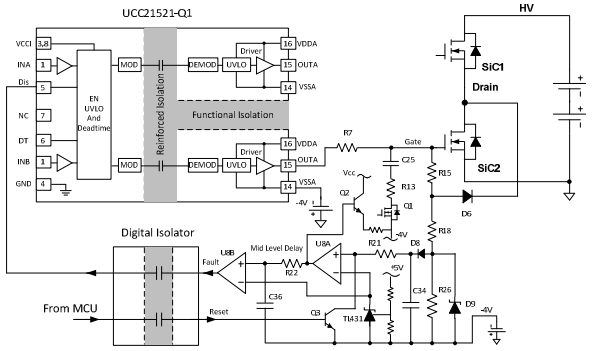


Fig. 4. Isolated Gate Driver Circuit

III. Control Scheme

The TMS320F28009 Piccolo MCU is optimized for real-time control application [11]. A fast and high-quality analog-to-digital controller (ADC) enables accurate measurement of the current and voltage signals. .

To modulate the current through the inductor, It is assumed that the direction of current is positive in the direction from the AC line into the rectifier and that the grid is fairly stiff when using the DC bus feedforward and the AC voltage feedforward [12-13]. The developed current loop model is shown in Figure 5. A proportional integral compensator is designed for the current loop. In the case of three interleaved phases, the current is simply three times more as the same duty cycle is provided to each leg [14]. The closed current loop model is given by the following equation.

$$H_{p\_i} = \frac{i_{Li}^{*}}{D} = 3 * \frac{1}{K_{v\_gain}} * K_{i\_gain} * K_{i\_fltr} * G_d * \frac{1}{Z_i} \quad (4)$$

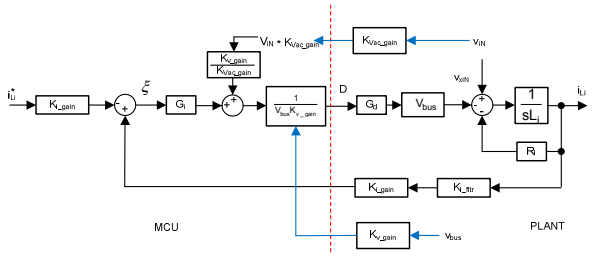


Fig. 5. Current Loop Control Model

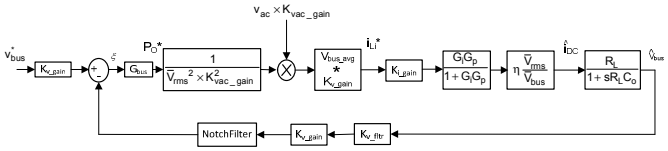


Fig. 6. DC Voltage Loop Control Model

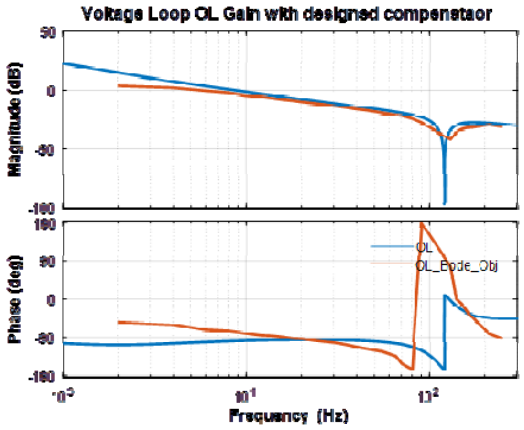


Fig. 7. Comparison of modeled and measured DC voltage loop

The DC bus regulation loop is assumed to provide the power reference. The power reference is then divided by the square of the line voltages RMS to provide the conductance, which is further multiplied by the line voltage giving the instantaneous current command. Small signal model of the DC bus regulation loop is developed by linearizing $\hat{i}_{DC}$ around the operating point. The derived loop model is shown in Figure 6. An additional DC bus feed forward is applied, which allows the control loop independent of the bus voltage, which is critical when operating the PFC in an OBC application as the bus is varied to make the DC-DC stage operate more efficiently. The plant model is thus given by the following equation:

$$H_{p\_bus} = H_{load} * \eta * \frac{1}{K_{i\_gain}} * K_{v\_gain} * K_{v\_fltr} * \left(\frac{K_{v\_gain}}{K_{vac\_gain}} \right) \quad (2)$$

Comparison of the measured and modeled bode plots for the voltage loop is shown in Figure 7, where the measurement is carried out using an in-circuit frequency

response analyzer [15]. As can be seen the two curves are matching closely with each other.

IV. Experimental Results

Figure 8 shows the picture of 6.6kW PFC prototype with outlined dimensions. Four gate driver daughter cards are plugged in to drive the SiC MOSFETs in four half bridges, and the three power inductors represent three interleaved channels. The DC link capacitor is formed by twenty four 350 V rating, 150µF capacitors with two in series and twelve groups in parallel. The power devices are under the PCB board and mounted on the cold plate. The design achieves the power density of 63.7 W/inch^3.

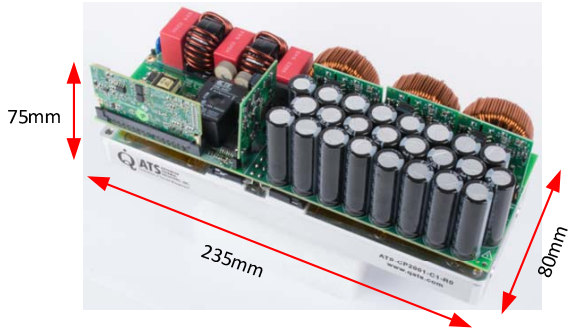


Fig. 8. 6.6kW PFC Prototype and Dimension

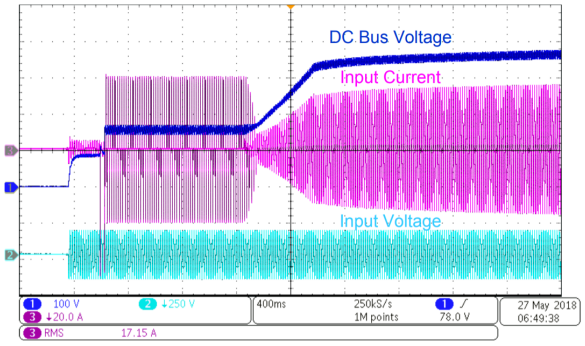


Fig. 9. Startup at 120-V AC input, 400-V DC output and 3.3kW load

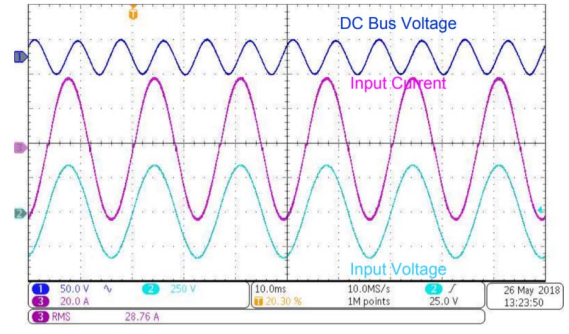


Fig. 10. Steady State Waveforms at 240-V AC input, 6.6kW load

Figure 9 shows the startup waveform with single AC phase input of 120-V AC and 400-V DC Bus output. The PFC is loaded with 3.3kW. There is about 1.5 second delay time till the relay is closed. During the period PTC resistors are connected in the loop to limit the inrush current and pre-charge the DC bus.

Figure 10 shows the stead state waveforms at 240-V AC input and 6.6kW full load. As can be seen the input current shape and phase follow tightly with the input voltage. The low frequency ripple with 100V peak to peak is observed at the output. The ripple voltage is reverse proportionally with the DC link capacitance.

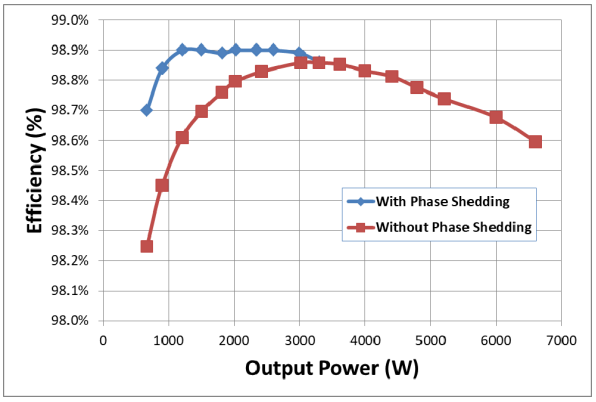
The measured detailed results of the PFC at 120VAC input and 240VAC input voltages and different power levels are summarized in Table 5 and Table 6 respectively. As can be seen very high power factor and low THD are achieved crossing the 6.6kW full load range.

TABLE V. Measured Detailed Results with 120VAC Input and at Different Power Levels

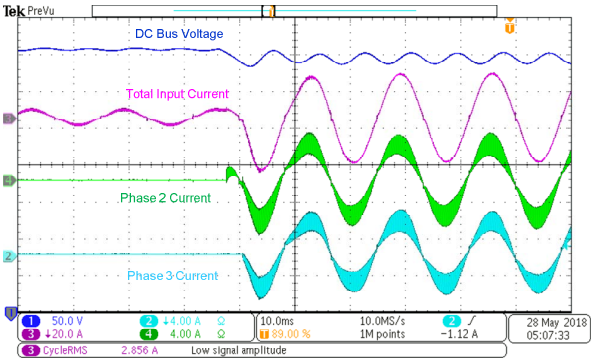
V_{in}(RMS)	P_{out}(W)	I_{out}(A)	Efficiency(%)	THD(%)	PF
120.2	333.45	0.834	96.33%	5.56	0.9940
119.92	617.74	1.544	96.91%	4.14	0.997
119.87	786.26	1.19	97.21%	3.75	0.9974
119.83	902.83	2.26	97.43%	3.37	0.9978
119.74	1201.65	3.0	97.67%	2.81	0.9984
119.69	1507.65	3.77	97.76%	2.44	0.9987
119.59	1816.88	4.54	97.77%	2.18	0.9989
119.50	2221.5	5.55	97.69%	1.95	0.9990
119.49	2423.94	6.05	97.63%	1.85	0.9991
119.43	2622.3	6.55	97.56%	1.77	0.9991
119.36	3018.6	7.54	97.42%	1.63	0.9992
119.28	3300.9	8.25	97.3%	1.56%	0.9992

TABLE VI. Measured Detailed Results with 240VAC Input and at Different Power Levels

V_{in}(RMS)	P_{out}(W)	I_{out}(A)	Efficiency(%)	THD(%)	PF
240.14	666.5	1.667	98.25%	12.39	0.9803
240.1	897.6	2.24	98.45%	7.3	0.992
240.1	1201	3.0	98.61%	4.06	0.9965
240.0	1507.27	3.769	98.7%	3.28	0.998
239.9	2021.48	5.05517	98.8%	3.06	0.9988
238.8	2622	6.55	98.81%	2.79	0.999
239.7	3296.7	8.24	98.86%	2.51	0.9993
239.6	3998.7	9.99	98.83%	2.21	0.9993
239.6	4406	11.01	98.81%	2.10	0.9994
239.5	5213.2	13.02	98.74%	1.89	0.9994
239.8	5602	14	98.71%	1.73	0.999
240.1	6601	16.5	98.60%	1.59%	0.9997



(a)



(b)

Fig. 11. (a) Comparison of efficiency with and without phase shedding (b) Phase shedding transition from 1 phase to 3 phases

Phase shedding is an important technique to increase the efficiency especially at light load. Figure 11 shows the measurements of: (a) the measured efficiency at 240V input, 400V output, with and without phase shedding. (b) Phase Shedding transition from 1 phase to 3 phases. As can be seen the PFC transitions smoothly from single phase to three phase operation. 98.9% peak efficiency is achieved with phase shedding being enabled.

V. Conclusions and Future Work

This paper presents the design, control and performances of a 6.6kW Totem pole PFC with 98.9% peak efficiency using SiC MOSFETs. Three phase interleaving is selected as the optimum operation point according to the simulation result. Calculation and selection of key component values are presented. The designed gate driver is in half bridge configuration with 4-A source and 6-A sink peak current capability, and contains built-in two-level turn-off feature which effectively protects the MOSFET from voltage overshoot during the short-circuit turn-off. Measurements show that maximum of 0.5% efficiency is improved with phase shedding at light load and reaches almost 99% peak efficiency. The C2000 Piccolo MCU provides full digital control with advanced features, such as phase shedding and adaptive dead-time control, greatly improves the system performance.

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