FPGA ACTIVE DIGITAL COCHLEA MODEL

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***Abstract*-Hearing is one of the senses of the human being and and is performed by the auditory system consisting of the outer and middle ear, cochlea (inner ear) and auditory cortex in the brain. The functionality of the cochlea is to process non-linear travelling wave and give information to the brain to perform tasks such as speech recognition and cross correlation of the incoming sound. This paper presents a model of a dual channel human cochlea embedded in a Xilinx XC3S500E, each consisting of a cascade of digital IIR low-pass filters. The filters are based on dual fixed point arithmetic. The model also integrates automatic gain control which mimics the functionality of the outer hair cells (OHCs), as well as the sensing mechanism involved in the inner hair cells (IHCs) of biological cochlea.**

Index Terms— Cochlea model, Automatic Gain Control, Human Auditory System, Inner Hair Cell (IHC), Outer Hair Cell (OHC).

I. INTRODUCTION

Efforts have been carried out to understand the functioning of the human body and more over such understanding was expressed in terms of mathematical computations in order to be able to model organs of the human body. A digital implementation on FPGA based on Lyon's Design of the human cochlea [1] is to be designed. The filter module consists of a cascade of 24 digital filters. This filter cascade mimics the behavior of the human cochlea where filter frequency cut-offs are set to start from higher to lower frequencies covering the human auditory frequency range of 20 kHz to 20 Hz. Digital models of the cochlea have already been documented in literature [2, 3, 4], however, the proposed model also incorporates an AGC mechanism built around a 4-bit digitally programmable gain amplifier (PGA), which mimics the OHC functionality. Furthermore, the model also implements the functionality of the IHCs which consists of signal differentiation and peak detection [5].

II. FILTER DESIGN

A. DESIGN

The filter design is based on a second order IIR topology which were designed starting from the continuous-time counterparts using the bilinear transform and uses DFX computation [2]. Two synchronized filter cascade channels were implemented in order to mimic the left and right ears of the biological system. Such a system allows further binaural processing to be carried out at a later stage, which could involve processing to determine the localization of a sound source.

III. FILTER CASCADE

A. CASCADE DESIGN

The FPGA cochlea model consists of a cascade of 24 IIR second order filter sections. Each of these filters is to be set to have a cut-off frequency in the range of 20 kHz to 20 Hz. The filter cut-offs are spaced in an exponential way as depicted in figure 1. The cascaded model of the cochlea is explained in figure 2, where the output taps are placed after every four filter sections. The on-chip 10 hardware multipliers are utilized for this purpose in a time-multiplexed manner.

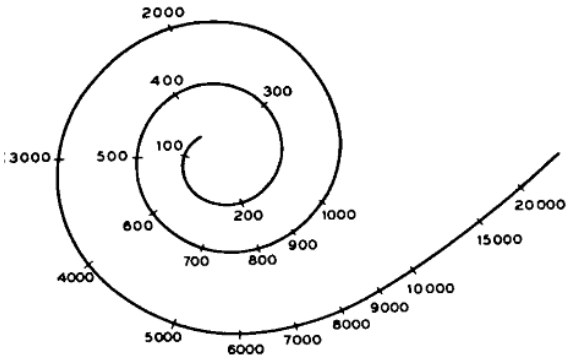

Figure 1 – Filter spacing along the cochlea, showing cut-off frequencies in Hz [6]

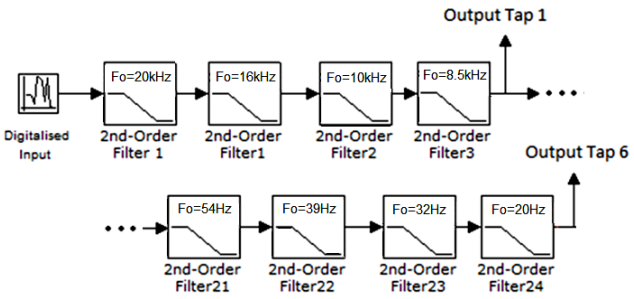

Figure 2 - Filter Cascade with output taps every four sections

B. DECIMATION

A sampling frequency of 80 kHz, was chosen for the ADC as well as the first 4 filter sections. However, this frequency is unpractical for use for stages operating at lower cut-off frequencies due to the limited precision of the resulting filter coefficients. A solution for this issue, which does not entail the use of increased hardware precision, is to use decimation [4], where stages operating at lower cut-off frequencies effectively operate at a lower sampling rate. The scheme adopted here was to reduce the sampling frequency by half after a filter stage consisting of four filters. Since the preceding stages effectively limit the frequency content of the signal input to subsequent stages, Nyquist Theorem is not violated.

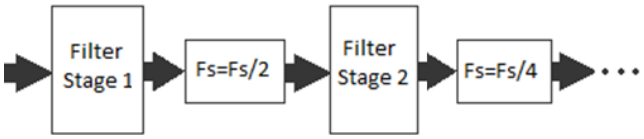

Figure 3 – Use of decimation in the fitler cascade.

IV. DATA AQUISITION

In the proposed system, audio analogue signals from two microphones are first amplified and then digitized using the analog capture unit, consisting of the two-channel PGA and ADC, available on the Spartan-3E FPGA Starter Kit board. Both devices are controller via an SPI bus [7]. The analogue capture unit accepts two inputs, derived from a preamplified microphone signal having a DC offset of 1.65 V.

A. PRE-PROGRAMMABLE AMPLIFIER

The onboard LTC6912-1 chip provides two independent inverting amplifiers with 4-bit SPI-programmable gain, which is ideal for the binaural model. The gain values for both amplifiers are set simultaneously via an 8-bit SPI command byte.

B. ANALOGUE TO DIGITAL CONVERTER

The onboard LTC1407-1 dual channel ADC is used to digitize the input signals with 14-bit representation. The ADC output is represented a 14-bit two's complement digital output, representing the values between -2^{13} and $2^{13}-1$. The ADC is read in sequential order; first channel 1 and then channel 2, in about 34 SPI clock cycles.

V. INNER HAIR CELL MODEL

In proposed FPGA digital model that mimics the functionality of the inner hair cells of the HAS was developed. Basically the IHC model differentiates the filter output and captures the highest peak signal. The functionality of the inner hair cells was analyzed in Meddis's [5] and Dau's [8] IHC models. The IHC model implemented broadly resembles Dau's model which was chosen due to its low hardware complexity requirement. . Since the inner hair cells, in the biological cochlea, are sensitive to the velocity of the incoming signal rather than displacement, a differentiation process is to be implemented before the rectification process. In the proposed model, the output from the filter cascade is differentiated, rectified and then passed through a peak detection module where the current output signal is compared to a previous value and if it is higher, the stored value is updated. The stored value decays in an exponential manner, however, in this implementation this was approximated by a linear decay. This process effectively changes the low pass function of the filters into a band-pass function and extracts the envelope magnitude of the resulting signal.

A compromise for the decay time-constant value was determined so that the IHC model output adequately follows the signal envelope while still attenuating high frequency content. Full wave rectification is preferred over half wave rectification since this also utilizes information in the negative half cycle. Hence in the digital domain, the process of rectification is essentially obtained by ignoring the sign of the signal and using just the magnitude part. A block diagram of the proposed digital model description can be seen in figure 4.

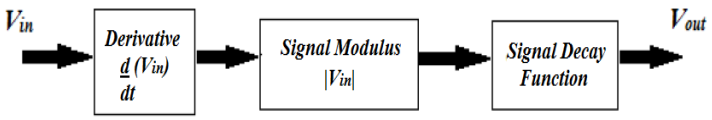

Figure 4 - IHC Model

VI. AUTOMATIC GAIN CONTROL

In the human auditory system, the OHCs provide adaptable amplification the incoming sound wave and effectively increase the dynamic range [9]. The automatic gain control implemented in this model, adjusts the gain such that the incoming audio signal is heard at constant level. When a low magnitude signal is presented to the system, the AGC mechanism implemented in the FPGA, increases the gain setting of the PGA so as to maximize the dynamic range of the ADC as well as the filter cascade. On the other hand when a strong signal is present the AGC mechanism reduces the PGA gain to a lower value. A feedback loop was designed so that the gain could be adjusted by comparing the current output with two pre-set thresholds. Figure 5 represents a block diagram of how the AGC is connected in the system.

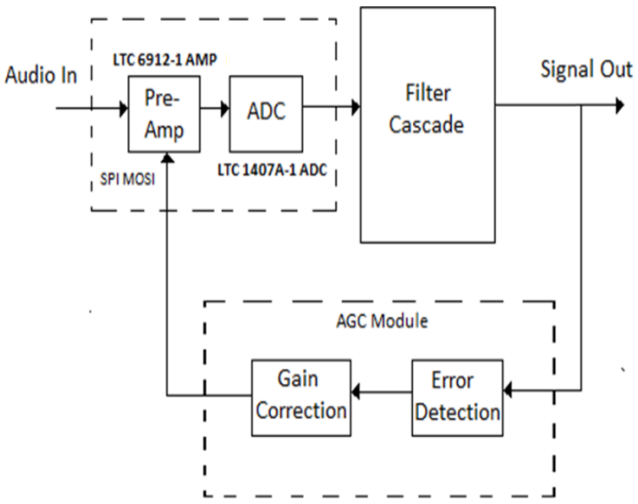

Figure 5 – AGC loop controlling PGA setting.

VII. RESULTS

A. FILTER IMPLEMENTATION

A single filter module was first implemented on the FPGA for testing purposes. Step input was given to the system and the filter output was expected to follow the given input. The resulting filter response, obtained using Xilinx Chipscope Pro can be seen in figure 6. From the results obtained it is concluded that the filter module has some steady state ripple which is due to the finite precision used in the computation.

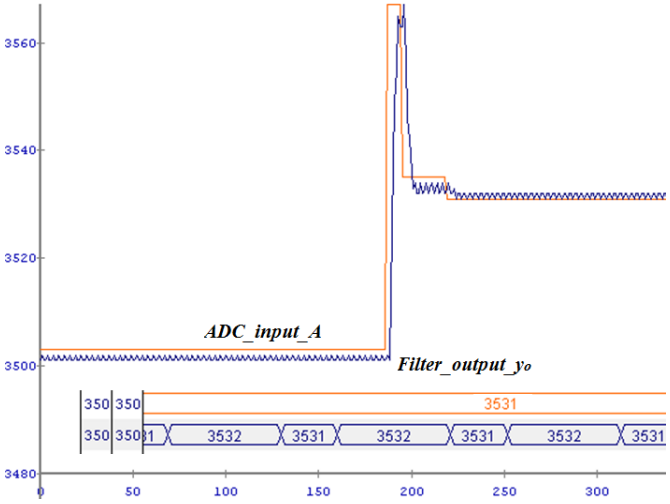

Figure 6 - Filter Implementation Result: The Filter output signal in response to a change in the ADC input.

B. CASCADED IMPLEMENTATION

The input of the filter cascade was connected with the ADC module. Thus, the first filter receives its input directly from the ADC while its output is fed as the input of the next filter in the cascade. For testing purposes, the first four filters in the cascade were considered. A DC input was utilized and the output taps were observed to follow this input. From the obtained results shown in figure 7 the value of the taps is slowly reaching the value of the input value.

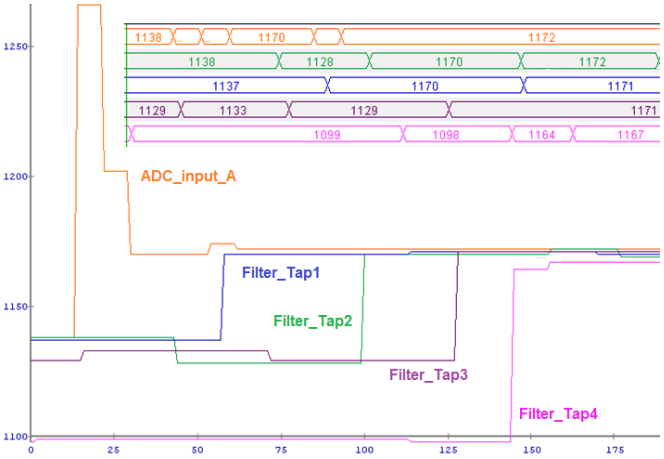

Figure 7 - Cascaded Implementation where output taps (blue, green, purple, pink) are following the DC input (orange).

C. AGC IMPLEMENTATION

The AGC module was simulated and implemented on the FPGA together with the filter module. Again, a step input was applied to the ADC. When the input magnitude is below the lower threshold magnitude, the gain is changed accordingly. As input is set back greater than the threshold, the gain setting of the PGA is reduced back to 1. The resulting AGC response is shown in figure 8.

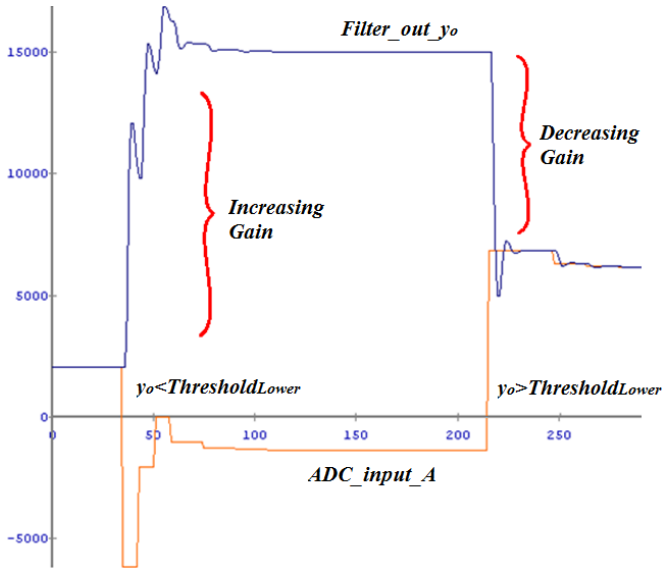

Figure 8 – AGC mechanism response showing variation PGA gain setting according to the input signal magnitude.

D. IHC MODEL IMPLEMENTATION

The output from the IHC model is expected to follow the peak value of differentiated signal and decay linearly until another peak is detected. The differentiated output from the filter was presented as input to the IHC model and the result was observed to reach the value of a detected peak together with a subsequent decay characteristic. The resulting plot can be observed in figure 8.

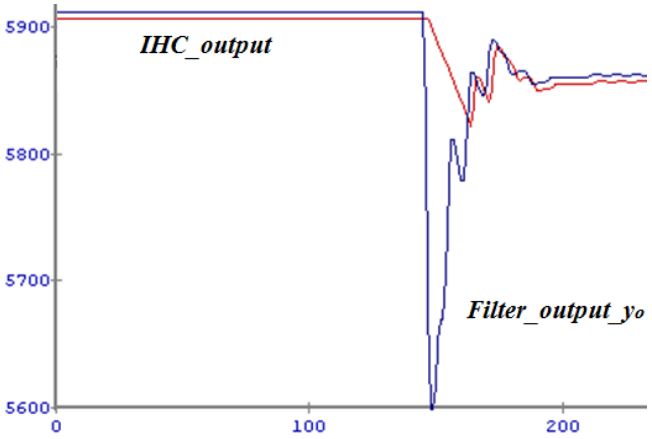

Figure 8 - IHC Model Behavior: the IHC output (red) detects a peak value from differentiated filter output and subsequently decays until another peak is detected.

VIII. CONCLUSION

To test the functionality and precision of the implementation a bottom up testing approach was utilized and therefore each of the modules and was tested on its own and when satisfying results were obtained the module was then connected with other modules and then the entire system with all modules was retested all together. Before implementing the system on the FPGA, simulations were carried out verifying that the filter cascade is covering the whole human auditory system range. The filter output response reached the given step input with within acceptable limits imposed by the precision of the DFX representation. Furthermore, when cascading the filters their response has shown the desired behavior to the applied step input. Decimation introduced in the system was beneficial to reduce the required hardware. The peak detection implemented mimicked the IHC model of the human ear obtaining a firing nerve signals. The AGC mechanism improved the sensitivity of the system to lower sound levels, thus increasing the dynamic range of the system, making its behavior similar to the human auditory system.

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