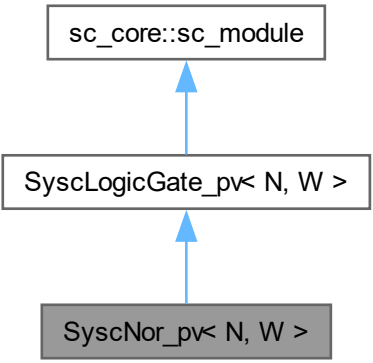


sc\_core::sc\_module



```
graph BT; A[SyscOr_pv< N, W >] --> B[SyscLogicGate_pv< N, W >]; B --> C[sc_core::sc_module];
```

SyscLogicGate\_pv< N, W >

SyscOr\_pv< N, W >