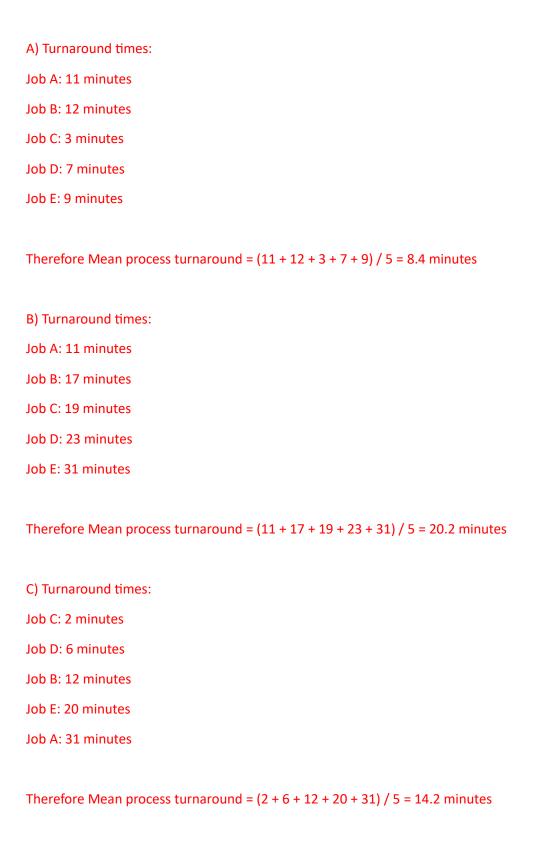
OS - Exercise 3

Question 1



Question 2

- (2.1) False. The decision of what is being kept in L1 cache is managed by the cache controller. The cache controller uses different cache replacement policies (such as Least Recently Used) which is based on usage patterns to determine which cache lines to keep in the L1 cache.
- (2.2) False. Changing the implementation does not guarantee a rise in hit rate. Fully associative cache can increase the complexity and the potential for conflicts. The impact on hit rate depends on other factors such as cache size, cache replacement policy, memory access patterns, and the workload being executed.
- (2.3) True. In a direct-mapped cache, each memory block can be mapped to only one cache line. However, in fully associative cache, any memory block can be mapped to any cache line, which requires additional storage in order to keep track of the mappings (of which memory block is associated with which cache line).

Question 3

I don't know

Question 4

a. B4E341B1

Binary: 10110100111000110100000110110001

Relevant bits for the block index: 101100011010000110100000110110001

Decimal representation (i.e the block index): 178

b. C2E87796

Binary: 11000010111010000111011110010110

Relevant bits for the block index: 1100001011101000011101111001

Decimal representation (i.e the block index): 200

c. D6312D0F

Binary: 11010110001100010010110100001111

Relevant bits for the block index: 1101011000110001001011010000

Decimal representation (i.e the block index): 173

d. 16FF913C

Binary: 000101101111111111001000100111100

Relevant bits for the block index: 00010110111111111001000100

Decimal representation (i.e the block index): 45