ECE 443
MIPS-16, Part 6:   Designing a 16-bit RISC style microprocessor
Lab #9:   PHYSICAL IMPLEMENTATION

Assigned	**April 18, 2023**
Demo due in lab	**April 18, 2023**
Makeup session:	**April 25, 2023**

Introduction
The goal of this laboratory is to implement your design in FPGA, using the Altera DE2 board.

Equipment:
1. Intel Quartus Prime software
2. Altera DE2-115 Development and Evaluation Board

Procedure:

1. Start from your Lab8 files; if you want, copy all the files in a new folder, create a new project. Don't forget to select the appropriate family of chips (Cyclone IV) and the appropriate device (the one that's actually used on the board).

2. Import assignments from an Excel assignment file (available on Blackboard).

3. Use one of the pushbutton switches (for example, KEY0) as a clock, so that you can step through your program once you download the configuration to the board.

4. Find your old EE343 code for seven segment displays and display the instruction that is currently being executed (hex code) on HEX3 – HEX0 (See "Help For Lab9.pdf"). If you did not take EE343 at UAF, contact the instructor for help.

5. Display some other information using red and green LEDs. For example, you can use red LEDs to display one of your 16-bit values (memory output, register file output, ALU output, etc.). Use green LEDs to display some other value – for example, a portion of a 16-bit signal, control signals, etc. Pick signals that will be most informative.

6. Change the names of the pins you would like to see on the board so that assignments are done automatically (optionally, you can manually map them). Compile the design. Enter the Chip Planner, look at the Net lists – use this opportunity (might be the last one for a while?) to examine the device.

7. Conduct a simulation of the design for the **exact Cyclone** chip used on the board. Show the appropriate input and output signals.

8. Burn (i.e., program) the device through the USB Blaster. Step through the program. Compare the display with the results obtained in step 7.

Requirements:
1. **No report** is required
2. Demonstrate the functionality to your TA/Instructor