ECE 443

MIPS-16, Part 4: Designing a 16-bit RISC style microprocessor

Lab #7: Completion and summary of components

Lab assigned: **April 04, 2023**
Report due **April 11, 2023**

Introduction
The goal of this laboratory is to consolidate the microprocessor components that have been designed in laboratory 4, 5 and 6. The microprocessor is a 16-bit machine that is based on the 32-bit Reduced Instruction Set Computer (RISC) machine that is presented in our textbook.

Equipment:
Intel Quartus Prime software

Procedure:
Carry out attached worksheet and exercises.

Worksheet:

1. The complete list of components expected from previous laboratory assignments is:
   `DCD3X8, MUX4X4, REG8, REG8X16, ADD4, AND_4, OR_4, PINV4, ALU4, ALU16, INCTWO, INS_MEM, DAT_MEM, SGNEXT6X16, SHLONE, ADD16, MUX3X16.`
   Make sure that you have all these components and that they are working as they are supposed to.
2. Design three new components:
   a. a 2-input 16-bit multiplexer **`MUX2X16`**,
   b. a 2-input 3-bit multiplexer **`MUX2X3`**,
   c. a functional unit that combines the **3 most significant bits** of PC with the 12 bits of the jump address and a '0' (i.e., multiply by 2); let's call it **`PCJMP`**.
3. Compile and simulate these components and add them to Table 1. Also add the following components designed in previous labs: REG8x16, ALU16, INS_MEM, DAT_MEM. If you need to, recompile them for the exact chip that's on the board we are using. List the components used in each device (if any). Give the range of propagation delays for each device; choose the minimum and maximum of all the delays listed in the timing analyzer.
4. Take another look at REG8X16 and set it up so that some registers always return a constant value (specifically, hardwire R0 to 0x0000 and R7 to 0x0100).
5. Download Figure 4.17 from Blackboard and annotate it with the names of each of the components you have designed. Make sure you have all the components. Where the components differ from those of P&H (e.g., adding 2 to the program counter instead of 4, etc.) annotate the figure appropriately. Include it in your report.
6. If you made some design choices (for example, changing the pin names, adding new pins, getting rid of some pins, etc.) please list those changes in your report.

Requirements:

1. The report should include all newly designed files.
2. The report should include **annotated** simulation files verifying that the three new machines work as designed.
3. The report should include the completed Table 1.
4. Send all the *.vhdl and *.vwf files to your TA.

TABLE 1. MIPS-16 COMPONENTS – An example

VHDL Filename	Description	Components	Logic cells used	Propagation delay range [ns]
MUX2X16	2-input 16-bit multiplexer	none	16	7.1 – 10.7
…				
REG8X16	8-by-16 register file (8 16-bit registers) with one input port (write) and two output ports (read)	DCD3X8 MUX4X4 REG8	168	10.0 -12.5 (read)
…				