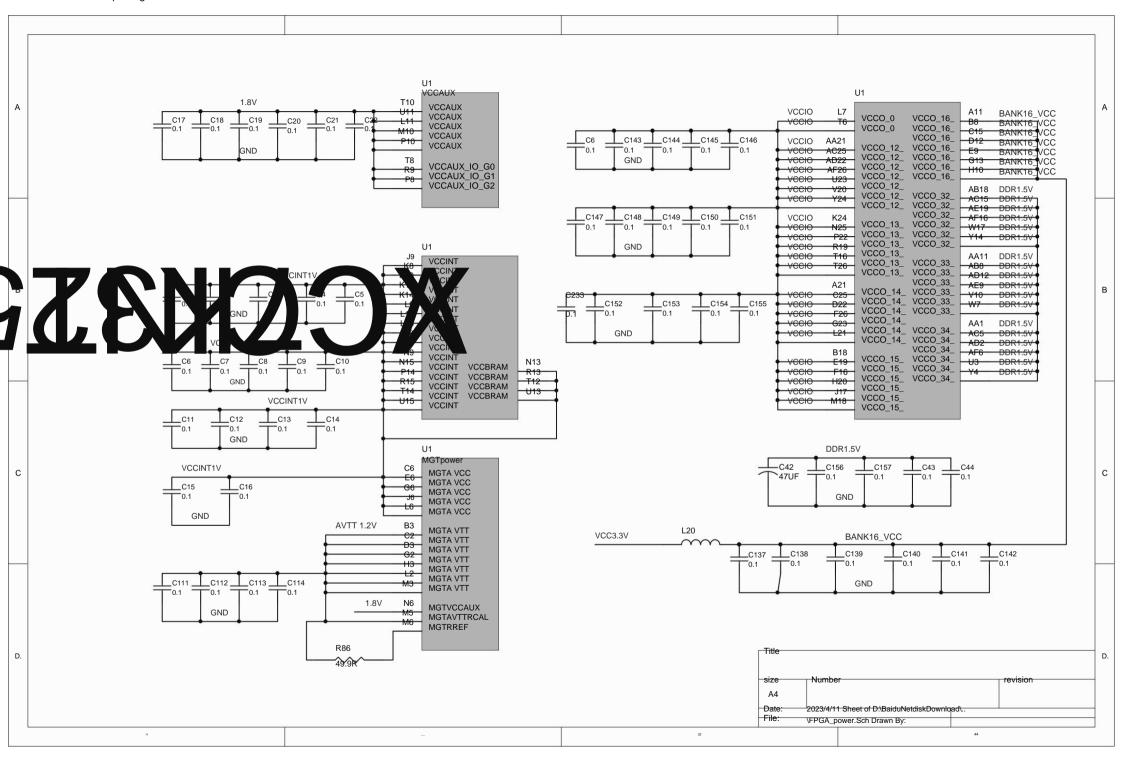


1 2	3 4	
A Out_HDMI_D2P	VCC3.3V R146	A B
C PIN C16 C16 PIN B16 B16 PIN A18 A18 PIN A19 A19 PIN B17 B17 PIN B17 B17 PIN C19 C19 PIN B19 B19 PIN B19 B19 PIN C17 C17 PIN C18 C18 PIN C18 C18 PIN D15 D15 PIN D15 D15 PIN D16 D16 PIN G16 G16 PIN G17 G17 PIN G16 G16 PIN G15 G15 PIN G15 G15 PIN G15 G15 PIN G15 G16 PIN G15 G16 PIN G16 G16 PIN G15 G15 PIN F15 F15 PIN F15 F15 PIN F15 F15 PIN F15 F15 PIN F115 J15 PIN F116 J16 PIN G16 G16 PIN G15 G15 PIN F15 F15 PIN F116 J16 PIN G16 G16 PIN G15 G15 PIN F15 F15 PIN F15 F15 PIN F15 F15 PIN F15 F15 PIN F116 J16 PIN G16 G16 PIN G15 G15 PIN F116 J16 PIN F116 J16 PIN G17 C17 PIN G18 G16 PIN G15 G15 PIN F116 J16 PIN F116 J16 PIN F116 J16 PIN F116 J16 PIN G15 G16 PIN F116 J16 PIN G15 G16 PIN F116 J16 PIN F116 J16 PIN G17 C17 PIN G17 C17 PIN G17 C17 PIN G18 G16 PIN G18 G18 PIN	H17 PIN H17 H18 PIN H18 D19 PIN D19 S D20 PIN D20 G19 PIN G19 F20 PIN F20 F19 PIN F19 E20 PIN F20 H19 PIN H19 G20 PIN G20 G3 K20 PIN K20 J18 PIN J18 J19 PIN J19 L19 PIN L19 L10 PIN L20 L20 PIN L20 P	c
PIN FJ16 J16 PIN E15 E15 PIN E16 E16 PIN G17 G17 PIN F18 F18 CLK50M F17 PIN E17 E17 PIN E17 E17 PIN K15 K15 D. L12P_T1_MRCC_AD5P D. D	K16	D. revision

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A			A
B DATA0 SD U22 CLK SD V22 PIN U24 PIN U25 PIN U25 PIN V23 PIN V24 PIN V24 PIN V24 PIN U26 PIN V26 PIN V26 PIN W26 PIN A825 PIN A825 PIN A825 PIN A825 PIN A826 PIN A827 PIN A828 PIN A828 PIN A828 PIN A829 PIN A829 PIN A821 PIN A824 PIN A8	N_TO	PIN P24 P24 PIN N26 N26 PIN N26 N26 PIN M26 M26 PIN M26 M26 PIN R25 R25 PIN P25 P25 PIN N19 N19 PIN M20 M20 PIN M24 M24 PIN L24 L24 PIN L24 L24 PIN P19 P19 PIN P20 P20 PIN P20 P20 PIN M21 M21 PIN M21 M21 PIN M22 M22 PIN M22 M22 PIN M21 M21 PIN M22 M22 PIN P33 P23 PIN N23 N23 PIN N21 N21 N21 PIN N21 N21 N21 PIN N22 N22 PIN N21 N22 N22 PIN N22 N22 PIN N23 N23 PIN N21 N21 N21 PIN N22 N22 PIN N23 N23 PIN N21 N21 N21 PIN N22 N22 PIN N22 N22 PIN N23 N23 PIN N21 N21 N21 PIN N22 N22 PIN N22 N22 PIN N23 N23 PIN N21 N21 N21 PIN N22 N22 PIN N22 N22 PIN N23 N23 PIN N21 N21 N21 PIN N22 N22 PIN N22 N22 PIN N23 N23 PIN N22 N22 PIN N23 N23 PIN N23 N23 PIN N21 N22 PIN N22 N22	2_MRCC R22 PIN R22 12_SRCC R23 PIN R23 12_SRCC R23 PIN R23 12_SRCC T24 PIN T24 T2_DQS T25 PIN T25 N_T2_DQ T20 PIN T20 _L16P_T2 R20 PIN R20 _L16N_T2 T22 PIN T22 _L17P_T2 T23 PIN T23 _L17P_T2 T23 PIN T23 _L17N_T2 U19 PIN U19 _L18P_T2 U20 PIN U20 _L18P_T3 T19 PIN T18 _L19P_T3 T19 PIN T18 _L19P_T3 T19 PIN T19 3_VREF P16 PIN P16 _L20P_T3 N17 PIN N17 _L20N_T3 R16 PIN R16 _T3_DQS R17 PIN R17
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i		
ĺ	U1	
i	XC7K325T676 BANK32 U1 ddr3-B dd1 AE17 AC18 ddr3-B dd16 XC7K325T676 BANK33	
	10.11 TO 10.113 T2 MRCC AD18 01.35 Util 10.11 T0 10.113 T3 MRCC AD18 01.35 Util 10.11 T0 10.113 T3 MRCC	AB11 CLK200_P
Α	Hed 65 W11 IO_LIN_IU IO_LISN_IZ_MIRCU AB17 Ud.38_ud19 Hed 65 W11 IO_LIP_IU IO_LISN_IZ_MIRCU AB17 Ud.38_ud19 Hed 65 W11 IO_LIP_IU IO_LISN_IZ_MIRCU	AC11 CLK200_N A
	4015-8 dqs0-p	AB10 data B data
	tdi3-B_dqs0_n AF18	AC42 UUI3-D_AT4
	4545 10 14P T0 10 116P T2 4400 4013-5-4421 4013-	AA12 ddr3-B_AT5
	10 L5P T0 IO L17P T2 AC19 ddi3-B_dq23 ddi3-B_tas	AA12 ddr3-B_odt0
	ddi.5-B dm0 AD16 IO_L5N_T0 IO_L17N_T2 AB19 ddi.3-B dm2 led d3	AD13
	0.75_VRF2 AB46 O_L6P_110 O_L18P_12 AB20 did3-8_reset	Y13 ddr3-B_odt1
	AAAF IO L7P T1 IO L19P T3 V49	AD11
	B dq8 ddr3- AC14 IO_L7N_I1 IO_L19N_I3_VKEF V46 Udr3-B_dq28 Udr3-B_A13 AF7 IO_L7P_I1 IO_L19N_I3_VKEF V46 Udr3-B_dq28 Udr3-B_A13 AF7 IO_L7N_I1 IO_L19N_I3_VKEF V47 Udr3-B_dq28 Udr3-B_A13 AF7 IO_L7N_I1 IO_L19N_I3_VKEF V46 Udr3-B_dq28 Udr3-B_A13 U	AB10 ddr3-B_A5
	5_d[10 dd]3-	AE10 lod d4
	8 dqs1_pddi3-	AE12
	D_SQ471	AF8 dds B box
	ddi3-B_dq13 AA17	AF8 ddr3-B_we
В	B Gaille D-sign AR16 IO_L11N_T1_SRCC IO_L23N_T3 V/14 Gaille D-sign Gaille D-sign AR0 IO_L11P_T1_SRCC IO_L23P_T3	AF13
	Hold Heaville Hold Heaville Hold	AF10 ddr3-B_A3
	IO_0_VRN_32	V12
	IO_0_VRN_33 IO_25_VRP_33	
	R38 DDR 1.5V	R87
	★ ★9.9 ~	> 49.9
	U1 U1	}
	XC7K325T676 BANK34	
	ddr3-B_dq33	
	ddi3-B_dq35 	
	INC. I IO L2N TO IO L14N T2 SRCC AAS	
	ddi3-B_dqs4_11 W6 IO_L3P_1L_2Dd3 \ AB6 \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	
	Udi 3-5_4430	
С	O O O O O O O O O O	C
	duis-b_uqs9 V4 IO L5N TO IO L17N T2 Apg duis-b_uqs5	
	0.75_VRF1 W4 IO_16P_T0 IO_18P_T2 AD5 led d1 AD4	
	10 L7P T1 10 L19P T3 AD2 0.75V L7	
	ddi3-B_dq42	
	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	
	ddi3-B_dqs5_n AC1	
	V1 10 L10P T1 10 L22P T3 AE2	
	ddi3-B_dq46 AB2	
	ddi3-B_dq47 AA2 IO L11N T1 SRCC IO L23N T3 AE2 ddi3-B_dq01	
	10_12P_T1_MRCC	
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	1	2	3	4
A		U1	U1	A
В	Sfp. A. tx. P Sfp. A. tx. n Sfp. A. tx. n Sfp. A. rx. p Sfp. A. rx. n Sfp. B. tx. p Sfp. B. rx. p Sfp. B. rx. p Sfp. B. rx. n Sfp. B. rx. p Sfp. B. rx. n B-SATA TX. P B-SATA TX. N B-SATA RX. P B-SATA RX. P A-SATA TX. P A-SATA TX. N	XC7K325T676 MGT BANK115 H1 J4 J3 MGTXTXN3_115 MGTXTXN3_115 MGTXTXN3_115 MGTXTXN3_115 MGTXTXP2_115 MGTXTXN2_115 MGTXTXN2_115 MGTXTXN2_115 MGTXTXN2_115 MGTXTXN2_115 MGTXTXN1_115 MGTXTXN1_115	MGTXTXP3_116 MGTXTXP2_116 MGTXTXP2_116 MGTXTXP2_116 MGTXTXP2_116 MGTXTXP2_116 MGTXTXP2_116 MGTXTXP2_116 MGTXTXP2_116 MGTXTXP3_116 MGTXTXP3_116 MGTXTXP3_116 MGTXTXP1_116 MGTX	В
С	CLK_N clock is not input by default. CLK_P can use Y3 input clock pcie_ck+ pcie_ck	K5 H6 H5 MGTREFCLK1P_115 MGTREFCLK0P_115 MGTREFCLK0N_115 MGTREFCLK0N_115	CLK150 N F5 CLK156.25 P D6 CLK156.25 N D5 GLK156.25 N D5 MGTREFCLK1P_116 MGTREFCLK0P_116 MGTREFCLK0N_116	C
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