d) In digital system... that the circuitry used to ...
e) None of the above

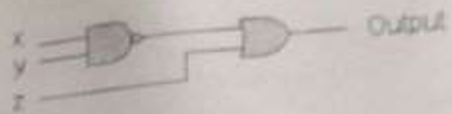
4. What type of logic gate is this?

a) 3 Inputs OR
b) 3 Inputs AND
c) 3 Inputs NOR
d) 3 Inputs NAND
e) none of the above

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

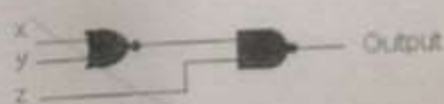
5. What function is implemented by the circuit shown

a) $\overline{x}.\overline{y}+z$
b) $(\overline{x}+\overline{y})z$
c) $\overline{x}.\overline{y}.z$
d) $\overline{x}+\overline{y}+z$



6. What function is implemented by the circuit shown

a) $x+y+z$
b) $x+y+\overline{z}$
c) $\overline{x}.\overline{y}.z$
d) $\overline{x}+\overline{y}+\overline{z}$



7. What function is implemented by the circuit shown

a) $xz+y$
b) $\overline{x}.z+\overline{y}$
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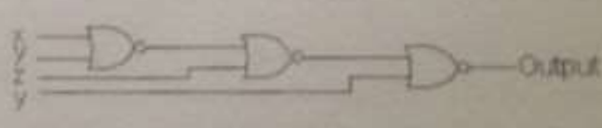

8. Use Boolean algebra to simplify the logic function $A+(\bar{A}.B)$
(a) $A.B+\bar{A}$

valuations for input switches A, B and C that generate a 1 at the output: (A=1, B=1, C=0), (A=1, B=0, C=1), (A=0, B=1, C=1).

i. Complete the truth table
ii. Write the Boolean expression
iii. Draw the Logic circuit

A	B	C	output
0	0	0	
1	1	0	
1	0	1	
0	1	1	

F. K AMPONG

Appendix A

Single-Variable Theorems

1a. $x \cdot 0 = 0$

1b. $x + 1 = 1$

2a. $x \cdot 1 = x$

d) In digital systems, the convenient feature of using ONLY TWO voltage levels is that the circuitry used to generate, manipulate and store them is very simple

e) None of the above

4. What type of logic gate is this?

a) 3 Inputs OR
b) 3 Inputs AND
c) 3 Inputs NOR
d) 3 Inputs NAND
e) none of the above

A	B	C	X
[illegible]	[illegible]	[illegible]	[illegible]

5. What function is implemented by the circuit shown

a) $\overline{x}.\overline{y}+z$
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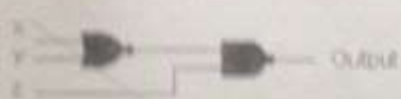

What function is implemented by the circuit shown

a) $xz+y$
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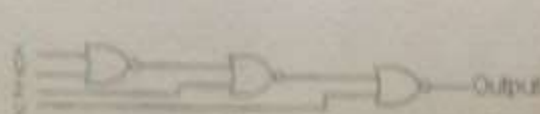
c) $\overline{x}.\overline{y}+\overline{y}.\overline{z}$
d) $\overline{x}.\overline{y}+\overline{y}.z$



Use Boolean algebra to simplify the logic function $A+(\bar{A}.B)$

(a) $A.B+\bar{A}$

Index number.... 6225111

March 2014

TIME : 1 Hr

Answer all questions
Answer section A on the question paper and section B in your answer booklet.
(Find attached: Appendix A - list of Boolean algebra theorems)

Section A [10 Marks]

1. Digital circuits play a very important role in today's electronic systems. They are employed in almost every facet of electronics, excluding,
   a) Control Instrumentation
   b) Communication
   c) Computing
   d) Amplification of weak signals
   e) None of the above

2. A logic gate is:
   a) A special type of amplifier circuit designed to amplifier voltage signals corresponding to binary 1's and 0's.
   b) A special type of amplifier circuit designed to amplifier current signals corresponding to binary 1's and 0's.
   c) A special type of voltage amplifier circuit designed to generate voltage signals corresponding to binary 1's and 0's.
   d) A special type of amplifier circuit designed to accept and generate voltage signals corresponding to binary 1's and 0's.
   e) None of the above

3. Which of the following statements about a logic gate is false?
   a) Gate circuits are most commonly represented in a schematic by their own unique symbols rather than by their constituent transistors and resistors.
   b) Logic circuits provide solution to a problem. They implement functions that are needed to carry out specific tasks
   c) Within the framework of a computer, logic circuits do not provide complete capability for execution of programs and processing of data.

(b) A + B
(c) $\bar{A} + A$
(d) $\bar{A}.A$

9. Use Boolean algebra to simplify the logic function $A.(B + \bar{B}.C)$.
(a) A.(B + C)
(b) $A + \bar{B}$
(c) A.C + B
(d) A + B.C

10. Simplify the logic function F = (B+A).(B+C)
(a) B+A.C
(b) B.A+B
(c) (A+B).(B.C)
(d) C+A.B

SECTION B [10 MARKS]

ANSWER ALL QUESTIONS FROM THIS SECTION IN YOUR ANSWER BOOKS

11. Draw the Logic circuit that would be used to implement the following Boolean equations

a) P = (AC + BC)(A + C)
b) R = BC + D + AD
c) S = B(A + C) + AC + D

12.

INPUT			OUTPUT
C	B	A	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Let us assume that we are designing a simple electronic lock. The lock will open only when certain switches are activated. A 1 at the output will open the lock. There are three

EXERCISE 2

1. In MOSFET the current control mechanism is based on an ______________ established by the voltage applied to the control terminal.
   (a) <u>Electric field</u>
   (b) Induction layer
   (c) Induced field
   (d) None of the above

2. In the n-channel depletion-type MOSFET, the threshold voltage is
   (a) The value of the Gate-to-source voltage at which the channel is completely depleted of electrons.
   (b) The value of the Gate-to-source voltage at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel.
   (c) The value of the saturation voltage.
   (d) The inversion layer voltage

3. What is an inversion layer?
   (a) <u>An induced channel</u>
   (b) A depletion layer
   (c) A pn junction
   (d) The gate electrode

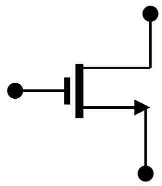
4. For the JFET to operate in the pinch-off
   (a) The drain voltage must be greater than the gate voltage by at least $|V_p|$.
   (b) The source voltage must be greater than the drain voltage by –Vp.
   (c) The gate voltage must be less than the source voltage by –Vp
   (d) <u>None of the above</u>.

5. The conduction of the channel is proportional to
   (a) The pn junction voltage between the source and the drain.
   (b) <u>The excess gate voltage</u>
   (c) The threshold voltage
   (d) The inversion layer voltage

6. The maximum value of the gate-to-source voltage in an n-type JFET is
   (a) –1 V
   (b) +1 V
   (c) <u>0 V</u>
   (d) 0.7 V

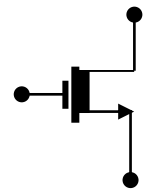
Give the names of the following circuit symbols.

7.



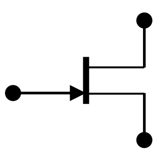
n-channel Enhancement MOSFET

8.



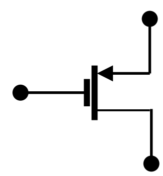
n-channel Depletion MOSFET

9.



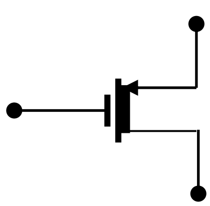
n-channel JFET

10.



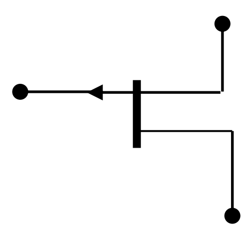
p-channel Enhancement MOSFET

11.



p-channel Depletion type MOSFET

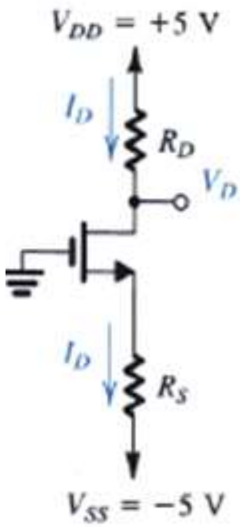
12.



p-channel JFET

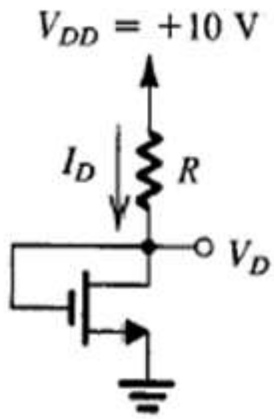
Example 1

Design the circuit of fig.1 so that the transistor operates at I_D = 0.4mA and V_D = +1V. The NMOS transistor has Vt. = 2V, μ_nC_{ox} = 20μA/V^2, L = 10 μm, and W = 400 μm. neglect the channel-length modulation effect (i.e. assume λ = 0).



Example 2

Design the circuit in fig. 2 to obtain a current I_D of 0.4mA. give the value required for R and find the dc voltage V_D. Let the NMOS transistor have Vt. = 2 V, μ_nC_{ox} = 20 μA/V^2, L = 10 μm, and W = 100 μm. neglect the channel-modulation effect (i.e. assume λ = 0).



$V_{DD} = +10$ V
I_D
R
V_D

Digital circuits

Short quiz 1

1. What is meant by the term analog, with regards to an electronic circuit?

2. What is meant by the term digital, with regards to an electronic circuit?

3. A NOT circuit is also called a/an ……………………..

4.

INPUT			OUTPUT
C	B	A	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

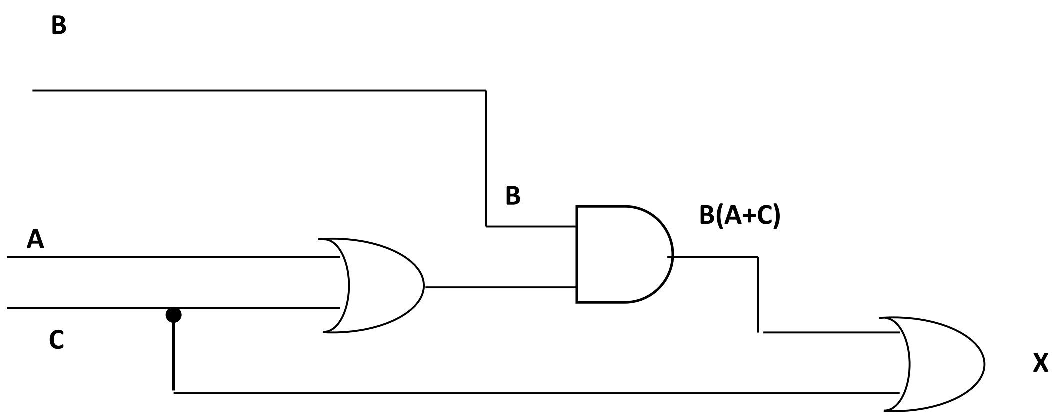
Let us assume that we are designing a simple electronic lock. The lock will open only when certain switches are activated. The figure above is a truth table for the electronic lock. Notice that there are two valuations for input switches A, B and C that generate a 1 at the output. A 1 at the output will open the lock.

i. Write the Boolean expression
ii. Draw the Logic circuit

5. A certain application requires that two lines be monitored for the occurrence of a HIGH level voltage on either or both lines. Upon detection of a HIGH level, the circuit must provide a LOW voltage to energize an alarm circuit.

i. Design the truth table
ii. Write the Boolean expression
iii. Draw the Logic circuit

6. The logic circuit shown below is used to turn on a warning buzzer at "X" based on the input conditions at A, B, and C. A simplified equivalent circuit that will perform the same function can be formed by using Boolean algebra. Write the equation of the circuit, simplify the equation and draw the logic circuit of the simplified equation.



7. Write the Boolean logic equation and draw the logic circuit that represents the following function:

   A Bank burglar alarm (A) is to activate if it is after Banking hours (H) and the front door (F) is opened or if it is after Banking hours (H) and the vault door (V) is opened.

The logic level of the variable H is "1" after Banking hours and "0" during Banking hours. F is "1" if the door sensing switch is open and "0" if the door sensing switch is closed. V is "1" if the vault sensing switch is open and "0" if the vault sensing switch is closed.

d) In digital systems, the convenient feature of using ON/OFF voltage levels is that the circuitry used to generate, manipulate and store them is very simple
e) None of the above

4. What type of logic gate is this?

a) 3 inputs OR
b) 3 inputs AND
c) 3 inputs NOR
d) 3 inputs NAND
e) none of the above

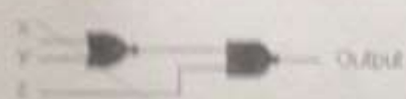
A	B	C	[illegible]	X
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

5. What function is implemented by the circuit shown

a) $\overline{x}.\overline{y}+z$
b) $(\overline{x}+\overline{y})z$
c) $\overline{x}.\overline{y}.z$
d) $\overline{x}+\overline{y}+z$

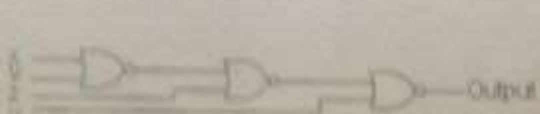
6. What function is implemented by the circuit shown

a) $x+y+z$
b) $x+y+\overline{z}$
c) $\overline{x}.\overline{y}.z$
d) $\overline{x}+\overline{y}+\overline{z}$



What function is implemented by the circuit shown

a) $xz+y$
b) $\overline{x}.z+\overline{y}$
c) $\overline{x}.\overline{y}+\overline{y}.\overline{z}$
d) $\overline{x}.\overline{y}+\overline{y}.z$



Use Boolean algebra to simplify the logic function A + ($\overline{A}$.B)
(a) A.B + $\overline{A}$

10. Simplify the expression $\overline{(\overline{A+C})(B+\overline{D})} = F$

(a) $A\overline{C}+B\overline{D}$

(b) $\overline{A}C+BD$

(c) $AC+\overline{B}D$

(d) $A\overline{C}+\overline{B}D$

$(\overline{\overline{A}}+C)+\overline{B}\,\overline{D}$

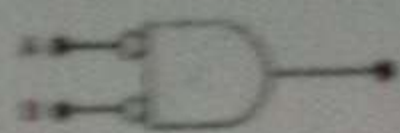


Figure 1

11. Figure 1 is the alternate logic gate representation for a ....

(a) NOR

(b) AND

(c) NOT

(d) NAND

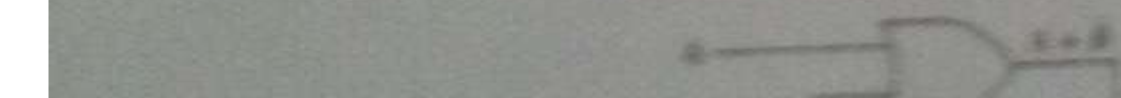
SECTION B THEORY: ANSWER THIS SECTION IN YOUR BOOKLETS

12. For the circuit in figure 2 perform the following:

I. Write down the Boolean expression

II. Simplify the Boolean expression

III. Draw the simplified circuit



4. A standard way of representing the behavior of logic circuits is to use

(a) Boolean algebra

(b) Boolean algebra theorems and axioms

(c) Universal gates

(d) Truth tables

5. The output of an AND gate with three inputs, A, B, and C, is HIGH w

(a) A = 1, B = 1, C = 0

(b) A = 0, B = 0, C = 0

(c) A = 1, B = 1, C = 1

(d) A = 1, B = 0, C = 1

A	B	C
0	0	0
0	0	1

6. If a 3-input NOR gate has eight input possibilities, how many of those will result in a HIGH output?

(a) 1

(b) 2

(c) 7

(d) 8

7. Use Boolean algebra to simplify the logic function $A + (\bar{A} B)$

(a) $A B + \bar{A}$

(b) $A + B$

(c) $\bar{A} + A$

(d) $\bar{A} A$

$A + (\bar{A} B)$

$A + B$

8. Use Boolean algebra to simplify the logic function $A (B + \bar{B} C)$.

(a) $A (B + C)$

(b) $A + \bar{B}$

(c) $A C + B$

(d) $A + B C$

$AB + A\bar{B}C$

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(b) $A + B$

(c) $\bar{A} + A$

(d) $\bar{A}.A$

$A + (\bar{A}\ B)$

$A + B$

8. Use Boolean algebra to simplify the logic function $A.(B + \bar{B}.C)$.

(a) $A.(B + C)$

(b) $A + \bar{B}$

(c) $A.C + B$

(d) $A + B.C$

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5. The output of an AND gate with three inputs, A, B, and C, is HIGH

(a) A = 1, B = 1, C = 0

(b) A = 0, B = 0, C = 0

(c) A = 1, B = 1, C = 1

(d) A = 1, B = 0, C = 1

A	B	C
0	0	0
0	0	

6. If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a HIGH output?

(a) 1

(b) 2

(c) 7

(d) 8

7. Use Boolean algebra to simplify the logic function $X = (\bar{A}.B$

(a) $A.B + \bar{A}$

(b) $A + B$

(c) $\bar{A} + A$

(d) $\bar{A}.A$

$A + (\bar{A}.B)$

$A + B$

8. Use Boolean algebra to simplify the logic function $A.B +$

(a) $A.(B + C)$

(b) $A + \bar{B}$

(c) $A.C + B$

(d) $A + B.C$

(b) A + B
(c) $\bar{A} + A$
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9. Use Boolean algebra to simplify the logic function $A.(B + \bar{B}.C)$.
(a) A.(B + C)
(b) $A + \bar{B}$
(c) A.C + B
(d) A + B.C

10. Simplify the logic function F = (B+A).(B+C).
(a) B+A.C
(b) B.A+B
(c) (A+B).(B.C)
(d) C+A.B

SECTION B [10 MARKS]

ANSWER ALL QUESTIONS FROM THIS SECTION IN YOUR ANSWER BOOKS

11. Draw the Logic circuit that would be used to implement the following Boolean equations

a) P = (AC + BC)(A + C)
b) R = BC + D + AD
c) S = B(A + C) + AC + D

12.

INPUT			OUTPUT
C	B	A	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
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Let us assume that we are designing a simple electronic lock. The lock will open only when certain switches are activated. A 1 at the output will open the lock. There are three

d) In digital system... that the circuitry used to ...

e) None of the above

4. What type of logic gate is this?

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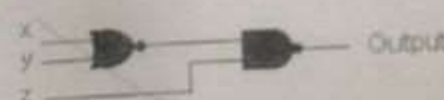

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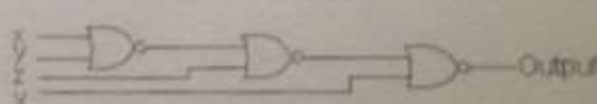


8. Use Boolean algebra to simplify the logic function A + ($\bar{A}$.B)

(a) A.B + $\bar{A}$

valuations for input switches A, B and C that generate a 1 at the output: (A=1, B=
C=0), (A=1, B=0, C=1), (A=0, B=1, C=1),

i. Complete the truth table
ii. Write the Boolean expression
iii. Draw the Logic circuit

A	B	C	outpu
0	0	0	
1	1	0	
1	0	1	
0	1	1	

F. K AMPONG

Appendix A

Single-Variable Theorems

1a. $x \cdot 0 = 0$

1b. $x + 1 = 1$

2a. $x \cdot 1 = x$

valuations for input switches A, B and C that generate a 1 at the output: (A=1, B=
C=0), (A=1, B=0, C=1), (A=0, B=1, C=1),

i. Complete the truth table
ii. Write the Boolean expression
iii. Draw the Logic circuit

A	B	C	outpu
0	0	0	
1	1	0	
1	0	1	
0	1	1	

F. K AMPONG

Appendix A

Single-Variable Theorems

1a. $x \cdot 0 = 0$

1b. $x + 1 = 1$

2a. $x \cdot 1 = x$

...onics II

Index number....6225111...........................

March 2014

TIME: 1 Hr

Answer all questions
Answer section A on the question paper and section B in your answer booklet.
(Find attached: Appendix A - list of Boolean algebra theorems)

Section A [10 Marks]

1. Digital circuits play a very important role in today's electronic systems. They are employed in almost every facet of electronics, excluding,
   a) Control Instrumentation
   b) Communication
   c) Computing
   d) Amplification of weak signals
   e) None of the above

2. A logic gate is:
   a) A special type of amplifier circuit designed to amplifier voltage signals corresponding to binary 1's and 0's.
   b) A special type of amplifier circuit designed to amplifier current signals corresponding to binary 1's and 0's.
   c) A special type of voltage amplifier circuit designed to generate voltage signals corresponding to binary 1's and 0's.
   d) A special type of amplifier circuit designed to accept and generate voltage signals corresponding to binary 1's and 0's.
   e) None of the above

3. Which of the following statements about a logic gate is false?
   a) Gate circuits are most commonly represented in a schematic by their own unique symbols rather than by their constituent transistors and resistors.
   b) Logic circuits provide solution to a problem. They implement functions that are needed to carry out specific tasks
   c) Within the framework of a computer, logic circuits do not provide complete capability for execution of programs and processing of data.

Index number....6225111..............................

March 2014

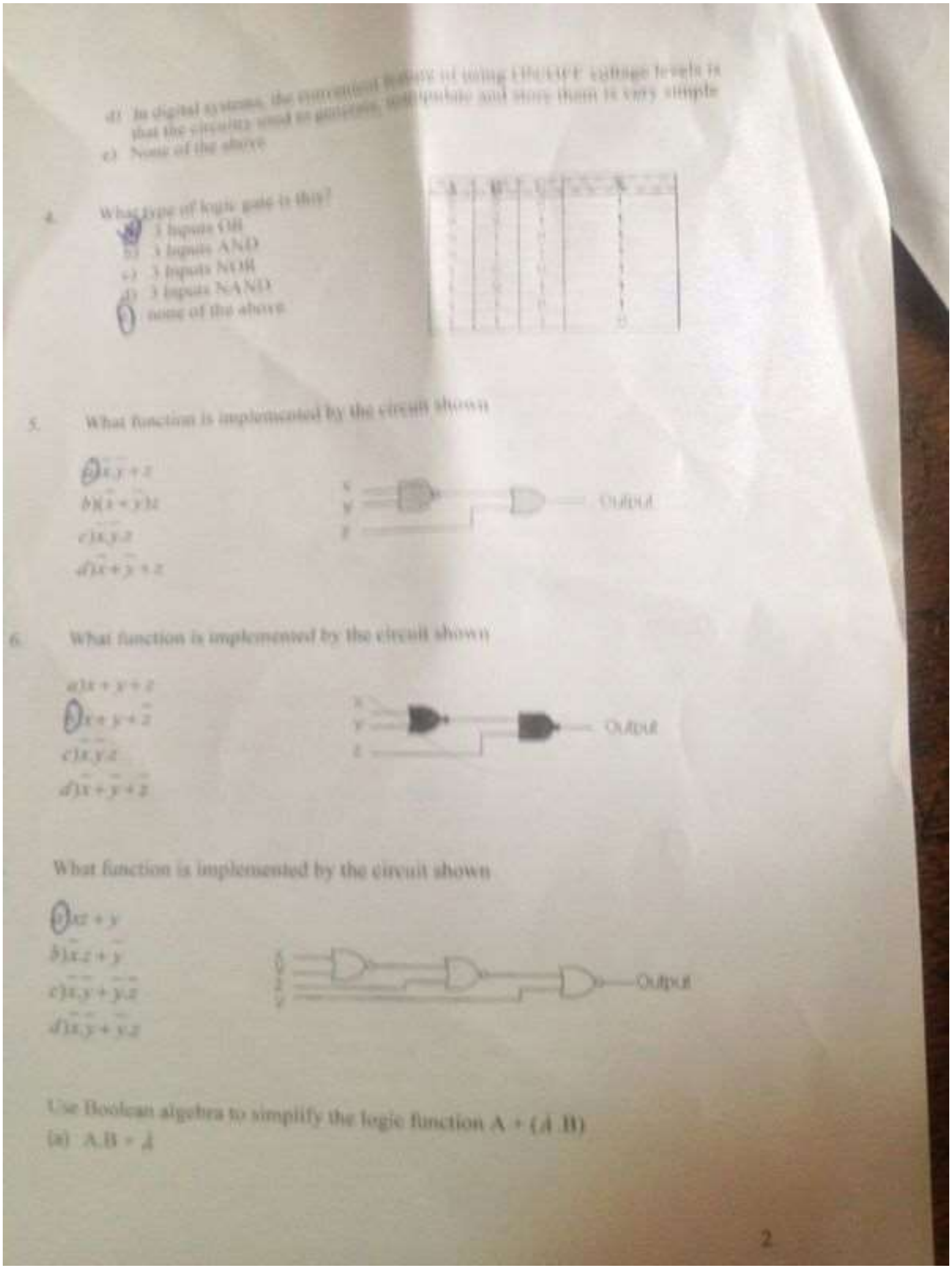
TIME : 1 Hr

Answer all questions
Answer section A on the question paper and section B in your answer booklet.
(Find attached: Appendix A - list of Boolean algebra theorems)
Section A [10 Marks]

1. Digital circuits play a very important role in today's electronic systems. They are employed in almost every facet of electronics, excluding,
   a) Control Instrumentation
   b) Communication
   c) Computing
   d) Amplification of weak signals
   e) None of the above

2. A logic gate is:
   a) A special type of amplifier circuit designed to amplifier voltage signals corresponding to binary 1's and 0's.
   b) A special type of amplifier circuit designed to amplifier current signals corresponding to binary 1's and 0's.
   c) A special type of voltage amplifier circuit designed to generate voltage signals corresponding to binary 1's and 0's.
   d) A special type of amplifier circuit designed to accept and generate voltage signals corresponding to binary 1's and 0's.
   e) None of the above

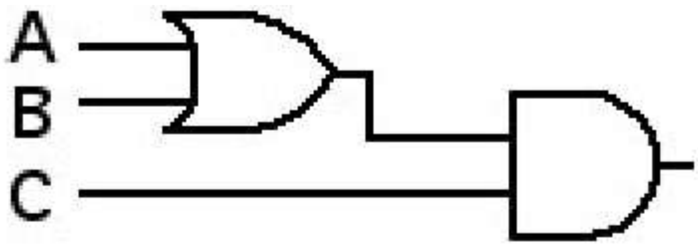
3. Which of the following statements about a logic gate is false?
   a) Gate circuits are most commonly represented in a schematic by their own unique symbols rather than by their constituent transistors and resistors.
   b) Logic circuits provide solution to a problem. They implement functions that are needed to carry out specific tasks
   c) Within the framework of a computer, logic circuits do not provide complete capability for execution of programs and processing of data.

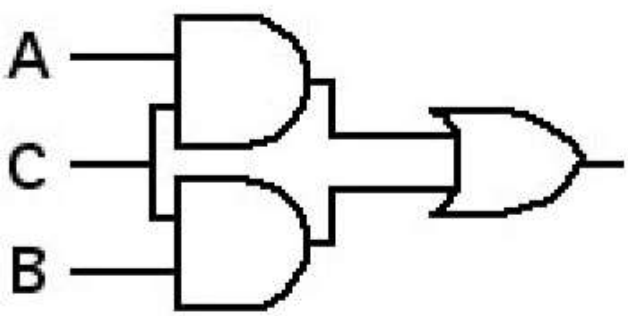


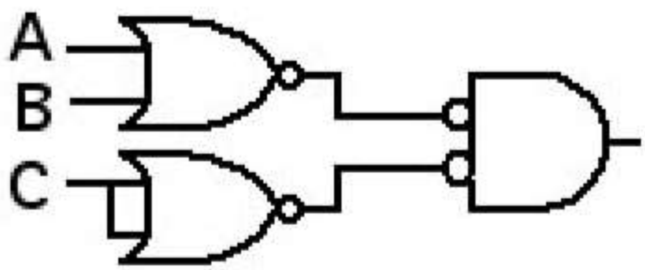
ii) Using Boolean algebra, reduce the logic function described to a simpler form and sketch the resulting circuit.

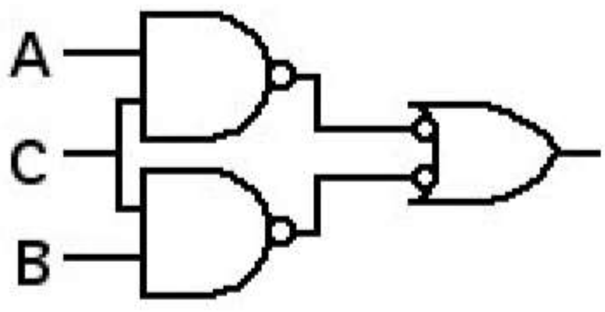
iii) If a burglar named Freshman, who has studied Boolean algebra, wants to rob the Bank by tampering with the sensors to prevent the alarm from going off, what would be the easiest way? Explain your answer.

8. Show that the following four circuits are identical in function.









Single-Variable Theorems

1a. $x \cdot 0 = 0$

1b. $x + 1 = 1$

2a. $x \cdot 1 = x$

2b. $x + 0 = x$

3a. $x \cdot x = x$

3b. $x + x = x$

4a. $x \cdot \bar{x} = x$

4b. $x + \bar{x} = 1$

5. $\bar{\bar{x}} = x$

Two-and Three-Variable Properties

1a. $x \cdot y = y \cdot x$ **Cumulative**

1b. $x + y = y + x$

2a. $x \cdot (y \cdot z) = (x \cdot y) \cdot z$ **Associative**

2b. $x + (y + z) = (x + y) + z$

3a. $x \cdot (y + z) = x \cdot y + x \cdot z$ **Distributive**

3b. $x + y \cdot z = (x + y) \cdot (x + z)$

4a. $x + x \cdot y = x$ **Absorption**

4b. $x \cdot (x + y) = x$

5a. $x \cdot y + x \cdot \bar{y} = x$ **Combining**

5b. $(x + y) \cdot (x + \bar{y}) = x$

6a. $\overline{x \cdot y} = \bar{x} + \bar{y}$ **DeMorgan's Theorem**

6b. $\overline{x + y} = \bar{x} \cdot \bar{y}$

7a. $x + \bar{x} \cdot y = x + y$

7b. $x \cdot (\bar{x} + y) = x \cdot y$

8a. $x \cdot y + y \cdot z + \bar{x} \cdot z = x \cdot y + \bar{x} \cdot z$ **Consensus**

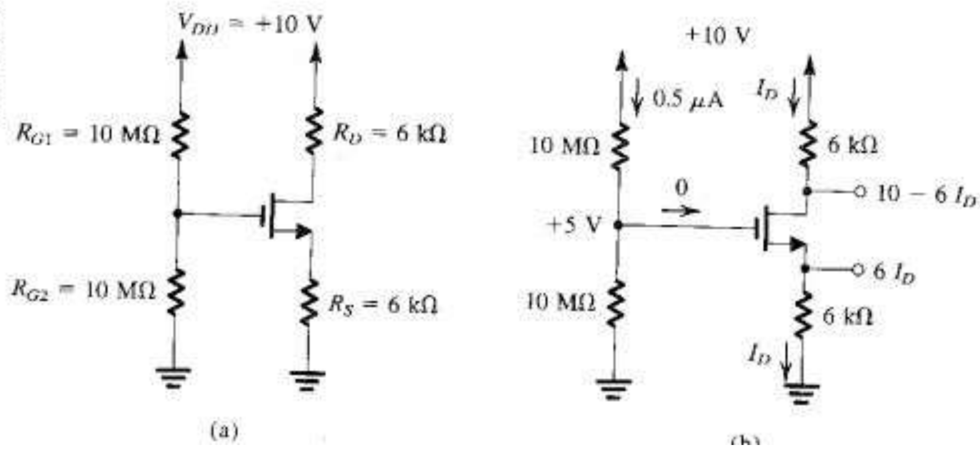
8b. $(x + y) \cdot (y + z) \cdot (\bar{x} + z) = (x + y) \cdot (\bar{x} + z)$

4.13 If in the circuit of Example 4.4 the value of R_D is doubled, find approximate values for I_D and V_D.

Ans. 0.2 mA; 0.05 V

EXAMPLE 4.5

Analyze the circuit shown in Fig. 4.23(a) to determine the voltages at all nodes and the currents through all branches. Let $V_t = 1$ V and $k_n'(W/L) = 1$ mA/V^2. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).



Solution

Since the gate current is zero, the voltage at the gate is simply determined by the voltage divider formed by the two 10-MΩ resistors,

$$V_G = V_{DD}\frac{R_{G2}}{R_{G2}+R_{G1}} = 10\times\frac{10}{10+10} = +5\text{ V}$$

With this positive voltage at the gate, the NMOS transistor will be turned on. We do not know, however, whether the transistor will be operating in the saturation region or in the triode region. We shall assume saturation-region operation, solve the problem, and then check the validity of our assumption. Obviously, if our assumption turns out not to be valid, we will have to solve the problem again for triode-region operation.

Refer to Fig. 4.23(b). Since the voltage at the gate is 5 V and the voltage at the source is $I_D\text{ (mA)}\times 6\text{ (k}\Omega) = 6I_D$, we have

$$V_{GS} = 5-6I_D$$

Thus I_D is given by

$$\begin{aligned} I_D &= \frac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_t)^2 \\ &= \frac{1}{2}\times 1\times(5-6I_D-1)^2 \end{aligned}$$

which results in the following quadratic equation in I_D:

$$18I_D^2-25I_D+8=0$$

This equation yields two values for I_D: 0.89 mA and 0.5 mA. The first value results in a source voltage of $6\times 0.89 = 5.34$, which is greater than the gate voltage and does not make physical sense as it would imply that the NMOS transistor is cut off. Thus,

$$\begin{aligned} I_D &= 0.5\text{ mA} \\ V_S &= 0.5\times 6 = +3\text{ V} \\ V_{GS} &= 5-3 = 2\text{ V} \\ V_D &= 10-6\times 0.5 = +7\text{ V} \end{aligned}$$

Since $V_D > V_G - V_t$, the transistor is operating iu saturation, as initially assumed.

Design the circuit in Fig. 4.21 to obtain a current I_D of 80 μA. Find the value required for R, and find the dc voltage V_D. Let the NMOS transistor have $V_t = 0.6$ V, $\mu_n C_{ox} = 200\ \mu A/V^2$, $L = 0.8\ \mu m$, and $W = 4\ \mu m$. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

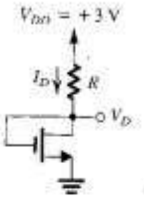


FIGURE 4.21 Circuit for Example 4.3.

Solution

Because $V_{DG} = 0$, $V_D = V_G$ and the FET is operating in the saturation region. Thus,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$
$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

from which we obtain V_{OV} as

$$V_{OV} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}}$$
$$= \sqrt{\frac{2 \times 80}{200 \times (4/0.8)}} = 0.4 \text{ V}$$

Thus,

$$V_{GS} = V_t + V_{OV} = 0.6 + 0.4 = 1 \text{ V}$$

and the drain voltage will be

$$V_D = V_G = +1 \text{ V}$$

The required value for R can be found as follows:

$$R = \frac{V_{DD} - V_D}{I_D}$$
$$= \frac{3 - 1}{0.080} = 25 \text{ k}\Omega$$

EXAMPLE 4.4

Design the circuit in Fig. 4.22 to establish a drain voltage of 0.1 V. What is the effective resistance between drain and source at this operating point? Let $V_t = 1$ V and $k_n'(W/L) = 1$ mA/V^2.

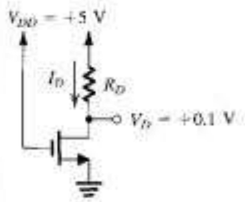


FIGURE 4.22 Circuit for Example 4.4.

Solution

Since the drain voltage is lower than the gate voltage by 4.9 V and $V_t = 1$ V, the MOSFET is operating in the triode region. Thus the current I_D is given by

$$I_D = k_n'\frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$I_D = 1 \times \left[(5-1) \times 0.1 - \frac{1}{2} \times 0.01\right]$$

$$= 0.395 \text{ mA}$$

The required value for R_D can be found as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D}$$

$$= \frac{5 - 0.1}{0.395} = 12.4 \text{ k}\Omega$$

In a practical discrete-circuit design problem one selects the closest standard value a· for, say, 5% resistors—in this case, 12 kΩ; see Appendix G. Since the transistor is oper the triode region with a small V_{DS}, the effective drain-to-source resistance can be deterr follows:

$$r_{DS} = \frac{V_{DS}}{I_D}$$

$$= \frac{0.1}{0.395} = 253\ \Omega$$

Design the circuit of Fig. 4.20 so that the transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. The NMOS transistor has $V_t = 0.7$ V, $\mu_n C_{ox} = 100\ \mu A/V^2$, $L = 1\ \mu m$, and $W = 32\ \mu m$. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).

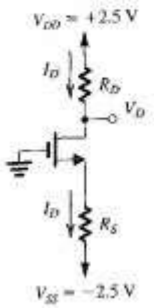


FIGURE 4.20 Circuit for Example 4.2.

Solution

Since $V_D = 0.5$ V is greater than V_G, this means the NMOS transistor is operating in the saturation region, and we use the saturation-region expression of i_D to determine the required value of V_{GS}.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

Substituting $V_{GS} - V_t = V_{OV}$, $I_D = 0.4$ mA $= 400\ \mu$A, $\mu_n C_{ox} = 100\ \mu A/V^2$, and $W/L = 32/1$ gives

$$400 = \frac{1}{2} \times 100 \times \frac{32}{1} V_{OV}^2$$

which results in

$$V_{OV} = 0.5 \text{ V}$$

Thus,

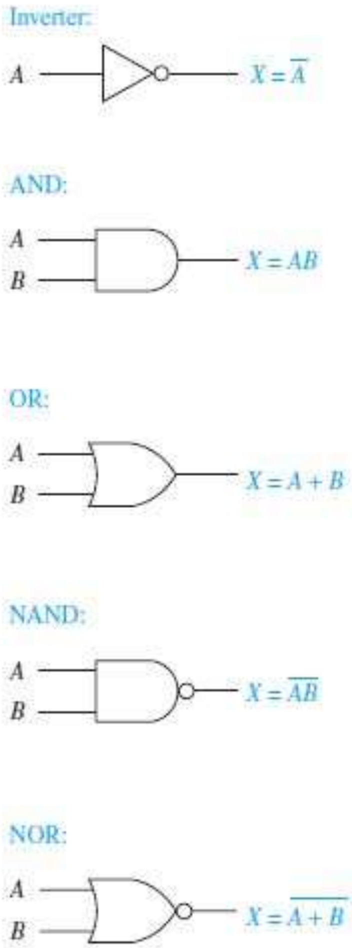
$$V_{GS} = V_t + V_{OV} = 0.7 + 0.5 = 1.2 \text{ V}$$

Referring to Fig. 4.20, we note that the gate is at ground potential. Thus the source must be at -1.2 V, and the required value of R_S can be determined from

$$R_S = \frac{V_S - V_{SS}}{I_D}$$
$$= \frac{-1.2 - (-2.5)}{0.4} = 3.25 \text{ k}\Omega$$

To establish a dc voltage of +0.5 V at the drain, we must select R_D as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D}$$
$$= \frac{2.5 - 0.5}{0.4} = 5 \text{ k}\Omega$$



(a)

A	X
0	1
1	0

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

(b)