ELECTRONICS II

EXERCISE 2

1. In MOSFET the current control mechanism is based on an _____ established by the voltage applied to the control terminal.
   (a) Electric field
   (b) Induction layer
   (c) Induced field
   (d) None of the above

2. In the n-channel depletion-type MOSFET, the threshold voltage is
   (a) The value of the Gate-to-source voltage at which the channel is completely depleted of electrons.
   (b) The value of the Gate-to-source voltage at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel.
   (c) The value of the saturation voltage.
   (d) The inversion layer voltage

3. What is an inversion layer?
   (a) An induced channel
   (b) A depletion layer
   (c) A pn junction
   (d) The gate electrode

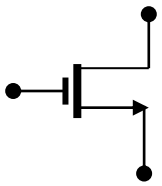
4. For the JFET to operate in the pinch-off
   (a) The drain voltage must be greater than the gate voltage by at least $|V_p|$.
   (b) The source voltage must be greater than the drain voltage by –Vp.
   (c) The gate voltage must be less than the source voltage by –Vp
   (d) None of the above.

5. The conduction of the channel is proportional to
   (a) The pn junction voltage between the source and the drain.
   (b) The excess gate voltage
   (c) The threshold voltage
   (d) The inversion layer voltage

6. The maximum value of the gate-to-source voltage in an n-type JFET is
   (a) –1 V
   (b) +1 V
   (c) 0 V
   (d) 0.7 V

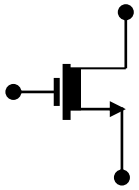
Give the names of the following circuit symbols.

7.



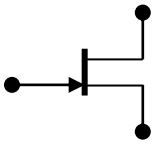
n-channel Enhancement MOSFET

8.



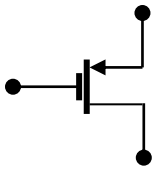
n-channel Depletion MOSFET

9.



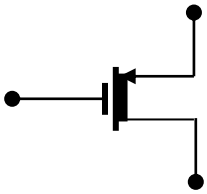
n-channel JFET

10.



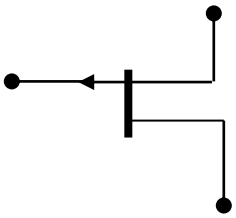
p-channel Enhancement MOSFET

11.



p-channel Depletion type MOSFET

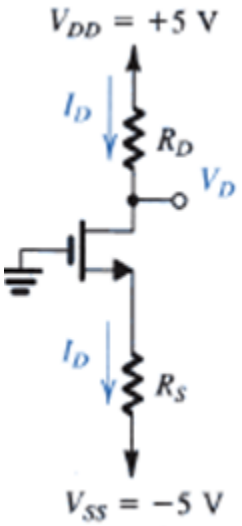
12.



p-channel JFET

Example 1

Design the circuit of fig.1 so that the transistor operates at I_D = 0.4mA and V_D = +1V. The NMOS transistor has Vt. = 2V, $\mu_n C_{ox}$ = 20μA/V^2, L = 10 μm, and W = 400 μm. neglect the channel-length modulation effect (i.e. assume λ = 0).



Example 2

Design the circuit in fig. 2 to obtain a current I_D of 0.4mA. give the value required for R and find the dc voltage V_D. Let the NMOS transistor have Vt. = 2 V, $\mu_n C_{ox}$ = 20 μA/V^2, L = 10 μm, and W = 100 μm. neglect the channel-modulation effect (i.e. assume λ = 0).