# JL7016M Datasheet

## Zhuhai Jieli Technology Co.,LTD

**Version：1.2**

**Date：2022.09.20**

# JL7016M Features

## CPU

- 32bit Dual-Core DSP
- Maximum speed 160MHz
- 32KB ICache and 16KB DCache
- IEEE754 Single precision FPU
- Mathematical accelerate engine
- Interrupts with 8 priority level

## Memory

- On-chip 640KB SRAM
- Support MMU
- Built-In Flash

## Clocks

- On-chip 16 MHz clock oscillator
- On-chip 200 kHz lower-temperature-drift clock oscillator
- 24 MHz crystal oscillator

## DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codec supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Single/Dual MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- Multi-band EQ configuration for voice Effects

## Audio Codec

- Two channels 24-bit DAC,SNR ≥ 104dB
- Two channels 24-bit ADC,SNR ≥ 95dB
- Audio DAC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz/64kHz/88.2kHz/96kHz are supported
- Audio ADC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz are supported
- Support four digital/analog MIC inputs
- Two channels analog audio inputs
- Audio DAC supports differential cap-less mode or single-ended mode
- Direct drive 16ohm/32ohm Speaker loading

## Bluetooth

- Compliant with Bluetooth V5.3+BR+EDR+BLE specification
- Support AoA/AoD direction finding
- Support LE audio BIS/CIS full function
- Meet class2 and class3 transmitting power requirement
- Maximum +9dbm transmitting power
- EDR receiver with -95dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap\gatt\rfcomm\sdp\l2cap profile
- bap 1.0\pacs 1.0\ccp 1.0\mcp 1.0\micp 1.0\vcp 1.0\csip 1.0
- a2dp 1.3.2\avctp 1.4\avdtp 1.3\ avrcp 1.6.2\hfp 1.8 \spp 1.2\rfcomm 1.1\pnp 1.3\hid 1.1.1\sdp core5.3\l2cap core 5.3

## Peripherals

- One full speed USB OTG controller
- One SD host controller for eMMC/SD
- Six multi-function 32-bit timers, support capture and PWM mode
- Four UART interface, UART0,UART1&UART2 support DMA
- I2C Master/Slave interface
- SPI Master/Slave interface
- I2S Master/Slave interface
- QDEC
- Low power CapSense
- 13-channel 10-bit ADC for analog sampling
- 4-channel Motor PWM controller

- 16 Individually programmable and multiplexed GPIO pins
- Up to 12 external interrupt/wake-up source(low power available,can be multiplexed to any I/O)

**PMU**

- Built-in lithium battery charging manager,up to 200mA charging current
- Built-in LDO and Buck DC-DC converter
- Less than 2uA sleep current
- VPWR range : 4.5V to 5.5V
- VBAT range : 2.2V to 4.5V
- IOVDD range : 2.2V to 3.6V

**Packages**

- QFN32(4mm*4mm)

**Temperature**

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

**Applications**

- Wireless microphone
- Bluetooth Stereo Headsets and Headphones
- Bluetooth TWS Earphones

# 1 Block Diagram

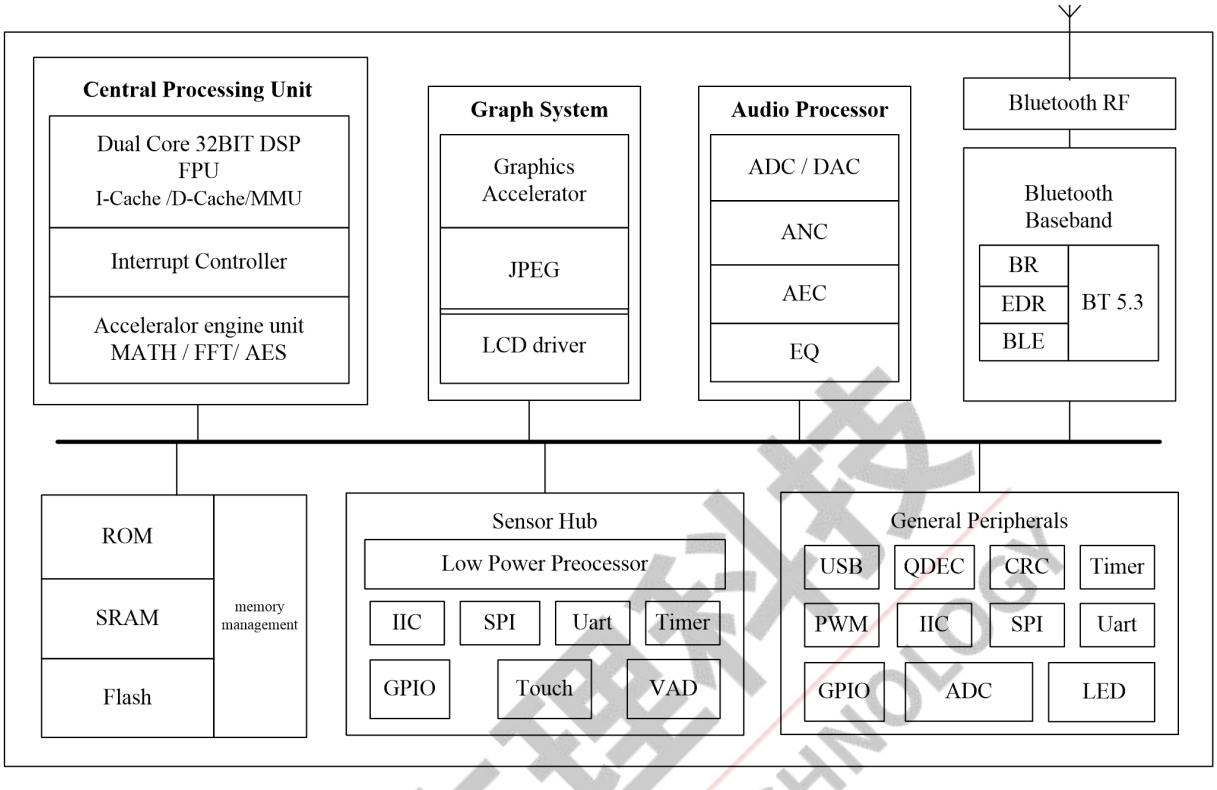



**Figure 1-1 JL7016M Block Diagram**

# 2 Pin Definition

## 2.1 Pin Assignment

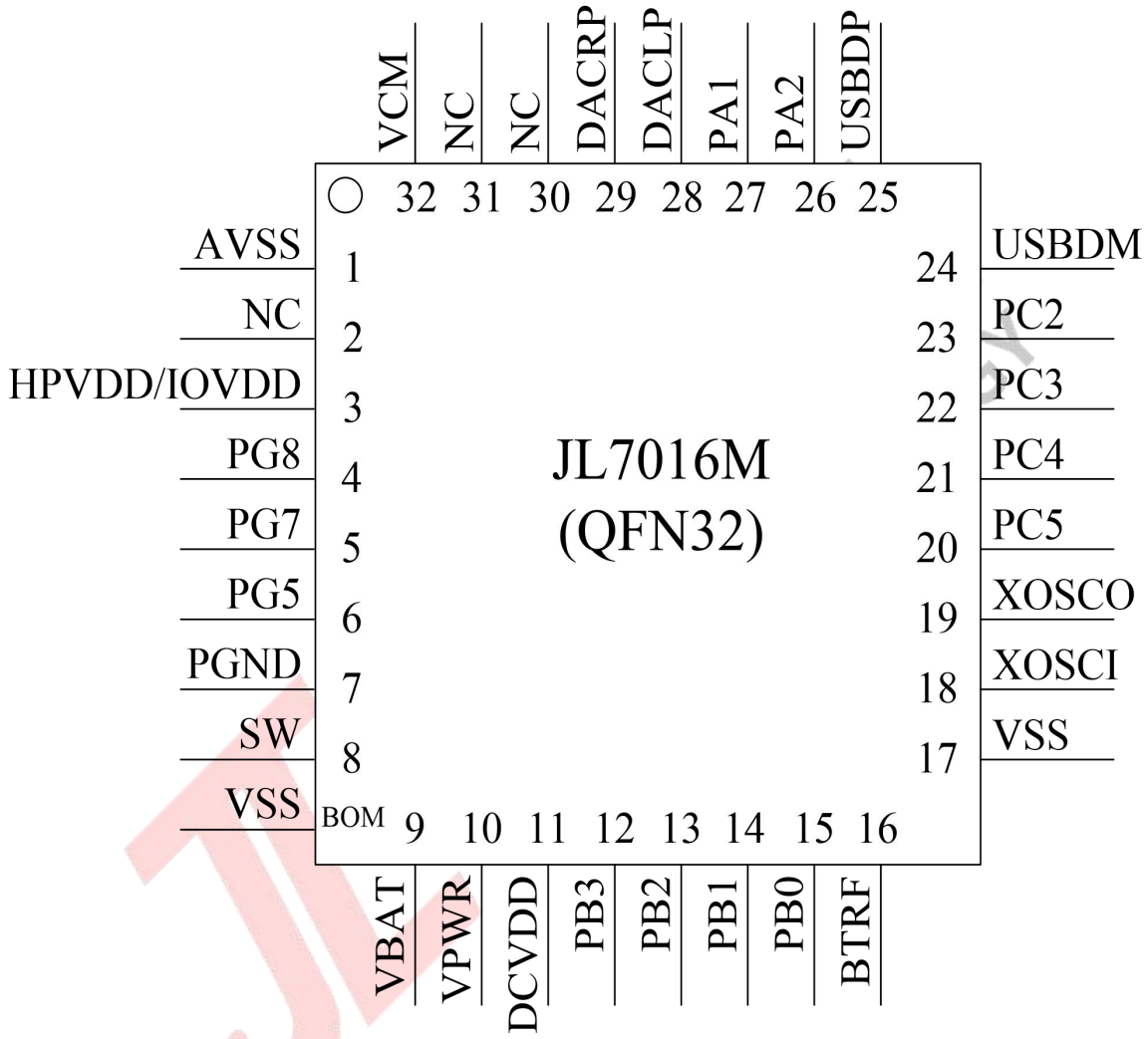



**Figure 2-1 JL7016M Package Diagram**

## 2.2 Pin Description

**Table 2-1 JL7016M Pin Description**

| PIN NO. | Name | Type | Function | Other Function |
|---|---|---|---|---|
| 1 | AVSS | G | | Audio analog ground; |
| 2 | NC | | | |
| 3 | HPVDD | PI | | Audio power; |
| | IOVDD | PO | | Built-in linear voltage regulator output; |
| 4 | PG8 | I/O | GPIO | MICIN2: MIC2 Input Channel 2;<br>MIC2_P: Different MIC2 Positive;<br>AMUX_C0:Analog Channel C0 input; |
| 5 | PG7 | I/O | GPIO | MIC_BIAS2: MIC2 Bias Output(Built-in resistor);<br>MIC2_N: Different MIC2 Negative;<br>AMUX_C1: Analog Channel C1 input;<br>ADC15: ADC Input Channel 15; |
| 6 | PG5 | I/O | GPIO | MIC_BIAS3: MIC3 Bias Output(Built-in resistor);<br>MIC3_N: Different MIC3 Negative;<br>AMUX_D1:Analog Channel D1 input;<br>ADC14: ADC Input Channel 14;<br>TMR3CK: PWM Timer3 CLK In; |
| 7 | PGND | G | | The ground of Buck DC-DC converter; |
| 8 | SW | PO | | Switch signal of the Buck converter, connected to inductor; |
| 9 | VBAT | P | | Battery interface; |
| 10 | VPWR<br>(PP0) | PI<br>(I/O) | GPIO<br>(High Voltage Input) | Charging Power Input;<br>High Voltage Resistance I/O;<br>UART0TXB: Uart0 Data Out(B);<br>UART0RXB: Uart0 Data In(B);<br>PWM3: Timer3 PWM Output;<br>CAP1: Timer1 Capture; |
| 11 | DCVDD | P | | Internal Power; |
| 12 | PB3 | I/O | GPIO<br>(High Voltage Input) | SPI4DOA: SPI4 Data Out(A);<br>Q-decoder0_1: Quadrature decoder0_1;<br>UART3RXA: Uart3 Data In(A); |
| 13 | PB2 | I/O | GPIO<br>(High Voltage Input) | LP_Touch2: Low Power Touch Channel 2;<br>SPI4CLKA: SPI4 Clock(A);<br>Q-decoder0_0: Quadrature decoder0_0;<br>ADC7: ADC Input Channel 7;<br>UART3TXA: Uart3 Data Out(A);<br>CAP5: Timer5 Capture; |

| | | | | |
|---|---|---|---|---|
| 14 | PB1 | I/O | GPIO<br>(High Voltage Input) | Hold down 0 to reset;<br>LP_Touch1: Low Power Touch Channel 1;<br>ADC6: ADC Input Channel 6; |
| 15 | PB0 | I/O | GPIO<br>(High Voltage Input) | LP_Touch0: Low Power Touch Channel 0;<br>TMR4: Timer4 Clock Input; |
| 16 | BTRF | RFI | | Bluetooth RF antenna interface; |
| 17 | VSS | G | | System Ground |
| 18 | XOSCI | I | | System Crystal Oscillator Input; |
| 19 | XOSCO | O | | System Crystal Oscillator Output; |
| 20 | PC5 | I/O | GPIO | SPI0_DAT2C: SPI0 Data2(C);<br>SD0_CLKA: SD0 Clock(A);<br>SPI1DOB: SPI1 Data Out(B);<br>IIC0_SDA_B: IIC0 SDA(B);<br>ALNK_DAT3(B): Audio Link Data3(B);<br>ADC5: ADC Input Channel 5;<br>UART2RXA: Uart2 Data In(A); |
| 21 | PC4 | I/O | GPIO | SPI0_DIC: SPI0 Data In(C);<br>SD0CMDA: SD0 CMD(A);<br>SPI1CLKB: SPI1 Clock(B);<br>IIC0_SCL_B: IIC0 SCL(B);<br>ALNK_DAT2B: Audio Link Data2(B);<br>ADC4: ADC Input Channel 4;<br>UART2TXA: Uart2 Data Out(A);<br>PWM4: Timer4 PWM Output; |
| 22 | PC3 | I/O | GPIO | SPI0_CSC: SPI0 Chip Select(C);<br>SD0DATOA: SD0 Data Out(A);<br>SPI1DIB: SPI1 Data In(B);<br>ALNK_LRCKB: Audio Link Word Select(B);<br>TMR3: Timer3 Clock Input; |
| 23 | PC2 | I/O | GPIO | SPI0_DOC: SPI0 Data Out(C);<br>ALNK_SCLKB: Audio Link Serial Clock(B);<br>TMR1: Timer1 Clock Input; |
| 24 | USBDM | I/O | USB Negative Data<br>(pull down) | SDTAP_DATB: SDTAP Data(B);<br>SPI2DOB: SPI2 Data Out(B);<br>IIC0_SDA_A: IIC0 SDA(A);<br>ADC11: ADC Input Channel 11;<br>UART1RXB: Uart1 Data In(B); |
| 25 | USBDP | I/O | USB Positive Data<br>(pull down) | SDTAP_CLKB: SDTAP CLK(B);<br>SPI2CLKB: SPI2 Clock(B);<br>IIC0_SCL_A: IIC0 SCL(A);<br>ADC10: ADC Input Channel 10;<br>UART1TXB: Uart1 Data Out(B); |

| | | | | |
|---|---|---|---|---|
| 26 | PA2 | I/O | GPIO | MIC_BIAS0: MIC0 Bias Output(Built-in resistor);<br>MIC0_N: Different MIC0 Negative;<br>AMUX_A1:Analog Channel A1 input;<br>CLKOUT1: Clock Out1;<br>SPI1CLKA: SPI1 Clock(A);<br>ALNK_MCLKA: ALNK Master Clock(A);<br>UART1RXA: Uart1 Data In(A);<br>CAP3: Timer3 Capture; |
| 27 | PA1 | I/O | GPIO | MICIN0: MIC0 Input Channel 0;<br>MIC0_P: Different MIC0 Positive;<br>AMUX_A0:Analog Channel A0 input;<br>SPI1DIA: SPI1 Data In(A);<br>UART1TXA: Uart1 Data Out(A);<br>PWM0: Timer0 PWM Output; |
| 28 | DACLP | AO | | Left channel audio output positive; |
| 29 | DACRP | AO | | Right channel audio output positive; |
| 30 | NC | P | | |
| 31 | NC | P | | |
| 32 | VCM | P | | Audio analog reference bias; |
| PAD | VSS | G | | System Ground; |

| **Pin Type** | **Description** | **Pin Type** | **Description** |
|---|---|---|---|
| P | Power | I/O | Input or Output |
| PO | Power Output | I | Input |
| PI | Power Input | O | Output |
| G | Ground | RFI | Radio frequency interface |
| AO | Analog Output | | |

# 3 Electrical Characteristics

## 3.1 Absolute Maximum Ratings

**Table 3-1**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| Topt | Operating temperature | -40 | +85 | ℃ |
| Tstg | Storage temperature | -65 | +150 | ℃ |
| VBAT | Supply Voltage | -0.3 | 4.5 | V |
| VPWR | Charger Voltage | -0.3 | 6 | V |
| $V_{IOVDD}$ | Voltage applied at IOVDD | -0.3 | 3.6 | V |
| $V_{GPIO}$ | Voltage applied to GPIO | -0.3 | IOVDD+0.3 | V |
| $V_{HVIO}$ | Voltage applied to High Voltage Resistant IO | -0.3 | +5.5 | V |
| $V_{HPVDD}$ | Voltage applied at HPVDD | -0.3 | +3 | V |

**Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below**

## 3.2 PMU Characteristics

**Table 3-2**

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| VBAT | Voltage Input | 2.2 | 3.7 | 4.4 | V | |
| VPWR | Charger supply Voltage | 4.5 | 5.0 | 5.5 | V | |
| Operating mode | | | | | | |
| IOVDD | Voltage output | _ | 3.0 | _ | V | VBAT = 4.2V, 10mA loading |
| | Loading current | _ | _ | 200 | mA | IOVDD=3.2V@VBAT = 3.5V |
| DCVDD | Voltage output | _ | 1.25 | _ | V | IOVDD=3.0V, 10mA loading |
| | Loading current | _ | _ | 100 | mA | DCVDD=1.25V@IOVDD=3.0v on LDO mode |
| | | _ | _ | 180 | mA | DCVDD=1.25V@VBAT=3.0v on DCDC mode |
| EVDD | Voltage output | _ | 1.1 | _ | V | DCVDD=1.25V, 1mA loading |
| | Loading current | _ | _ | 5 | mA | EVDD=1.1V@DCVDD=1.25v |
| Low Power mode | | | | | | |
| IOVDD | Loading current | _ | _ | 10 | mA | IOVDD=3V@VBAT = 4.2V |

## 3.3 Battery Charge

**Table 3-3**

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| VPWR | Charge Input Voltage | 4.5 | 5 | 5.5 | V | _ |
| $V_{bat\ float}$ | Charge Voltage | 4.15 | 4.2 | 4.25 | V | VPWR＞4.5V |
| | | 4.30 | 4.35 | 4.40 | V | VPWR＞4.65V |
| $I_{bat}$ | Charge Current | 15 | _ | 200 | mA | Charge current at fast charge mode VBAT=4.0V@VPWR=5.0V |
| $I_{end}$ | End Of Charge Current | 2 | _ | 30 | mA | End of charge current |
| $V_{Trikl}$ | Trickle Charge Voltage | _ | 3.0 | _ | V | VPWR＞4.5V |

## 3.4 IO Input/Output Electrical Logical Characteristics

**Table 3-4**

| **GPIO input characteristics** | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
| $V_{IL}$ | Low-Level Input Voltage | -0.3 | _ | 0.3* IOVDD | V | IOVDD = 3.0V |
| $V_{IH}$ | High-Level Input Voltage | 0.7* IOVDD | _ | IOVDD+0.3 | V | IOVDD = 3.0V |
| **High Voltage Resistant IO input characteristics** | | | | | | |
| **Symbol** | **Parameter** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
| $V_{IL}$ | Low-Level Input Voltage | -0.3 | _ | 0.3* IOVDD | V | IOVDD = 3.0V |
| $V_{IH}$ | High-Level Input Voltage | 0.7* IOVDD | _ | +5V | V | IOVDD = 3.0V |
| **GPIO & High Voltage Resistant IO output characteristics** | | | | | | |
| **Symbol** | **Parameter** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
| $V_{OL}$ | Low-Level Output Voltage | _ | _ | 0.1* IOVDD | V | IOVDD = 3.0V |
| $V_{OH}$ | High-Level Output Voltage | 0.9* IOVDD | _ | _ | V | IOVDD = 3.0V |

## 3.5 Internal Resistor Characteristics

**Table 3-5**

| Port | Drive(mA) | | Internal Pull-Up Resistor | Internal Pull-Down Resistor | Comment |
|---|---|---|---|---|---|
| PA1, PA2<br>PC2~PC5<br>PG5~PG8 | HD,HD0==0,0 | 2.4 | 10K | 10K | 1、PB1 default pull up<br>2、USBDM & USBDP default pull Down<br>3、internal pull-up / pull-down resistance \| accuracy ±20% |
| | HD,HD0==0,1 | 8 | | | |
| | HD,HD0==1,0 | 26 | | | |
| | HD,HD0==1,1 | 46 | | | |
| PP0<br>PB0~PB3 | 8<br>(High Voltage Resistant) | | 10K | 10K | |
| USBDP | 4 | | 1.5K | 15K | |
| USBDM | | | 180K | 15K | |

## 3.6 Audio DAC Characteristics

**Table 3-6**

| Parameter | MODE | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Frequency Response | | 20 | _ | 20k | Hz | 1KHz/0dB<br>32 ohm loading<br>With A-Weighted Filter |
| Output Swing | Differential | | 1.0 | | Vrms | |
| | Single-ended | _ | 0.5 | _ | Vrms | |
| THD+N | Differential | _ | -70 | _ | dB | |
| | Single-ended | _ | -67 | _ | dB | |
| S/N | Differential | _ | 104 | _ | dB | |
| | Single-ended | _ | 98 | _ | dB | |
| Dynamic Range | Differential | _ | 104 | _ | dB | 1KHz/-60dB<br>32 ohm loading<br>With A-Weighted Filter |
| | Single-ended | _ | 98 | _ | dB | |
| Noise Floor | Differential | | 5.7 | | uVrms | A-Weighted Filter |
| | Single-ended | _ | 5.8 | _ | uVrms | |
| DAC Output Power | Differential | | 30 | | mW | 32ohm loading |
| | Single-ended | | 16 | | mW | |

## 3.7 Audio ADC Characteristics

**Table 3-7**

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| Dynamic Range | | 94 | | dB | Fsample=44.1kHz,Gain=0dB<br>Fin=1KHz 590mVrms |
| SNR | _ | 95 | _ | dB | Fsample=44.1kHz,Gain=0dB<br>Fin=1KHz 590mVrms |
| THD+N | _ | -75 | _ | dB | |
| SNR | _ | 76 | _ | dB | Fsample=44.1kHz,Gain=18dB<br>Fin=1KHz 75mVrms |
| THD+N | _ | -73 | _ | dB | |

## 3.8 BT Characteristics

### 3.8.1 Transmitter

**Basic Rate** Table 3-8

| Parameter | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RF Transmit Power | | | 7 | 9 | dBm | 25℃, Power Supply VBAT=3.7V 2441MHz |
| RF Power Control Range | | | 18 | | dB | |
| 20dB Bandwidth | | | 950 | | KHz | |
| In-band spurious Emissions （BQB Test Mode RF_Tx Power=5dBm） | $F=F_0\pm1MHz$ | | -20 | | dBm | |
| | $F=F_0\pm2MHz$ | | -51 | | dBm | |
| | $F=F_0\pm3MHz$ | | -55 | | dBm | |
| | $F=F_0$+/->3MHz | | -55 | | dBm | |

**Enhanced Data Rate** Table 3-9

| Parameter | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Relative Power | | | -2 | | dB | 25℃, Power Supply VBAT=3.7V 2441MHz |
| π/4 DQPSK Modulation Accuracy | DEVM RMS | | 9 | | % | |
| | DEVM 99% | | 23 | | % | |
| | DEVM Peak | | 18 | | % | |
| In-band spurious Emissions （BQB Test Mode RF_Tx Power=5dBm） | $F=F_0\pm1MHz$ | | -4 | | dBm | |
| | $F=F_0\pm2MHz$ | | -34 | | dBm | |
| | $F=F_0\pm3MHz$ | | -43 | | dBm | |
| | $F=F_0$+/->3MHz | | -48 | | dBm | |

### 3.8.2 Receiver

**Basic Data Rate** Table 3-10

| Parameter | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Sensitivity | | | -92 | | dBm | 25℃, Power Supply VBAT=3.7V 2441MHz DH5 |
| Co-channel Interference Rejection | | | 10 | | dB | |
| Adjacent channel selectivity C/I | +1MHz | | -4 | | dB | |
| | -1MHz | | -3 | | dB | |
| | +2MHz | | -39 | | dB | |
| | -2MHz | | -33 | | dB | |
| | +3MHz | | -45 | | dB | |
| | -3MHz | | -28 | | dB | |

**Enhanced Data Rate** **Table 3-11**

| Parameter | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Sensitivity | | -95 | -94 | | dBm | 25℃, Power Supply VBAT=3.7V 2441MHz 2DH5 |
| Co-channel Interference Rejection | | | 10 | | dB | |
| Adjacent channel selectivity C/I | +1MHz | | -8 | | dB | |
| | -1MHz | | -8 | | dB | |
| | +2MHz | | -40 | | dB | |
| | -2MHz | | -33 | | dB | |
| | +3MHz | | -45 | | dB | |
| | -3MHz | | -27 | | dB | |

### 3.8.3 BLE

**1M Data Rate** **Table 3-12**

| Parameter | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Sensitivity | | | -96 | | dBm | 25℃ Power Supply VBAT=3.7V 2440MHz |
| RF Transmit Power | | | 7 | | dBm | |
| In-band Spurious Emission | \|M-N\|=2MHz | | -37 | | dBm | |
| | \|M-N\|≥3MHz | | | -34 | dBm | |
| Modulation Characteristics | Δf1 avg | | 250 | | KHz | |
| | Δf2 99% | | 211 | | KHz | |
| | Δf1avg/Δf2avg | | 0.9 | | | |
| Carrier Frequency Offset | | -15 | | +15 | KHz | |
| Frequency Drift | | -25 | | +25 | KHz | |
| Frequency Drift Rate | | -5 | | +5 | KHz/50us | |

**2M Data Rate** **Table 3-13**

| Parameter | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Sensitivity | | | -94 | | dBm | 25℃ Power Supply VBAT=3.7V 2440MHz |
| RF Transmit Power | | | 7 | | dBm | |
| In-band Spurious Emission | \|M-N\|=4MHz | | -44 | | dBm | |
| | \|M-N\|=5MHz | | -43 | | dBm | |
| | \|M-N\|≥6MHz | | | -48 | dBm | |
| Modulation Characteristics | Δf1 avg | | 500 | | KHz | |
| | Δf2 99% | | 428 | | KHz | |
| | Δf1avg/Δf2avg | | 0.9 | | | |
| Carrier Frequency Offset | | -20 | | +20 | KHz | |

| | | | | | |
|---|---|---|---|---|---|
| Frequency Drift | -25 | | +25 | KHz | |
| Frequency Drift Rate | -5 | | +5 | KHz/50us | |

**Long Range** **Table 3-14**

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| Sensitivity LE 125K(S8) | | -104 | | dBm | VBAT=3.7V,25℃ 2440MHz |
| Sensitivity LE 500K(S2) | | -100 | | dBm | |

## 3.9 ESD Protectio

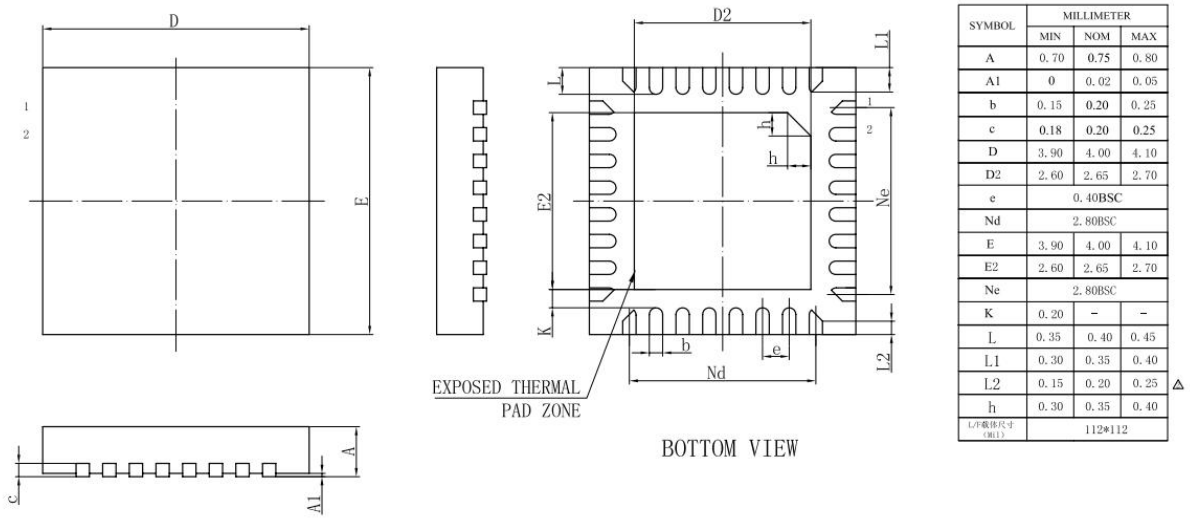
**Table 3-15**

| Parameter | Typ. | Test pin | Reference standard |
|---|---|---|---|
| Human Body Mode | ±4KV | All pins | JEDEC EIA/JESD22-A114 |
| Machine Mode | ±200V | All pins | JEDEC EIA/JESD22-A115 |
| Charge Device Model | ±1KV | All pins | JEDEC EIA/JESD22-C101F |
| Latch up | ±200mA | All GPIO pins | JEDEC STANDARD NO.78E |
| | 1.5xVopmax | All power pins | |

**Note : 1.5xVopmax = 1.5 times maximum operating voltage.**

# 4 Package Information

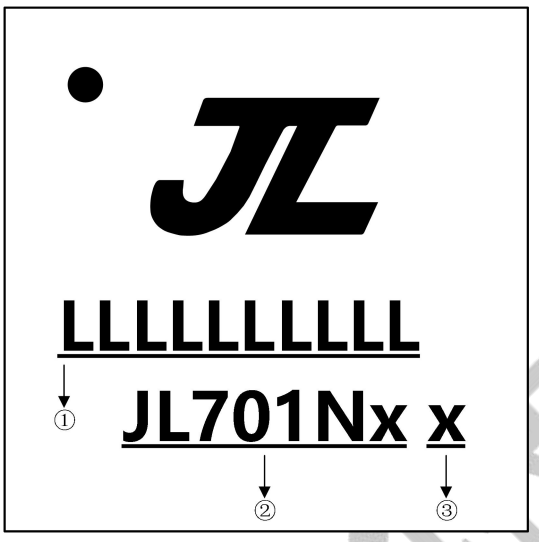
## 4.1 QFN32_4.0x4.0




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.18 | 0.20 | 0.25 |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.60 | 2.65 | 2.70 |
| e | 0.40BSC | | |
| Nd | 2.80BSC | | |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.60 | 2.65 | 2.70 |
| Ne | 2.80BSC | | |
| K | 0.20 | – | – |
| L | 0.35 | 0.40 | 0.45 |
| L1 | 0.30 | 0.35 | 0.40 |
| L2 | 0.15 | 0.20 | 0.25 |
| h | 0.30 | 0.35 | 0.40 |
| 载体尺寸 | 112*112 | | |

**Figure 4-1 JL7016M Package**

# 5 IC Marking Information




① LLLLLLLLLL：Production Batch

② JL701Nx：Chip Model

③ x：Built-in flash size

0: No Flash Memory

2: 2Mbit Flash

4: 4Mbit Flash

8: 8Mbit Flash

6: 16Mbit Flash

3: 32Mbit Flash

# 6 Solder-Reflow Condition

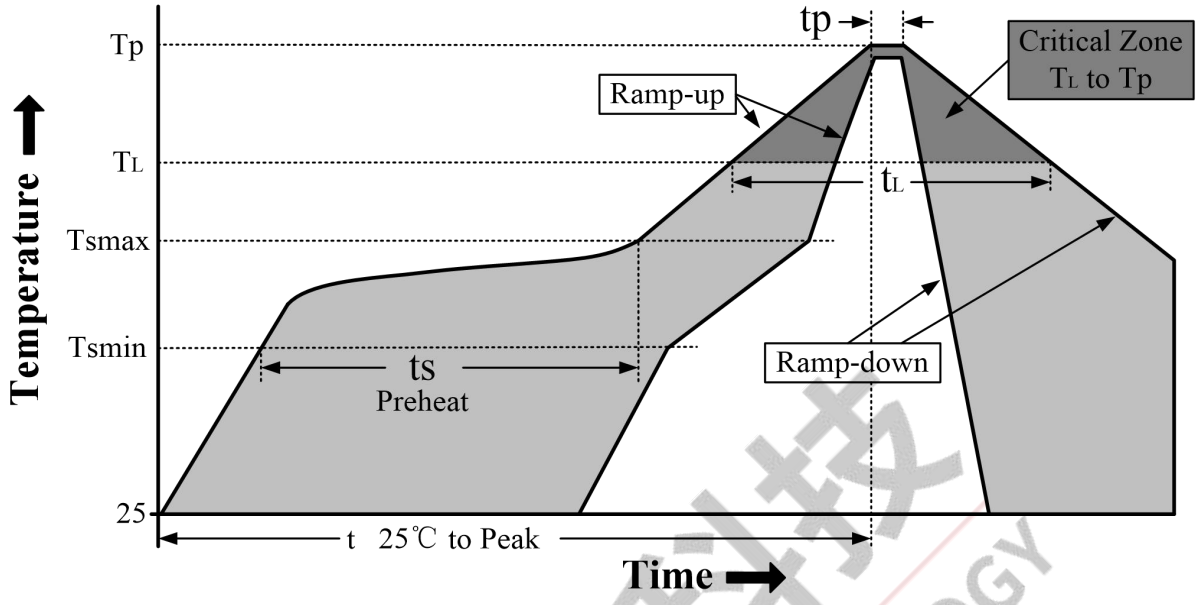



**Figure 6-1 Classification Reflow Profile**

**Classification Profiles** **Table 6-1**

| Profile Feature | | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|---|---|---|
| Preheat/ Soak | Temperature Min ($T_{smin}$) | 100℃ | 150℃ |
| | Temperature Max ($T_{smax}$) | 150℃ | 200℃ |
| | Time (ts) from ($T_{smin}$ to $T_{smax}$) | 60-120 seconds | 60-180 seconds |
| Average ramp-up rate ($T_{smax}$ to $T_p$) | | 3℃/second max | 3℃/second max |
| Liquidous temperature ($T_L$)<br>Time ($t_L$) maintained above $T_L$ | | 183℃<br>60-150 seconds | 217℃<br>60-150 seconds |
| Peak package body temperature ($T_p$) | | See Table 6-2 | See Table 6-3 |
| Time within 5℃ of actual Peak Temperature (tp)[2] | | 10-30 seconds | 20-40 seconds |
| Ramp-down rate ($T_p$ to $T_L$) | | 6℃/second max | 6℃/second max |
| Time 25℃ to peak temperature | | 6 minutes max | 8 minutes max |

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5℃ of actual peak temperature (tp) specified for the reflow profiles is a "supplier" minimum and "user" maximum.

**SnPb - Classification Temperature** **Table 6-2**

| Package Thickness | Volume mm³ < 350 | Volume mm³ ⩾ 350 |
|---|---|---|
| <2.5 mm | 240 +0/-5℃ | 225 +0/-5℃ |
| ⩾2.5 mm | 225 +0/-5℃ | 225 +0/-5℃ |

**Pb-free - Classification Temperature** **Table 6-3**

| Package Thickness | Volume $mm^3$ < 350 | Volume $mm^3$ 350 - 2000 | Volume $mm^3$ > 2000 |
|---|---|---|---|
| < 1.6mm | 260℃ | 260℃ | 260℃ |
| 1.6 mm - 2.5mm | 260℃ | 250℃ | 245℃ |
| > 2.5mm | 250℃ | 245℃ | 245℃ |

# 7 Storage Condition

## 7.1 Moisture Sensitivity Level

JL7016M is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-033.

## 7.2 Storage Alert

1. Calculated shelf life in sealed bag 12 months at＜40°C and 90% relative humidity (RH).
2. Peak package body temperature≤260°C.
3. After bag is opened,devices that will be subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions≤30°C/60%RH or stored per J-STD-033.
4. Devices require bake before mounting if humidity indicator card reads ＞ 10% for level 2a-5a devices or＞60% for level 2 devices when read at 23±5°C,or 3a or 3b are not met.
5. Please refer to IPC/JEDEC J-STD-033 for baking procedure if necessary.

# 8 Revision History

| Date | Revision | Description |
|---|---|---|
| 2022.06.08 | V1.0 | Initial Release |
| 2022.07.20 | V1.1 | Update BT Characteristics |
| 2022.09.20 | V1.2 | Add Storage Condition，Update IC Marking Information |