AD157A0 Datasheet

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AD157A0 Features

CPU Core

- 32-bit CPU,Built-in ICACH, can be connected to Flash for expansion of code
- The main frequency is up to 120MHz

Memory

- Built-in 20Kbytes of SRAM
- 8Kbytes 2-Way Icache

Clock Source

- RC Clock frequency about 16MHz
- LRC(low power RC) clock frequency about 200KHz

Digital I/O

- Up to 24 programmable digital I/O pins
- General the IO supports pull-up(10k),pull-down(60k), strong,weak output,input and high impedance
- Up to 12 external interrupt/wake-up source(low power available,can be multiplexed to any I/O, with hardware filter)
- Input channel and Output channel, provide arbitrary IO input and output options for some modules

Digital peripherals

- Two UART Controllers(UART0/1) supports DMA and Flow Control
- Two SPI Controllers with DMA(SPI0/1)

support master mode and slave mode

- One Spi Flash Controller to run code
- One SD host controller
- Three 32-bit Asynchronous Divider Timers
- One IIC Controller
- Four channel PWM output
- Infrared remote control decoder
- Watchdog
- 64-bit EFUSE

Analog Peripherals

- 0.5 watt Class-D audio amplifier output
- 10-bit high precision ADC
- Low voltage protection
- Power on reset

Operating Conditions

- Working voltage
  VBAT: 2.0v - 5.5v
  VDDIO: 2.0v - 3.4v
- Soft-off current is 2uA
- Operating Temperature: -40°C to +85°C

Package

- QSOP28

Application

- Sound Toy
- Audio player
- Universal Microcontroller

1、Pin Definition

1.1   Pin Assignment

PB10	1		28	DACN/PB11
PB9	2		27	DACP
PB8	3		26	VSS
PB6	4		25	VBAT
PB5	5		24	VDDIO
PB4	6	AD157A0	23	PA0
PB2	7	QSOP28	22	PA1
PB1	8		21	PA2
PB0	9		20	PA3
PA15	10		19	PA6
PA14	11		18	PA7
PA13	12		17	PD0
PA12	13		16	PD1
PA11	14		15	PD2

Figure 1-1   AD157A0_QSOP28 Package Diagram

1.2 Pin Description

Table 1-1 AD157A0_QSOP28 Pin Description

PIN NO.	Name	Type	Drive (mA)	Function	Description
1	PB10	I/O	8	GPIO (pull up) (High Voltage Resistance)	MCLR(0 effective);
2	PB9	I/O	8	GPIO (High Voltage Resistance)	SPI1DOD:SPI1 Data Out(D); UART1TRXB:Uart1 Data In/Out(B); I2C_SDA(D); CAP1:Timer1 Capture;
3	PB8	I/O	8	GPIO (High Voltage Resistance)	SPI1CLKD:SPI1 Clock(D); I2C_SCL(D); OSCIA:Crystal Oscillator Input(A);
4	PB6	I/O	8/64	GPIO	SD0DATC:SD0 Data(C);
5	PB5	I/O	8/64	GPIO	ADC13:ADC Input Channel 13; SD0CMDC:SD0 Command(C);
6	PB4	I/O	8/64	GPIO	ADC12:ADC Input Channel 12; SD0CLKC:SD0 Clock(C);
7	PB2	I/O	8/64	GPIO	SPI1DIA:SPI1 Data In(A); SD0DATB:SD0 Data(B); TDM_DAT;
8	PB1	I/O	8/64	GPIO (pull down)	ADC11:ADC Input Channel 11; SPI1DOA:SPI1 Data Out(A); SD0CMDB:SD0 Command(B); I2C_SDA(A); TDM_SYN;
9	PB0	I/O	8/64	GPIO (pull down)	ADC10:ADC Input Channel 10; SPI1CLKA:SPI1 Clock(A); SD0CLKB:SD0 Clock(B); I2C_SCL(A); TDM_CLK;
10	PA15	I/O	8/64	GPIO	ADC9:ADC Input Channel 9; SPI1DOB:SPI1 Data Out(B); MCAP3:Motor Timer3 Capture;

11	PA14	I/O	8/64	GPIO	ADC8:ADC Input Channel 8; SPI1CLKB:SPI1 Clock(B); CAP0:Timer0 Capture; MCAP2:Motor Timer2 Capture;
12	PA13	I/O	8/64	GPIO	SPI1DIB:SPI1 Data In(B); TMR1:Timer1 Clock In; MCAP1:Motor Timer1 Capture;
13	PA12	I/O	8/64	GPIO	MPWM3:PWM Channel3 Output;
14	PA11	I/O	8/64	GPIO	TMR0:Timer0 Clock In; MPWM2:PWM Channel2 Output;
15	PD2	I/O	8/64	GPIO (pull up)	SPI0CSA:SPI0 Chip Select(A); SFCCSA:SFC Chip Select(A);
16	PD1	I/O	8/64	GPIO	SPI0DOA(0):SPI0 Data0 Out(A); SFCDOA(0):SFC Data0 Out(A);
17	PD0	I/O	8/64	GPIO	SPI0CLKA:SPI0 Clock(A); SFCCLKA:SFC Clock(A);
18	PA7	I/O	8/64	GPIO	ADC7:ADC Input Channel 7; SPI1DOC:SPI1 Data Out(C); UART0RXA:Uart0 Data In(A); I2C_SDA(C); MPWM1:PWM Channel1 Output;
19	PA6	I/O	8/64	GPIO	ADC6:ADC Input Channel 6; SPI1CLKC:SPI1 Clock(C); UART0TXA:Uart0 Data Out(A); I2C_SCL(C); TMR2:Timer2 Clock In; MPWM0:PWM Channel0 Output;
20	PA3	I/O	8/64	GPIO	ADC3:ADC Input Channel 3; SPI0DIB(1):SPI0 Data1 In(B); SD0DATA:SD0 Data(A); CLKOUT; PWM2(B); MCAP0:Motor Timer0 Capture;
21	PA2	I/O	8/64	GPIO	ADC2:ADC Input Channel 2; SPI0DOB(0):SPI0 Data0 Out(B); SD0CMDA:SD0 Command(A); I2C_SDA(B); PWM2(A);

22	PA1	I/O	8/64	GPIO	ADC1:ADC Input Channel 1; SPI0CLKB:SPI0 Clock(B); SD0CLKA:SD0 Clock(A); UART0RXB:Uart0 Data In(B); I2C_SCL(B); CAP2:Timer2 Capture;
23	PA0	I/O	8/64	GPIO (pull up)	Long Press Reset; ADC0:ADC Input Channel 0; UART0TXB:Uart0 Data Out(B);
24	VDDIO	P	/		Digital Power; (Internal linear regulator output)
25	VBAT	P	/		Battery Power Supply;
26	VSS	G			Ground;
27	DACP	O	/		Class-D APA Positive Output;
28	DACN	O	/		Class-D APA Negative Output;
	PB11	I/O	8	GPIO (High Voltage Resistance)	OSCIB:Crystal Oscillator Input(B);

2、Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Tamb	Ambient Temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	5.5	V
$V_{VDDIO33}$	3.3V IO Input Voltage	-0.3	3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.0	3.7	5.5	V	_
V_{VDDIO}	Voltage output	2.0	3.0	3.4	V	VBAT = 3.7V, 100mA loading
I_{VDDIO}	Loading current	_	_	100	mA	VBAT=3.7V

2.3 IO Input/Output Electrical Logical Characteristics

Table 2-3

IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* VDDIO	V	VDDIO = 3.3V
V_{IH}	High-Level Input Voltage	0.7* VDDIO	_	VDDIO+0.3	V	VDDIO = 3.3V
IO output characteristics						
V_{OL}	Low-Level Output Voltage	_	_	0.33	V	VDDIO = 3.3V
V_{OH}	High-Level Output Voltage	2.7	_	_	V	VDDIO = 3.3V

2.4 Internal Resistor Characteristics

Table 2-4

Port	General Output	High Drive	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA0~PA3 PA6,PA7 PA11~PA15 PB0~PB2 PB4~PB6 PD0~PD2	8mA	64mA	10K	60K	1、PA0,PB10,PD2 default pull up 2、PB0 & PB1 default pull down 3、internal pull-up/pull-down resistance	accuracy ±20%
PB8~PB11	8mA	_	10K	60K	

3、 Package Information

3.1 QSOP28

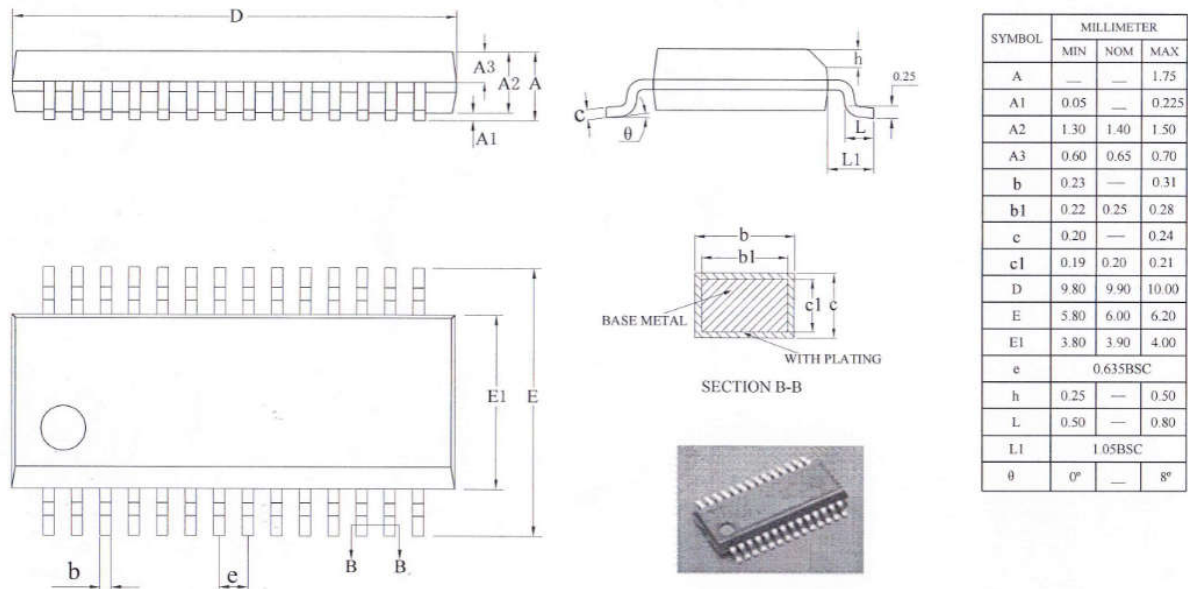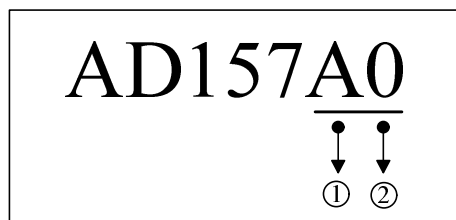| SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0°	—	8°

Figure 3-1. AD157A0_QSOP28 Package

4、 Package Type Specification

AD157A0

①②

①Represents different packages

②Represents different memory sizes

  0: No memory

  2: 2Mbit Flash

  4: 4Mbit Flash

  8: 8Mbit Flash

5、 Revision History

Date	Revision	Description
2021.10.21	V1.0	Initial Release