AD154 Datasheet

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AD154 Features

CPU Core

- 32-bit CPU,Built-in ICACH, can be connected to Flash for expansion of code
- The main frequency is up to 120MHz

Memory

- Built-in 28Kbytes of SRAM
- 8Kbytes 2-Way Icache

Clock Source

- RC Clock frequency about 16MHz
- LRC(low power RC) clock frequency about 200KHz

Digital I/O

- Up to 28 programmable digital I/O pins
- General the IO supports pull-up(10k),pull-down(60k), strong,weak output,input and high impedance
- Up to 12 external interrupt/wake-up source(low power available,can be multiplexed to any I/O, with hardware filter)
- Input channel and Output channel, provide arbitrary IO input and output options for some modules

Digital peripherals

- Two UART Controllers(UART0/1) supports DMA and Flow Control
- Two SPI Controllers with DMA(SPI0/1) support master mode and slave mode,SPI0 support 4bit,SPI1support 2bit
- One Spi Flash Controller to run code
- One SD host controller
- Three 32-bit Asynchronous Divider Timers
- One IIC Controller
- Four channel PWM output
- Infrared remote control decoder
- Watchdog
- 64-bit EFUSE

Analog Peripherals

- 0.5 watt Class-D audio amplifier output
- 14 channel 10-bit high precision ADC
- Low voltage protection
- Power on reset

Operating Conditions

- Working voltage
  VBAT: 2.0v - 5.5v
  HPVDD: 2.0v - 5.5v
  VDDIO: 2.0v - 3.4v
- Operating Temperature: -40°C to +85°C

Package

- LQFP48(7mm*7mm)

Application

- Sound Toy
- Audio player

1、Pin Definition

1.1 Pin Assignment

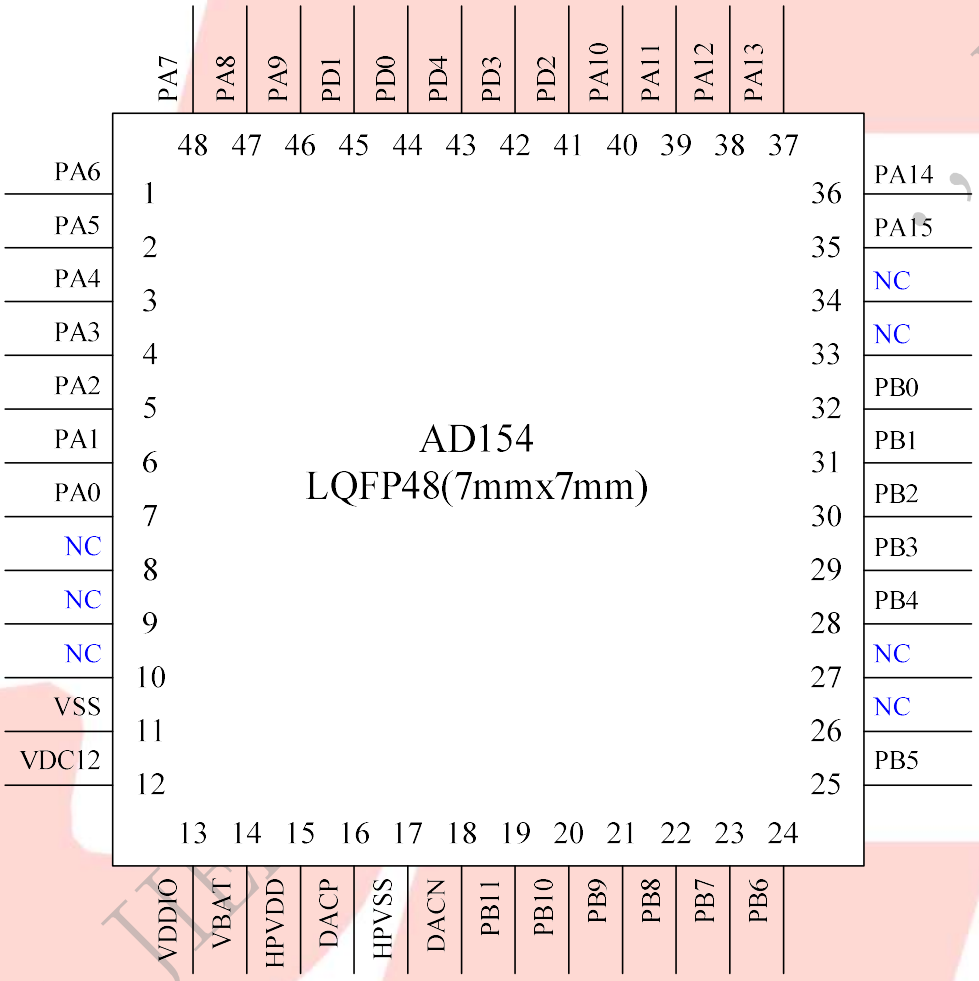


Figure 1-1 AD154_LQFP48 Package Diagram

1.2 Pin Description

Table 1-1 AD154_LQFP48 Pin Description

PIN NO.	Name	Type	Drive (mA)	Function	Description
1	PA6	I/O	8/64	GPIO	ADC6:ADC Input Channel 6; SPI1CLKC:SPI1 Clock(C); SD0CLKD:SD0 Clock(D); UART0TXA:Uart0 Data Out(A); I2C_SCL(C); TMR2:Timer2 Clock In; PWM0:PWM Channel0 Output;
2	PA5	I/O	8/64	GPIO	ADC5:ADC Input Channel 5; SPI0DAT3:SPI0 Data 3 UART1RXA:Uart1 Data In(A);
3	PA4	I/O	8/64	GPIO	ADC4:ADC Input Channel 4; SPI0DAT2:SPI0 Data 2; UART1TXA:Uart1 Data Out(A); LVD:Low Voltage Detect；
4	PA3	I/O	8/64	GPIO	ADC3:ADC Input Channel 3; SPI0DIB(1):SPI0 Data1 In(B); SD0DATA:SD0 Data(A); CLKOUT; PWM2L; MCAP0:Motor Timer0 Capture;
5	PA2	I/O	8/64	GPIO	ADC2:ADC Input Channel 2; SPI0DOB(0):SPI0 Data0 Out(B); SD0CMDA:SD0 Command(A); I2C_SDA(B); PWM2H;
6	PA1	I/O	8/64	GPIO	ADC1:ADC Input Channel 1; SPI0CLKB:SPI0 Clock(B); SD0CLKA:SD0 Clock(A); UART0RXB:Uart0 Data In(B); I2C_SCL(B); CAP2:Timer2 Capture;
7	PA0	I/O	8/64	GPIO (pull up)	Long Press Reset; ADC0:ADC Input Channel 0; UART0TXB:Uart0 Data Out(B);
8	NC	_	_		_

9	NC	_	_		_
10	NC	_	_		_
11	VSS	G	/		Digital Ground;
12	VDC12	P	/		PLL Power;(Connect the bypass capacitor)
13	VDDIO	P	/		Digital Power; (Internal linear regulator output)
14	VBAT	P	/		Battery Power Supply;
15	HPVDD	P	/		Class-D APA Power Supply;
16	DACP	O	/		Class-D APA Positive Output;
17	HPVSS	G	/		Class-D APA Ground;
18	DACN	O	/		Class-D APA Negative Output;
19	PB11	I/O	8	GPIO (High Voltage Resistance)	OSCIB:Crystal Oscillator Input(B);
20	PB10	I/O	8	GPIO (pull up) (High Voltage Resistance)	MCLR(0 effective);
21	PB9	I/O	8	GPIO (High Voltage Resistance)	SPI1DOD:SPI1 Data Out(D); UART1TRXB:Uart1 Data In/Out(B); I2C_SDA(D); CAP1:Timer1 Capture;
22	PB8	I/O	8	GPIO (High Voltage Resistance)	SPI1CLKD:SPI1 Clock(D); I2C_SCL(D); OSCIA:Crystal Oscillator Input(A);
23	PB7	I/O	8/64	GPIO	SPI1DID:SPI1 Data In(D);
24	PB6	I/O	8/64	GPIO	SD0DATC:SD0 Data(C);
25	PB5	I/O	8/64	GPIO	ADC13:ADC Input Channel 13; SD0CMDC:SD0 Command(C);
26	NC	_	_		_
27	NC	_	_		_
28	PB4	I/O	8/64	GPIO	ADC12:ADC Input Channel 12; SD0CLKC:SD0 Clock(C);
29	PB3	I/O	8/64	GPIO	TDM_MCLK;
30	PB2	I/O	8/64	GPIO	SPI1DIA:SPI1 Data In(A); SD0DATB:SD0 Data(B); TDM_DAT;

31	PB1	I/O	8/64	GPIO (pull down)	ADC11:ADC Input Channel 11; SPI1DOA:SPI1 Data Out(A); SD0CMDB:SD0 Command(B); I2C_SDA(A); TDM_SYN;
32	PB0	I/O	8/64	GPIO (pull down)	ADC10:ADC Input Channel 10; SPI1CLKA:SPI1 Clock(A); SD0CLKB:SD0 Clock(B); I2C_SCL(A); TDM_CLK;
33	NC	_	_		_
34	NC	_	_		_
35	PA15	I/O	8/64	GPIO	ADC9:ADC Input Channel 9; SPI1DOB:SPI1 Data Out(B); MCAP3:Motor Timer3 Capture;
36	PA14	I/O	8/64	GPIO	ADC8:ADC Input Channel 8; SPI1CLKB:SPI1 Clock(B); CAP0:Timer0 Capture; MCAP2:Motor Timer2 Capture;
37	PA13	I/O	8/64	GPIO	SPI1DIB:SPI1 Data In(B); TMR1:Timer1 Clock In; MCAP1:Motor Timer1 Capture;
38	PA12	I/O	8/64	GPIO	PWM3:PWM Channel3 Output;
39	PA11	I/O	8/64	GPIO	TMR0:Timer0 Clock In; PWM2:PWM Channel2 Output;
40	PA10	I/O	8/64	GPIO	
41	PD2	I/O	8/64	GPIO (pull up)	SPI0CSA:SPI0 Chip Select(A); SFCCSA:SFC Chip Select(A);
42	PD3	I/O	8/64	GPIO	SPI0DIA(1):SPI0 Data1 In(A); SFCDIA(1):SFC Data1 In(A);
43	PD4	I/O	8/64	GPIO	Flash Power Gate;
44	PD0	I/O	8/64	GPIO	SPI0CLKA:SPI0 Clock(A); SFCCLKA:SFC Clock(A);
45	PD1	I/O	8/64	GPIO	SPI0DOA(0):SPI0 Data0 Out(A); SFCDOA(0):SFC Data0 Out(A);
46	PA9	I/O	8/64	GPIO	
47	PA8	I/O	8/64	GPIO	SPI1DIC:SPI1 Data In(C); SD0DATD:SD0 Data(D);

48	PA7	I/O	8/64	GPIO	ADC7:ADC Input Channel 7; SPI1DOC:SPI1 Data Out(C); SD0CMDD:SD0 Command(D); UART0RXA:Uart0 Data In(A); I2C_SDA(C); PWM1:PWM Channel1 Output;

2、Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Tamb	Ambient Temperature	-40	+85	℃
Tstg	Storage temperature	-65	+150	℃
VBAT	Supply Voltage	-0.3	5.5	V
HPVDD	Class D Audio Power Amplifier	-0.3	5.5	V
$V_{VDDIO33}$	3.3V IO Input Voltage	-0.3	3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.0	3.7	5.5	V	_
V_{HPVDD}	Voltage Input	2.0	3.7	5.5	V	_
V_{VDDIO}	Voltage output	2.0	3.0	3.4	V	VBAT = 3.7V, 100mA loading
V_{VDC12}	Voltage output	1.05	1.2	1.4	V	VBAT=3.7V
I_{VDDIO}	Loading current	_	_	100	mA	VBAT=3.7V

2.3 IO Input/Output Electrical Logical Characteristics

Table 2-3

IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* VDDIO	V	VDDIO = 3.3V
V_{IH}	High-Level Input Voltage	0.7* VDDIO	_	VDDIO+0.3	V	VDDIO = 3.3V
IO output characteristics						
V_{OL}	Low-Level Output Voltage	_	_	0.33	V	VDDIO = 3.3V
V_{OH}	High-Level Output Voltage	2.7	_	_	V	VDDIO = 3.3V

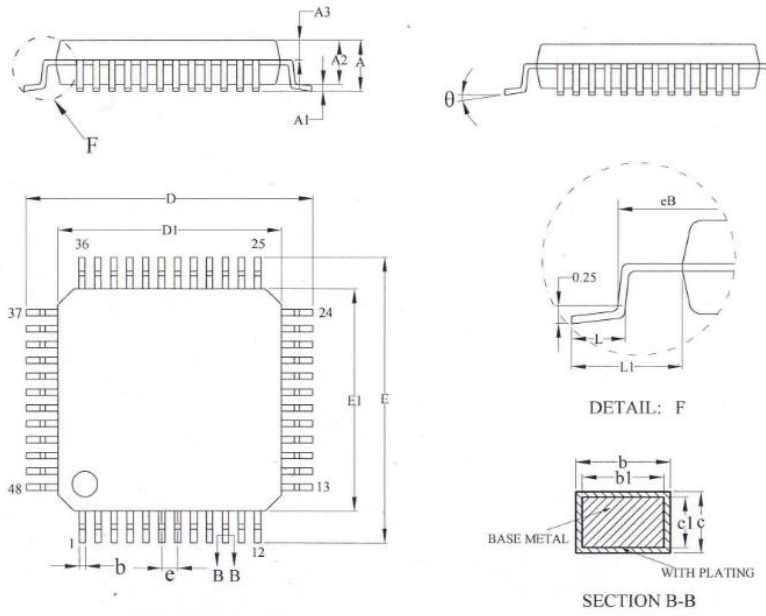
2.4 Internal Resistor Characteristics

Table 2-4

Port	General Output	High Drive	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA0~PA15 PB0~PB7 PD0~PD4	8mA	64mA	10K	60K	1、PA0,PB10,PD2 default pull up 2、PB0 & PB1 default pull down 3、internal pull-up/pull-down resistance | accuracy ±20%
PB8~PB11	8mA	_	10K	60K	

3、 Package Information

3.1 LQFP48(7mm*7mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.50BSC		
L	0.40	—	0.65
L1	1.00REF		
θ	0	—	7°

Figure 3-1. AD154_LQFP48 Package

4、 Revision History

Date	Revision	Description
2021.03.23	V1.0	Initial Release