AD159A Datasheet

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AD159A Features

CPU Core

- 32-bit CPU,Built-in ICACH, can be connected to Flash for expansion of code
- The main frequency is up to 120MHz

Memory

- Built-in Flash memory

Clock Source

- RC Clock frequency about 16MHz
- LRC(low power RC) clock frequency about 200KHz

Digital I/O

- Up to 17 programmable digital I/O pins
- General the IO supports pull-up(10k),pull-down(60k), strong,weak output,input and high impedance
- Up to 12 external interrupt/wake-up source(low power available,can be multiplexed to any I/O, with hardware filter)
- Input channel and Output channel, provide arbitrary IO input and output options for some modules

Digital peripherals

- Two UART Controllers(UART0/1) supports DMA and Flow Control
- Two SPI Controllers with DMA(SPI0/1) support master mode and slave mode
- Built-in Spi Flash to run code
- One SD host controller
- Three 32-bit Asynchronous Divider Timers
- One IIC Controller
- Four channel PWM output
- Infrared remote control decoder
- Watchdog

Analog Peripherals

- 0.5 watt Class-D audio amplifier output
- 10-bit high precision ADC
- Low voltage protection
- Power on reset

Operating Conditions

- Working voltage
  VBAT: 2.0v - 5.5v
  VDDIO: 2.0v - 3.4v
- Soft-off current is 2uA
- Power down current is 27uA
- Operating Temperature: -40°C to +85°C

Package

- QFN20

Application

- Universal Micro controller
- Sound Toy
- Audio player

1 Pin Definition

1.1 Pin Assignment

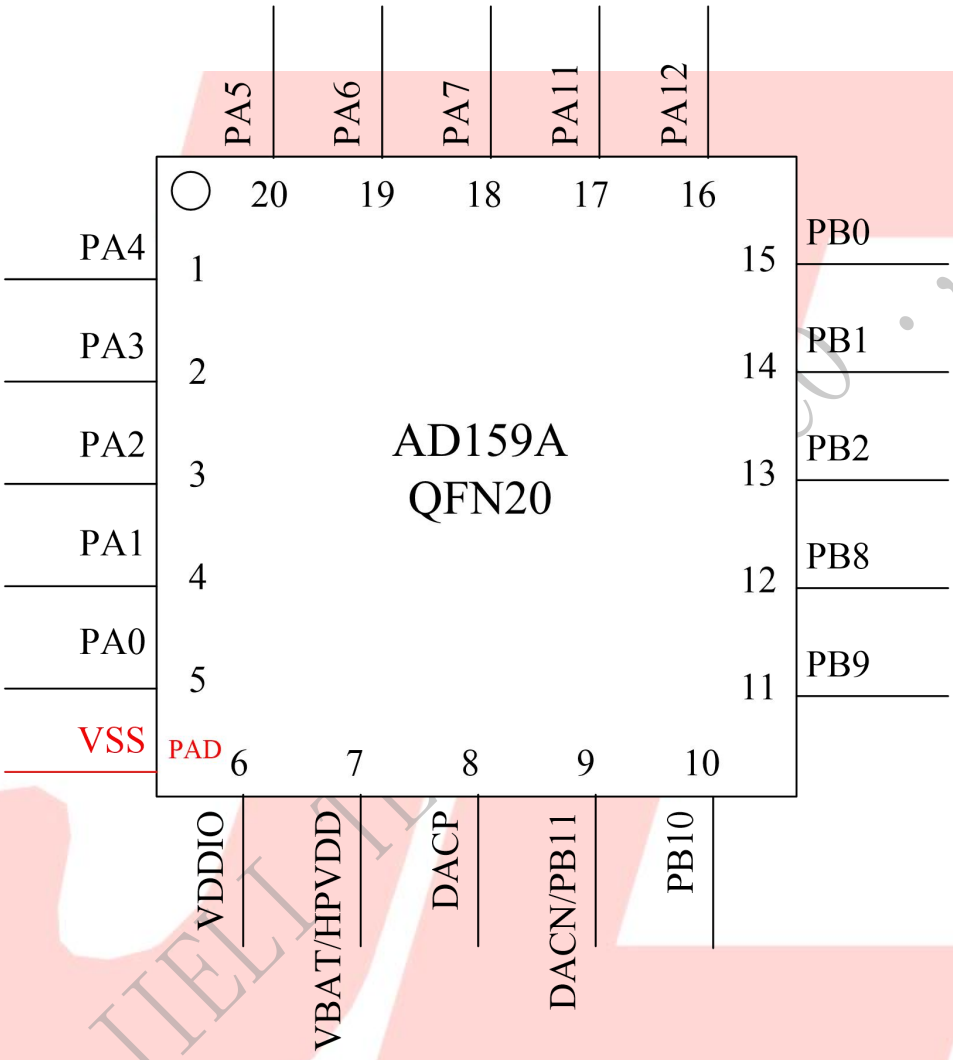


Figure 1-1 AD159A_QFN20 Package Diagram

1.2 Pin Description

Table 1-1 AD159A_QFN20 Pin Description

PIN NO.	Name	Type	Drive (mA)	Function	Description
1	PA4	I/O	8/64	GPIO	ADC4:ADC Input Channel 4; SPI0DAT2:SPI0 Data 2; UART1TXA:Uart1 Data Out(A); LVD:Low Voltage Detect；
2	PA3	I/O	8/64	GPIO	ADC3:ADC Input Channel 3; SPI0DIB(1):SPI0 Data1 In(B); SD0DATA:SD0 Data(A); CLKOUT; PWM2B; MCAP0:Motor Timer0 Capture;
3	PA2	I/O	8/64	GPIO	ADC2:ADC Input Channel 2; SPI0DOB(0):SPI0 Data0 Out(B); SD0CMDA:SD0 Command(A); I2C_SDA(B); PWM2A;
4	PA1	I/O	8/64	GPIO	ADC1:ADC Input Channel 1; SPI0CLKB:SPI0 Clock(B); SD0CLKA:SD0 Clock(A); UART0RXB:Uart0 Data In(B); I2C_SCL(B); CAP2:Timer2 Capture;
5	PA0	I/O	8/64	GPIO (pull up)	Long Press Reset; ADC0:ADC Input Channel 0; UART0TXB:Uart0 Data Out(B);
6	VDDIO	P	/		Digital Power; (Internal linear regulator output)
7	VBAT	P	/		Battery Power Supply;
	HPVDD	P	/		Class-D APA Power Supply;
8	DACP	O	/		Class-D APA Positive Output;
9	DACN	O	/		Class-D APA Negative Output;
	PB11	I/O	8	GPIO (High Voltage Resistance)	OSCIB:External clock Input(B);
10	PB10	I/O	8	GPIO (pull up) (High Voltage Resistance)	MCLR(0 effective);

11	PB9	I/O	8	GPIO (High Voltage Resistance)	SPI1DOD:SPI1 Data Out(D); UART1TRXB:Uart1 Data In/Out(B); I2C_SDA(D); CAP1:Timer1 Capture;
12	PB8	I/O	8	GPIO (High Voltage Resistance)	SPI1CLKD:SPI1 Clock(D); I2C_SCL(D); OSCIA:External clock Input(A);
13	PB2	I/O	8/64	GPIO	SPI1DIA:SPI1 Data In(A); SD0DATB:SD0 Data(B);
14	PB1	I/O	8/64	GPIO (pull down)	ADC11:ADC Input Channel 11; SPI1DOA:SPI1 Data Out(A); SD0CMDB:SD0 Command(B); I2C_SDA(A);
15	PB0	I/O	8/64	GPIO (pull down)	ADC10:ADC Input Channel 10; SPI1CLKA:SPI1 Clock(A); SD0CLKB:SD0 Clock(B); I2C_SCL(A);
16	PA12	I/O	8/64	GPIO	MPWM3:PWM Channel3 Output;
17	PA11	I/O	8/64	GPIO	TMR0:Timer0 Clock In; MPWM2:PWM Channel2 Output;
18	PA7	I/O	8/64	GPIO	ADC7:ADC Input Channel 7; SPI1DOC:SPI1 Data Out(C); UART0RXA:Uart0 Data In(A); I2C_SDA(C); MPWM1:PWM Channel1 Output;
19	PA6	I/O	8/64	GPIO	ADC6:ADC Input Channel 6; SPI1CLKC:SPI1 Clock(C); UART0TXA:Uart0 Data Out(A); I2C_SCL(C); TMR2:Timer2 Clock In; PWM0:PWM Channel0 Output;
20	PA5	I/O	8/64	GPIO	ADC5:ADC Input Channel 5; SPI0DAT3:SPI0 Data 3； UART1RXA:Uart1 Data In(A);
PAD	VSS	G	/		Ground;

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Tamb	Ambient Temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	5.5	V
HPVDD	Class D Audio Power Amplifier	-0.3	5.5	V
$V_{VDDIO33}$	3.3V IO Input Voltage	-0.3	3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below.

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.0	3.7	5.5	V	_
V_{HPVDD}	Voltage Input	2.0	3.7	5.5	V	_
V_{VDDIO}	Voltage output	2.0	3.0	3.4	V	VBAT = 3.7V, 100mA loading
I_{VDDIO}	Loading current	_	_	100	mA	VBAT=3.7V

2.3 IO Input/Output Electrical Logical Characteristics

Table 2-3

IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* VDDIO	V	VDDIO = 3.3V
V_{IH}	High-Level Input Voltage	0.7* VDDIO	_	VDDIO+0.3	V	VDDIO = 3.3V
IO output characteristics						
V_{OL}	Low-Level Output Voltage	_	_	0.33	V	VDDIO = 3.3V
V_{OH}	High-Level Output Voltage	2.7	_	_	V	VDDIO = 3.3V

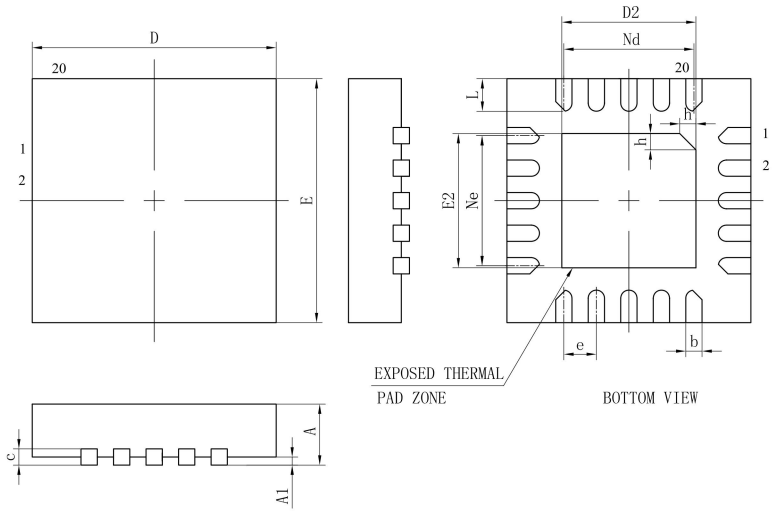
2.4 Internal Resistor Characteristics

Table 2-4

Port	General Output	High Drive	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA0~PA12 PB0~PB2	8mA	64mA	10K	60K	1、PA0 default pull up 2、PB0 & PB1 default pull down 3、internal pull-up/pull-down resistance | accuracy ±20%
PB8~PB11 (High Voltage Resistance)	8mA	_	10K	60K	

3 Package Information

3.1 QFN20



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30
L/F载体尺寸 (附注1)	75*75		

Figure 3-1. AD159A_QFN20 Package

4 Package Type Specification

①Represents different packages

②Represents different memory sizes

0: No memory

2: 2Mbit Flash

4: 4Mbit Flash

8: 8Mbit Flash

5 Revision History

Date	Revision	Description
2021.06.23	V1.0	Initial Release
2023.03.23	V1.1	Modify the Features.