EE660: Computer Architecture **Spring, 2017**

Assignment No. 2 (Due: Feburary 24, 2017)

Score: ____/100

Student: your name, your email *Date: February 3, 2017*

2.1 (20/100). Draw the pipeline diagram of the following code executing on the shown in-order two-way superscalar processor. Assume that branches execute in pipeline A, loads/stores in pipeline B. Assume full bypassing when possible and no alignment problems.

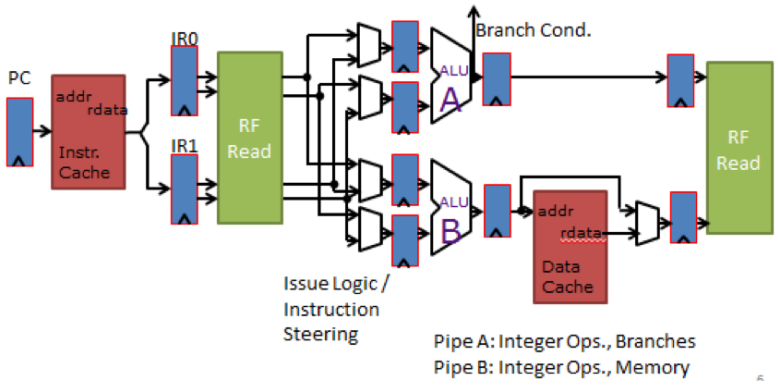

Figure 2.1: Two-Wide In-order Superscalar Processor Pipeline.

```
ADD R5, R6, R7
SUB R6, R7, R8
LW R10, R6(0)
ADDIU R12, R13, 1
LW  R15, R6(4)
LW  R15, R15(4)
ADD R6, R9, R10
ADDIU R8, R10, R11
```

2.2 (20/100). Given that you have an architecture which has the following pipeline stages:

F D I X0 X1 W

and that register fetch happens in the I stage of the pipeline and branch resolution happens in X1, how many dead instructions are need to be killed when a branch miss-predict is taken? Now assume that the pipeline is a three-wide superscalar, how many instructions need to be killed on a branch miss-predict? (Assume that the branch is the first instruction executing after a jump.)

2.3 (20/100). [PH11], page 248-249, problem 3.3-3.4.

2.4 (20/100). Assume that you have the IO2I pipeline from lecture. It can issue one instruction per cycle and can commit one instruction per cycle. Draw the pipeline diagram of the following code sequence executing.

```
MUL R6, R7, R8
ADD R9, R10, R11
ADD R11, R12, R13
ADD R13, R14, R15
ADD R19, R13, R10
LW R2, R3
ADD R12, R16, R19
LW R5, R2
ADD R15, R20, R21
```

2.5 (20/100). Assume architecture I2OI from lecture. Draw the state of the scoreboard when instruction 3 is in the I (Issue) stage of the pipeline.

```
0: MUL R6, R7, R8
1: ADD R9, R6, R11
2: MUL R7, R1, R2
3: LW R10, R12
```

References

[PH11] David A. Patterson and John L. Hennessy. *Computer Architecture: A Quantitative Approach*. 5th ed. Morgan Kaufmann Publishers Inc., 2011. ISBN: 9780123838728.