EE660: Computer Architecture **Spring, 2017**

Assignments 1 (Due: January 26, 2017)

Score:_____/100

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1-1 (20/100). [PH11], page 65, problem 1.9-a,b.

Solution 1-1-1:

1.9 a.

Because the system can execute the code twice as fast as necessary, we can turn off the system half of the time such that the performance still meet the requirement. Therefore the energy saved by this is **50%**.

Solution 1-1-2:

1.9 b

Frequency does not affect the total energy used. So the new energy is 50% *$(V/2)^2$ = 1/4 E.
So it saves 1-1/4 = 3/4 energy

1-2 (40/100). [PH11], page C-82, problem C.1-a,b,c,d,e,f,g.

Solution 1-2-1:

a.

Register R1 from LD to DADDI
Register R1 from first DADDI to SD
Register R2 from second DADDI to DSUB
Register R4 from DSUB to BNEZ
Register R2 from second DADDI to LD
Register R2 from second DADDI to SD

b.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
LD	F	D	X	M	W															
DADDI		F	D	D	D	X	M	W												
SD			F	F	F	D	D	D	X	M	W									
DADDI						F	F	F	D	X	M	W								
DSUB									F	D	D	D	X	M	W					
BNEZ										F	F	F	D	D	D	X	M	W		
LD																	F	D	X	M	W

Therefore, it takes 16 cycles to execute.

c.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
LD	F	D	X	M	W															
DADDI		F	D	D	X	M	W													
SD			F	F	D	X	M	W												
DADDI				F	D	X	M	W												
DSUB					F	D	X	M	W											
BNEZ						F	D	X	M	W										
(END)							F													
LD									F	D	X	M	W							

It takes 8 cycles to execute.

d.

```
                1  2  3  4  5  6  7  8  9  10 11 12 13 14 15 16 17 18 19 20
LD              F  D  X  M  W
DADDI              F  D  D  X  M  W
SD                    F  F  D  X  M  W
DADDI                    F  D  X  M  W
DSUB                        F  D  X  M  W
BNEZ                           F  D  X  M  W
LD                                F  D  X  M  W
```

It takes 7 cycles to execute.

e.

```
                1  2  3  4  5  6  7  8  9  10 11 12 13 14 15 16 17 18 19 20 21 22
LD              F1 F2 D1 D2 X1 X2 M1 M2 W1 W2
DADDI              F1 F2 D1 D2 D2 D2 D2 X1 X2 M1 M2 W1 W2
SD                    F1 F2 D1 D1 D1 D1 D2 X1 X2 M1 M2 W1 W2
DADDI                    F1 F2 F2 F2 F2 D1 D1 D2 X1 X2 M1 M2 W1 W2
DSUB                        F1 F1 F1 F1 F2 F2 D1 D2 D2 X1 X2 M1 M2 W1 W2
BNEZ                                    F1 F1 F2 D1 D1 D2 D2 X1 X2 M1 M2 W1 W2
LD                                         F1 F2 F2 D1 D1 D2 X1 X2 M1 M2 W1 W2
```

It takes 10 cycles to execute.

f.

For 5-stage, 0.8ns + 0.1ns = 0.9ns
For 10-stage, 0.4ns + 0.1ns = 0.5ns

g.

For (d), there are 7 clock cycles, so it is 7/6 = 1.166CPI.
For (e), there are 10 clock cycles, so it is 10/6 = 1.666CPI

For 5-stage, the average instruction execute time = 1.166 * 0.9ns = 1.05ns.
For 10-stage, the average instruction execute time = 1.666*0.5ns = 0.833ns

1-3 (40/100). [PH11], page C-85, problem C.6-a,b,c,d,e.

Solution 1-3-1:
Your solution

a.

F D M X W

b.

We can forward stage M, X and W back to Decode stage and stall on back-to-back ALU operations.

c.

ALU Ops are dependant: ADD R3, R4, R5

SUB R6, R3, R7

ALU feed LD/ST: ADD R3, R4, R5

LD R6, R3

ALU feed memory-register: ADD R3, R4, R5

SUB R6, R7, (R3)

d.

If LD and ST instructions has register indirect addressing now has to use 2 instructions:

Original: LW R4, 10(R3)

New: ADDI R5, R3, 10

LW R4, R5

If there are instructions with direct addressing LD and followed by ALU operations, these two instructions can merge into one instruction:

Original: LW R5, 0(R4)

ADD R6, R5, R7

New: ADD R6, R7, (R4)

e.

We can see from f, that if LD followed by dependant instructions, it will not stall, therefore, it has lower CPI. Also, there will be some situation that one instruction is split into two, this will increase CPI. For example:

ALU -> LD/ST

ALU -> ALU

ALC -> Memory-register

References

[PH11] David A. Patterson and John L. Hennessy. *Computer Architecture: A Quantitative Approach*. 5th ed. Morgan Kaufmann Publishers Inc., 2011. isbn: 9780123838728.