## Specialist Diploma in Embedded Systems: ED5502 Spring 2019, Homework 4

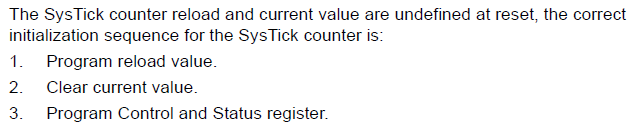
This homework sheet counts for 5% of the module assessment.

Submission date: Friday, 29 March 2019 (Week 10)

**Q1 (SysTick Registers)**

See Pages 245 – 250 of the STM32F4/L4 etc Programming Manual for SysTick details.

Given the following recommendation (p 249):



Write a program fragment to do the following:

Select a SysTick Exception Request on a count to zero

Select AHB/8 as the clock source.

Given an AHB Clock Frequency of 40 MHz, Set the reload register to count down to zero at 1ms intervals. You may ignore the calibration register.

SysTick->CTRL = 0;

SysTick->LOAD = 40000 -1;

NVIC\_SetPriority(SysTick\_IRQn, (1<<\_\_NVIC\_PRIO\_BITS) – 1);

SysTick->CTRL |= 0 << 2; // CLKSOURCE set to AHB/8

SysTick->CTRL |= 1<<1; // TICKINT to count down to zero and asserts the SysTick exception request

SysTick->CTRL |= SysTick\_CTRL\_ENABLE\_Msk;

**Q2 (STM32L476 Timer 1, TIM1)**

See Chapter 30 of the STM32L476RG Reference Manual for details of TIM1. (This is very detailed, you will only need to read the registers section, which starts on page 966).

The Counter and Reload registers are given on page 988 of the Reference Manual. Given a clock frequency of 80 MHz, what is the longest time period that can be defined using these registers?

Time Update frequency = 80\*10^6/1\*65535

Time Update frequency = 1,220ms (1.22Seconds)

**Q3 (STM32L476 Timer 1, TIM1)**

Given an AHB Clock Frequency of 80 MHz and given that TIM1 Prescale value has been set to 16000, find the ARR register value required to generate a time period of 50 ms.

80\*10^6/16000\*TIM\_ARR

TIM1 Clock = 80\*10^6

Prescaler = 16,000

ARR = 100,000

**Q4 (STM32L476 Timer 2, TIM2)**

The STM32L476RG Timer2 is a 32-bit Timer. Repeat Q2 for Timer2, again with 80 MHz as the clock frequency.

Time Update frequency = 80\*10^6/1\* 4294967296

Time Update frequency = 18ms (0.018Seconds)

**Q5 (STM32L476RG ADC Resolution)**

Suppose that ADC1 has been set up with a VREF of 2.5V, and has been initialised to use 12-bit resolution.

1. If an input voltage of 2.27V is applied to a single-ended ADC1 input, what value would you expect to read in the ADC1 Data Register (DR) after a conversion has been completed?

Data Register will be around 3719

1. If the ADC1\_DR result register is read as 1356 (decimal), what voltage was applied to the ADC1 input?

Voltage will be around 0.825V

**Submission:**

Please submit your answers on Sulis before 5pm Friday 29 March 2019, in plain text, MS Word, pdf or any other readable format.

All questions carry equal marks.