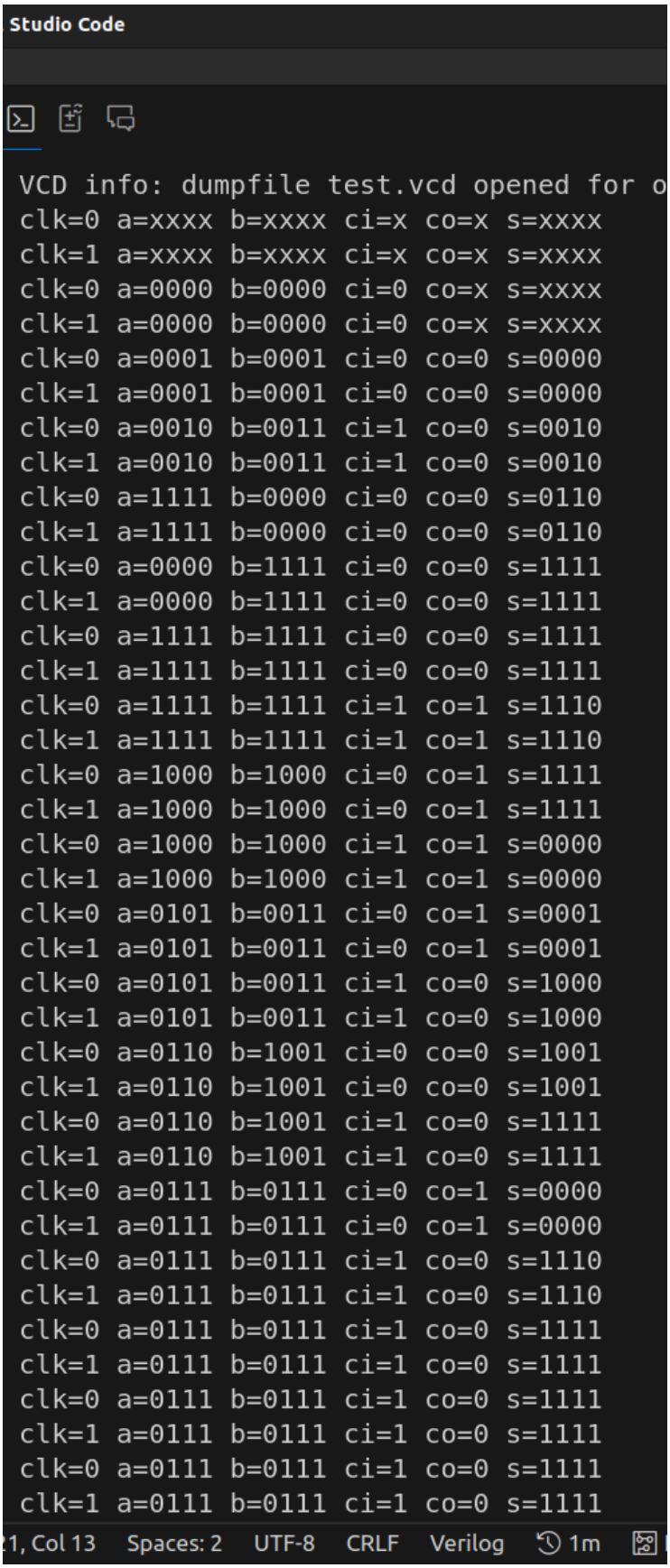
2023112027_ATTACHED PLOTS

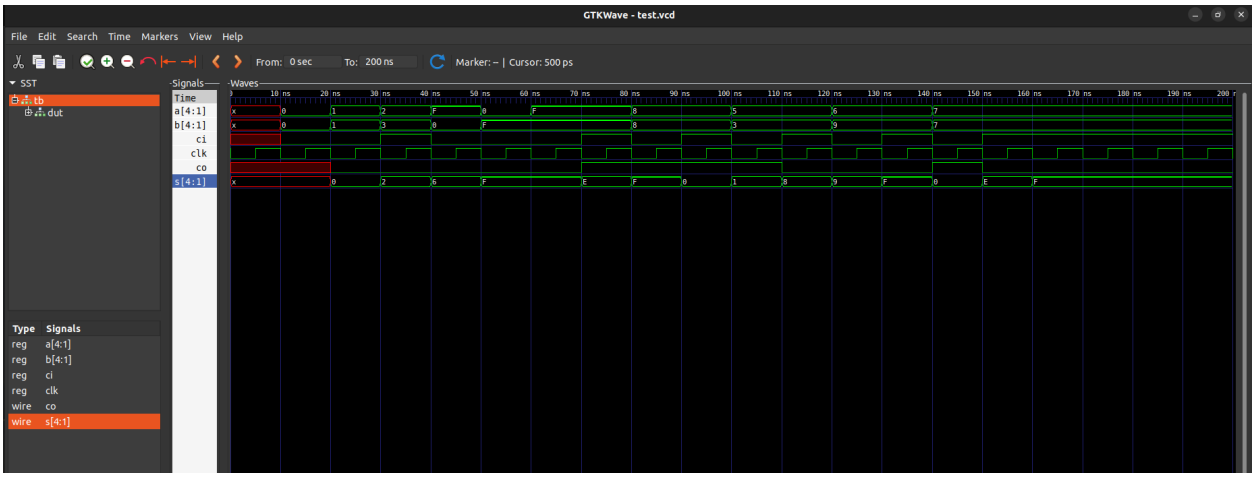
VERILOG PLOTS

- FLIP FLOP

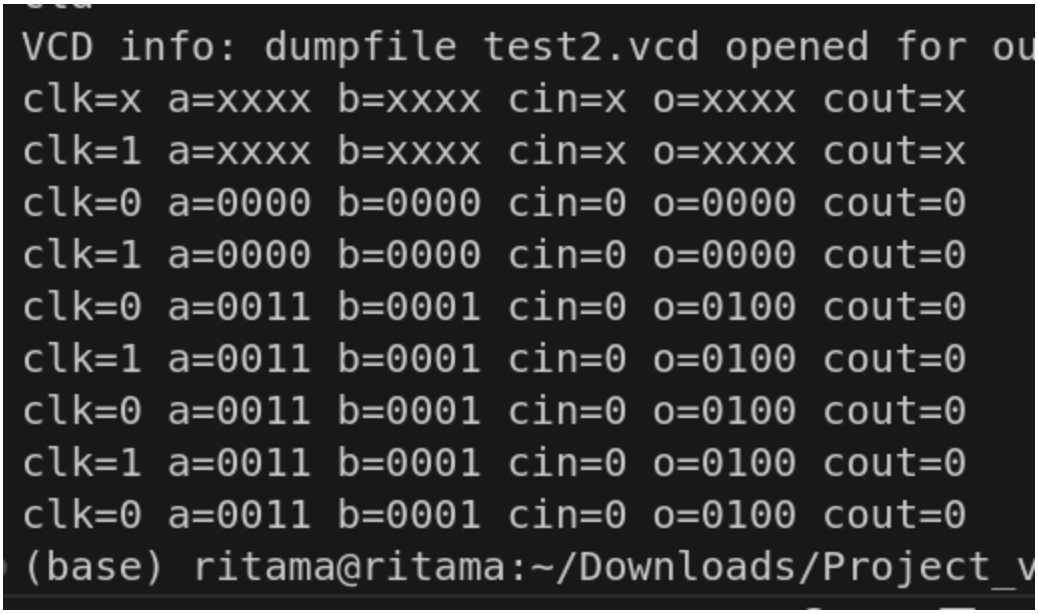
```
VCD info: dumpfile flipflop_wave.vcd opene
D=0 clk=0 Q1=x Qbar1=x Q2=x Qbar2=x
D=1 clk=1 Q1=x Qbar1=x Q2=0 Qbar2=1
D=1 clk=0 Q1=1 Qbar1=0 Q2=0 Qbar2=1
D=0 clk=1 Q1=1 Qbar1=0 Q2=1 Qbar2=0
D=0 clk=0 Q1=0 Qbar1=1 Q2=1 Qbar2=0
D=1 clk=1 Q1=0 Qbar1=1 Q2=0 Qbar2=1
D=1 clk=0 Q1=1 Qbar1=0 Q2=0 Qbar2=1
D=1 clk=1 Q1=1 Qbar1=0 Q2=1 Qbar2=0
D=0 clk=0 Q1=1 Qbar1=0 Q2=1 Qbar2=0
D=1 clk=1 Q1=1 Qbar1=0 Q2=0 Qbar2=1
D=1 clk=0 Q1=1 Qbar1=0 Q2=0 Qbar2=1
D=1 clk=1 Q1=1 Qbar1=0 Q2=1 Qbar2=0
D=1 clk=0 Q1=1 Qbar1=0 Q2=1 Qbar2=0
D=1 clk=1 Q1=1 Qbar1=0 Q2=1 Qbar2=0
(base) ritama@ritama:~/Downloads/Project_v
```

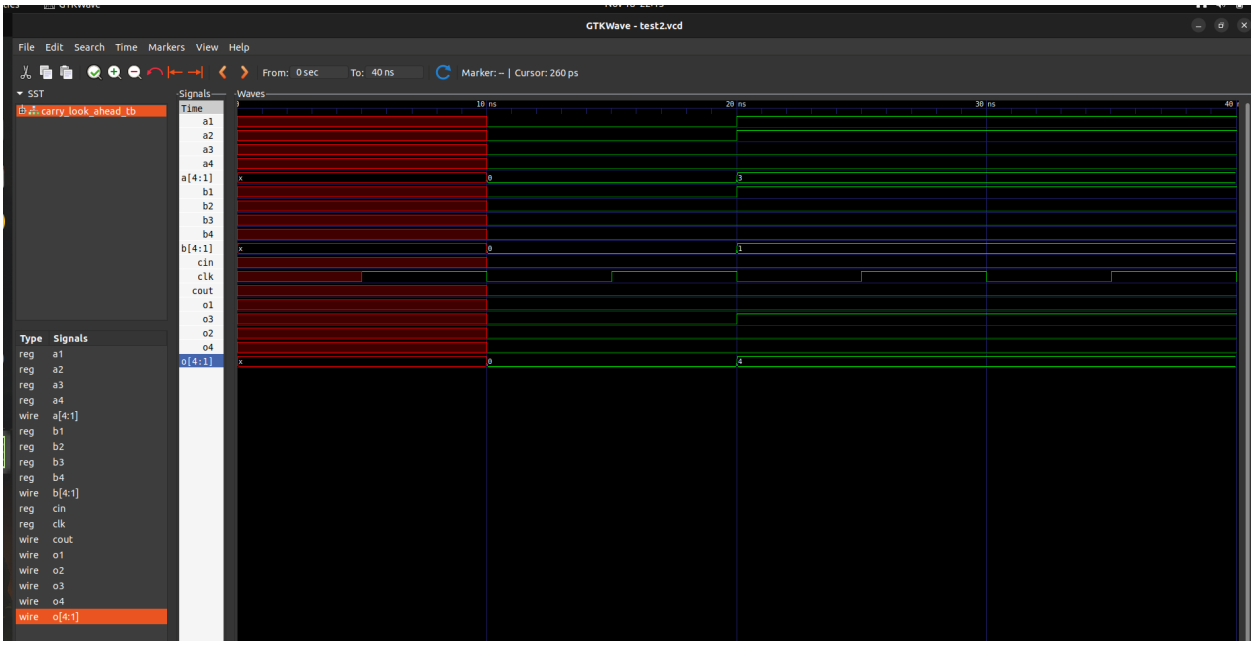
- FINAL CIRCUIT


Studio Code
VCD info: dumpfile test.vcd opened for o
clk=0 a=xxxx b=xxxx ci=x co=x s=xxxx
clk=1 a=xxxx b=xxxx ci=x co=x s=xxxx
clk=0 a=0000 b=0000 ci=0 co=x s=xxxx
clk=1 a=0000 b=0000 ci=0 co=x s=xxxx
clk=0 a=0001 b=0001 ci=0 co=0 s=0000
clk=1 a=0001 b=0001 ci=0 co=0 s=0000
clk=0 a=0010 b=0011 ci=1 co=0 s=0010
clk=1 a=0010 b=0011 ci=1 co=0 s=0010
clk=0 a=1111 b=0000 ci=0 co=0 s=0110
clk=1 a=1111 b=0000 ci=0 co=0 s=0110
clk=0 a=0000 b=1111 ci=0 co=0 s=1111
clk=1 a=0000 b=1111 ci=0 co=0 s=1111
clk=0 a=1111 b=1111 ci=0 co=0 s=1111
clk=1 a=1111 b=1111 ci=0 co=0 s=1111
clk=0 a=1111 b=1111 ci=1 co=1 s=1110
clk=1 a=1111 b=1111 ci=1 co=1 s=1110
clk=0 a=1000 b=1000 ci=0 co=1 s=1111
clk=1 a=1000 b=1000 ci=0 co=1 s=1111
clk=0 a=1000 b=1000 ci=1 co=1 s=0000
clk=1 a=1000 b=1000 ci=1 co=1 s=0000
clk=0 a=0101 b=0011 ci=0 co=1 s=0001
clk=1 a=0101 b=0011 ci=0 co=1 s=0001
clk=0 a=0101 b=0011 ci=1 co=0 s=1000
clk=1 a=0101 b=0011 ci=1 co=0 s=1000
clk=0 a=0110 b=1001 ci=0 co=0 s=1001
clk=1 a=0110 b=1001 ci=0 co=0 s=1001
clk=0 a=0110 b=1001 ci=1 co=0 s=1111
clk=1 a=0110 b=1001 ci=1 co=0 s=1111
clk=0 a=0111 b=0111 ci=0 co=1 s=0000
clk=1 a=0111 b=0111 ci=0 co=1 s=0000
clk=0 a=0111 b=0111 ci=1 co=0 s=1110
clk=1 a=0111 b=0111 ci=1 co=0 s=1110
clk=0 a=0111 b=0111 ci=1 co=0 s=1111
clk=1 a=0111 b=0111 ci=1 co=0 s=1111
clk=0 a=0111 b=0111 ci=1 co=0 s=1111
clk=1 a=0111 b=0111 ci=1 co=0 s=1111
clk=0 a=0111 b=0111 ci=1 co=0 s=1111
clk=1 a=0111 b=0111 ci=1 co=0 s=1111
1, Col 13 Spaces: 2 UTF-8 CRLF Verilog 1m



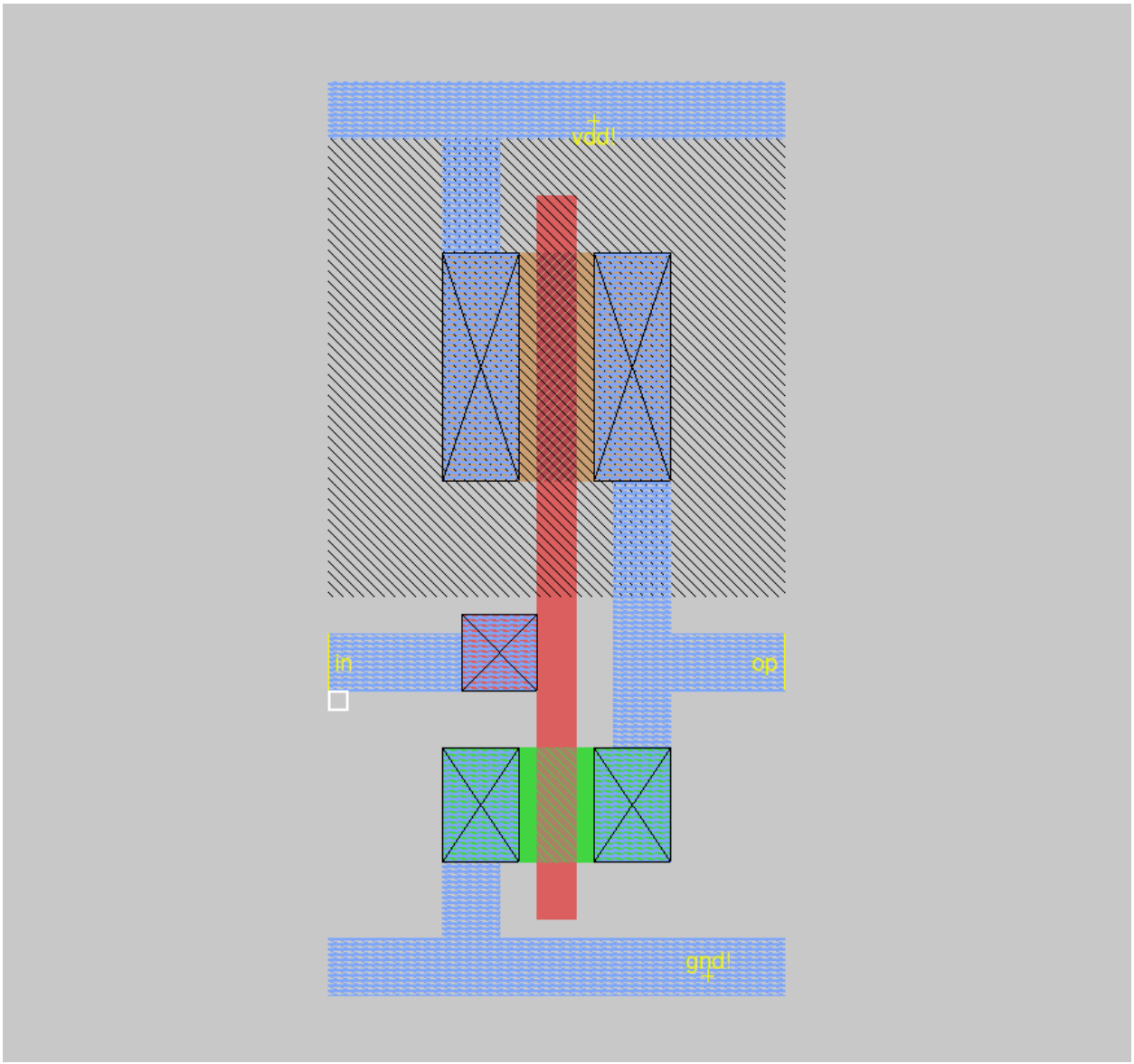
- CARRY LOOK AHEAD

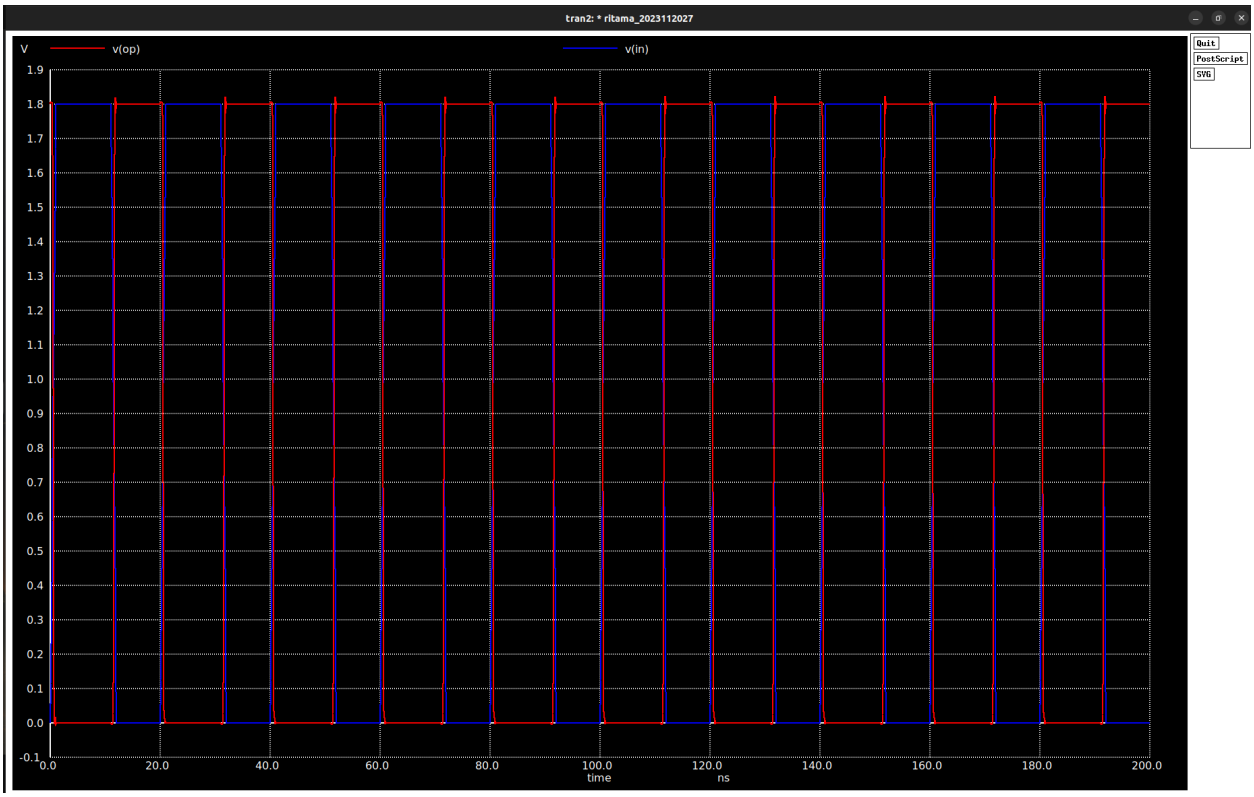




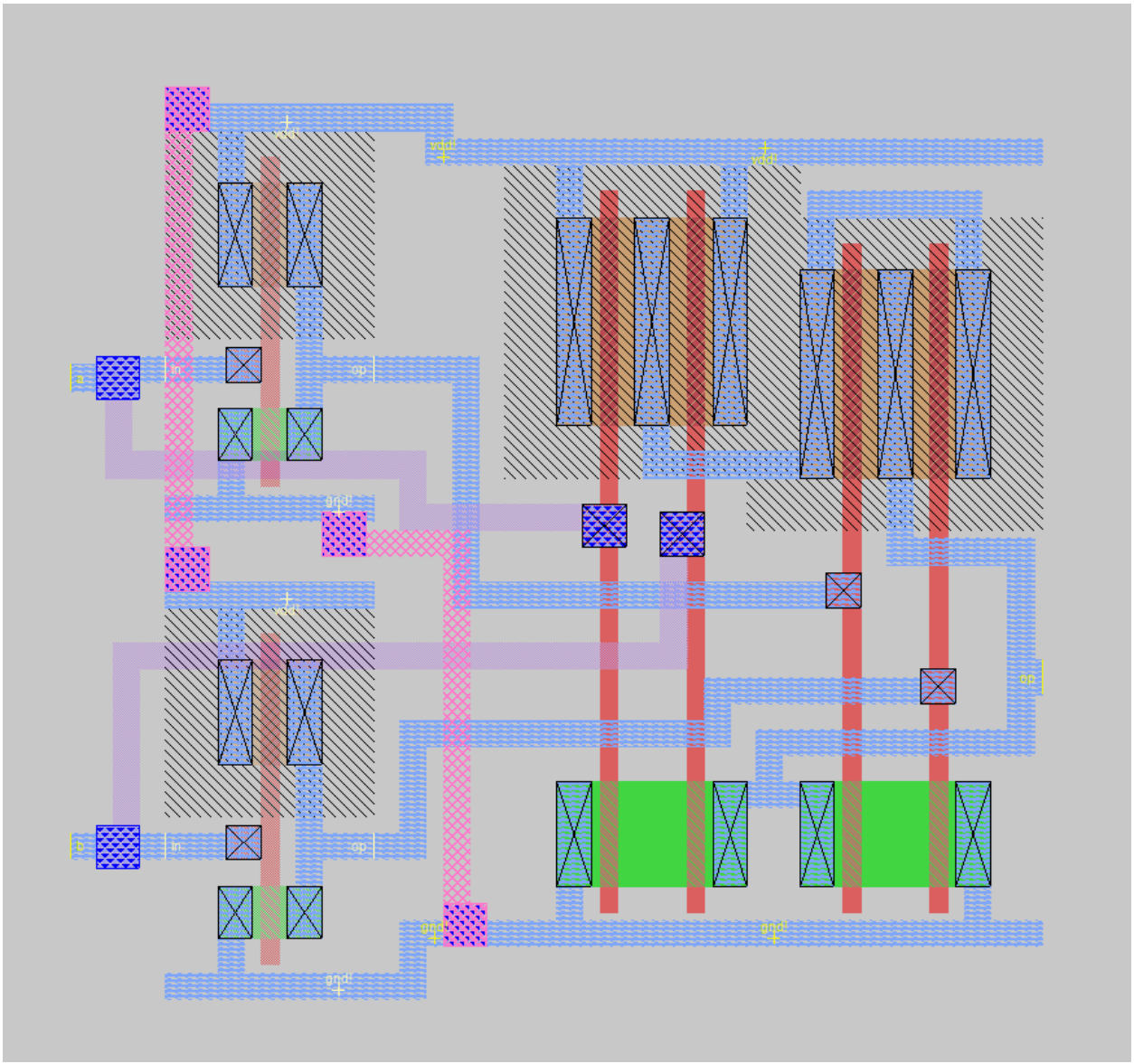
MAGIC PLOTS

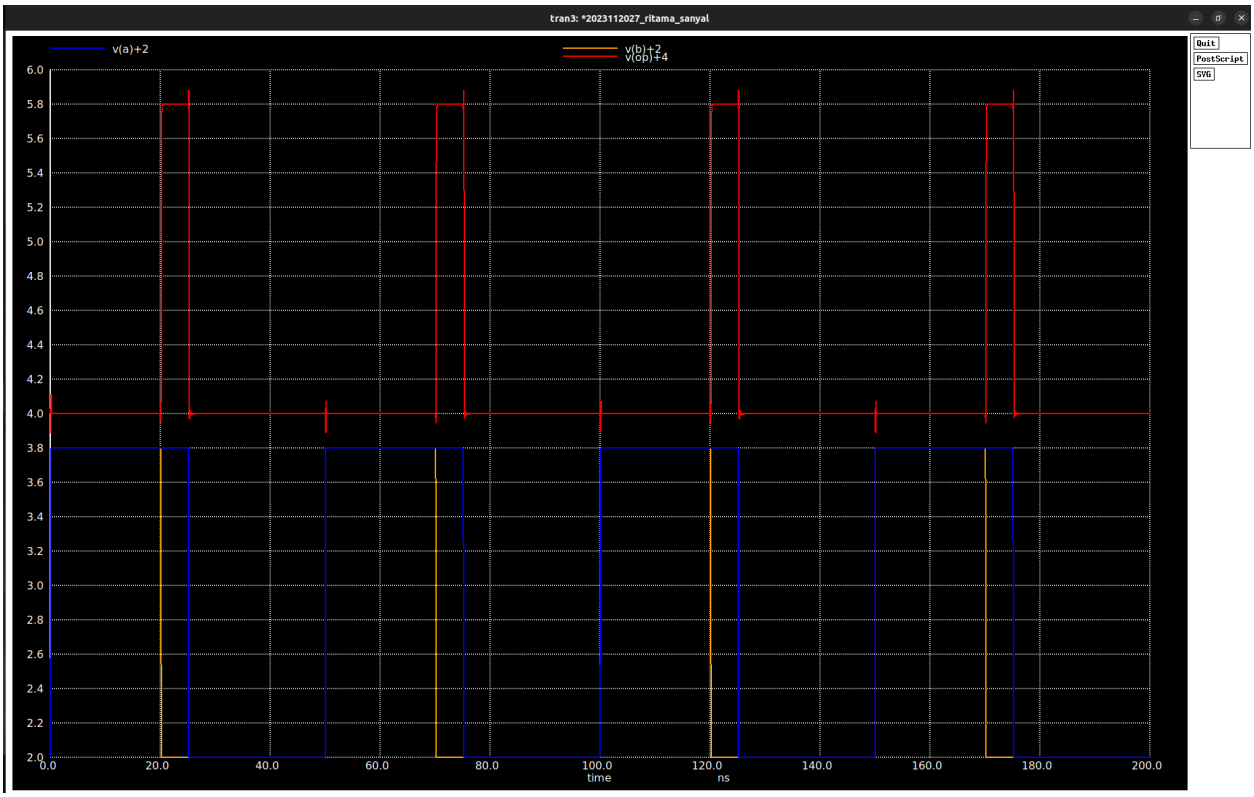
- INVERTER


vdd!
in
op
gnd!

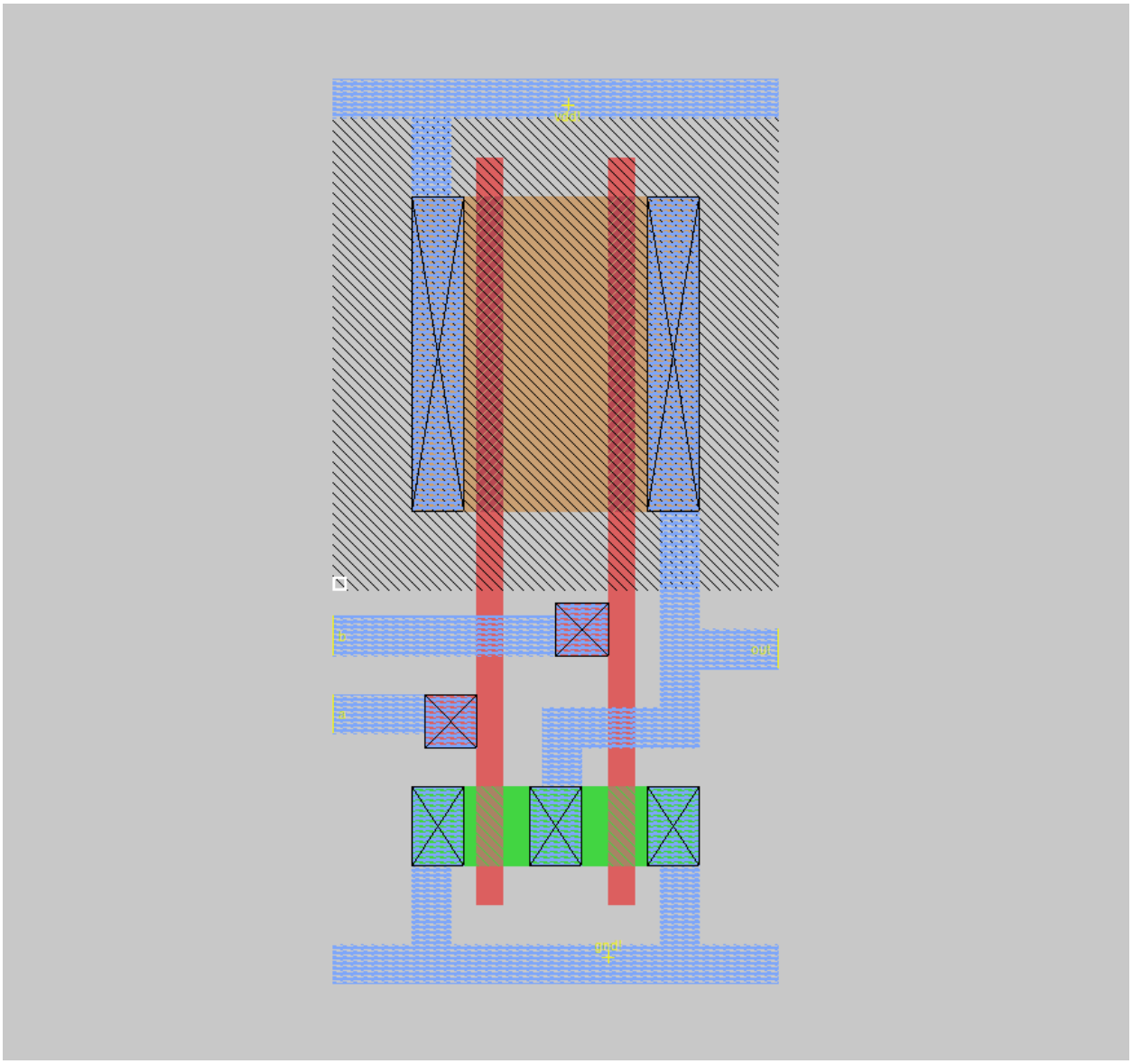

tran2: * ritama_2023112027
V
v(op)
v(in)
Quit
PostScript
SVG
1.9
1.8
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
time
ns

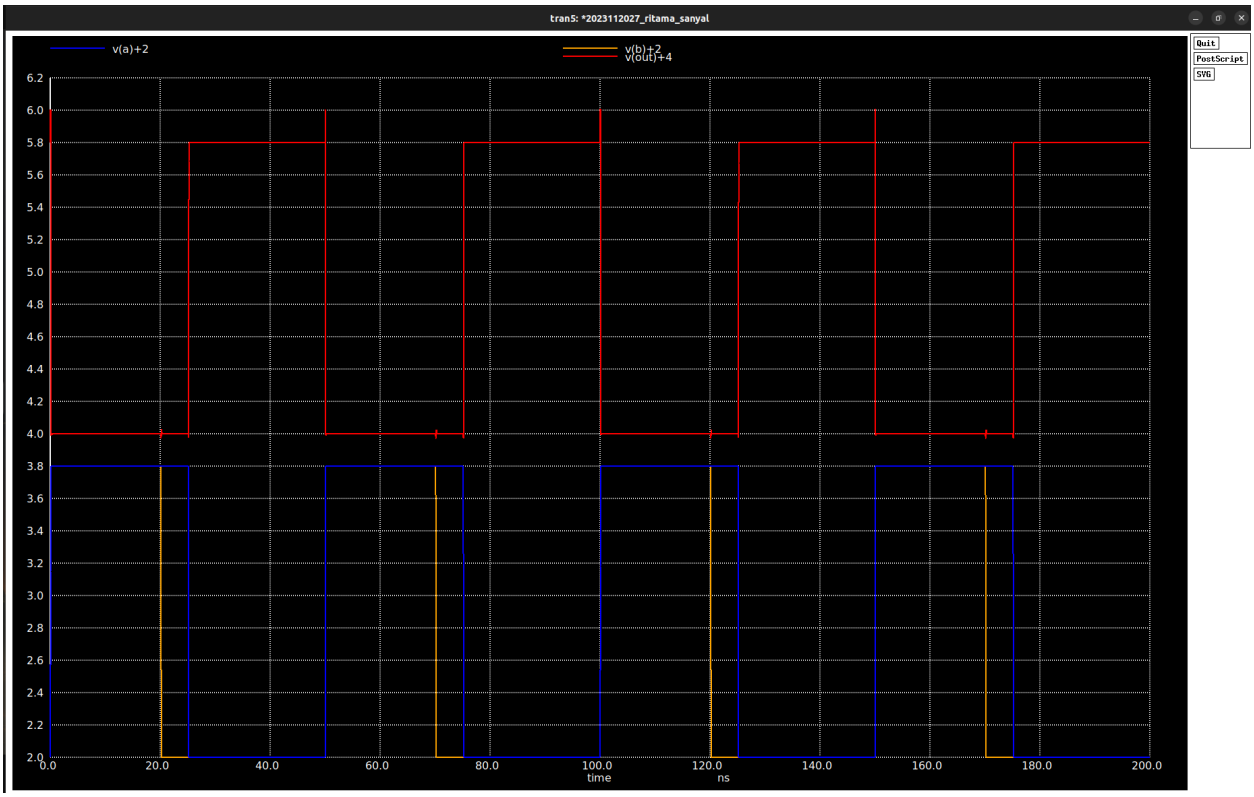
- XOR


vdd
gnd
in
a
q

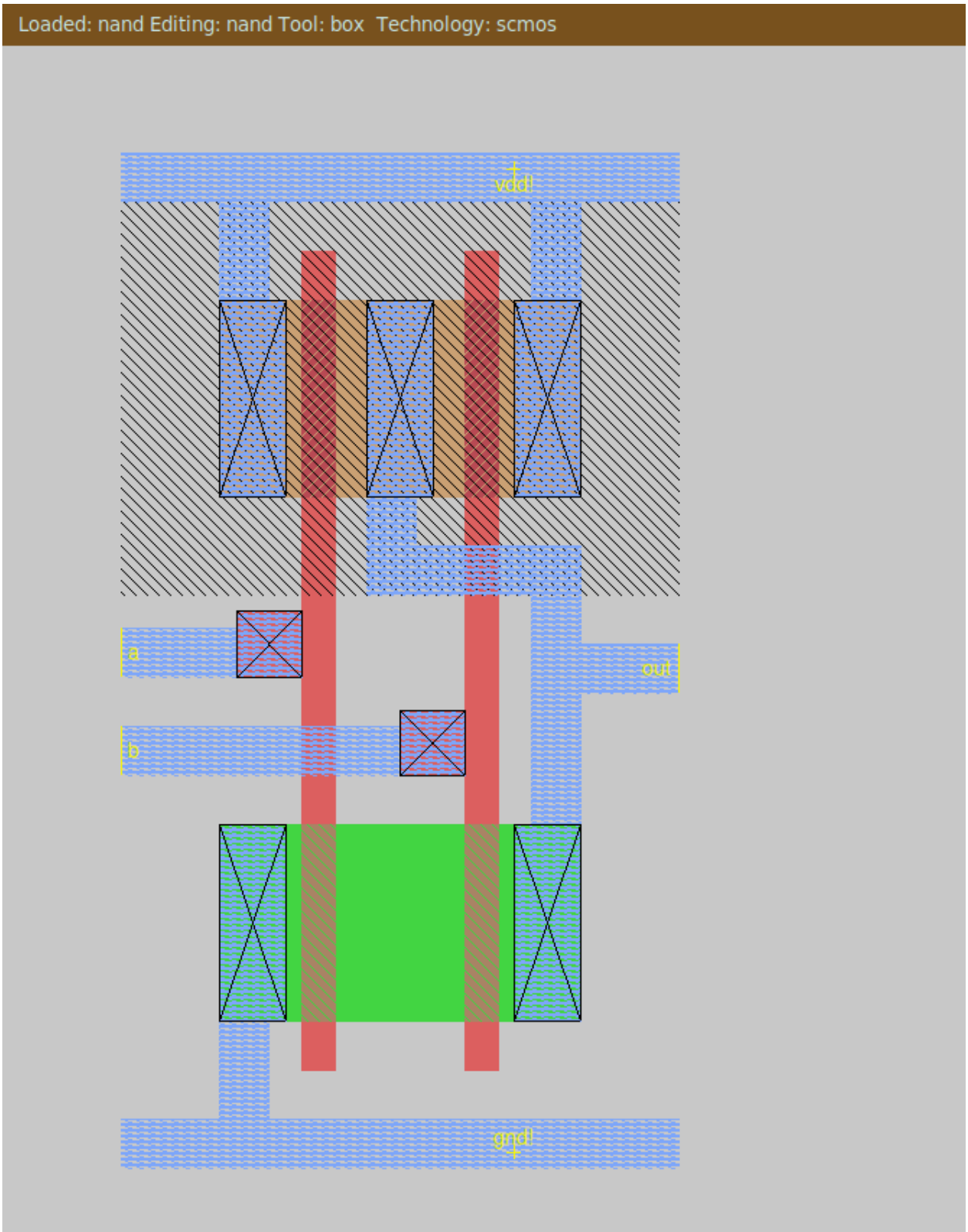

tran3: *2023112027_ritama_sanyal
v(a)+2
v(b)+2
v(op)+4
Quit
PostScript
SVG
6.0
5.8
5.6
5.4
5.2
5.0
4.8
4.6
4.4
4.2
4.0
3.8
3.6
3.4
3.2
3.0
2.8
2.6
2.4
2.2
2.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
time
ns

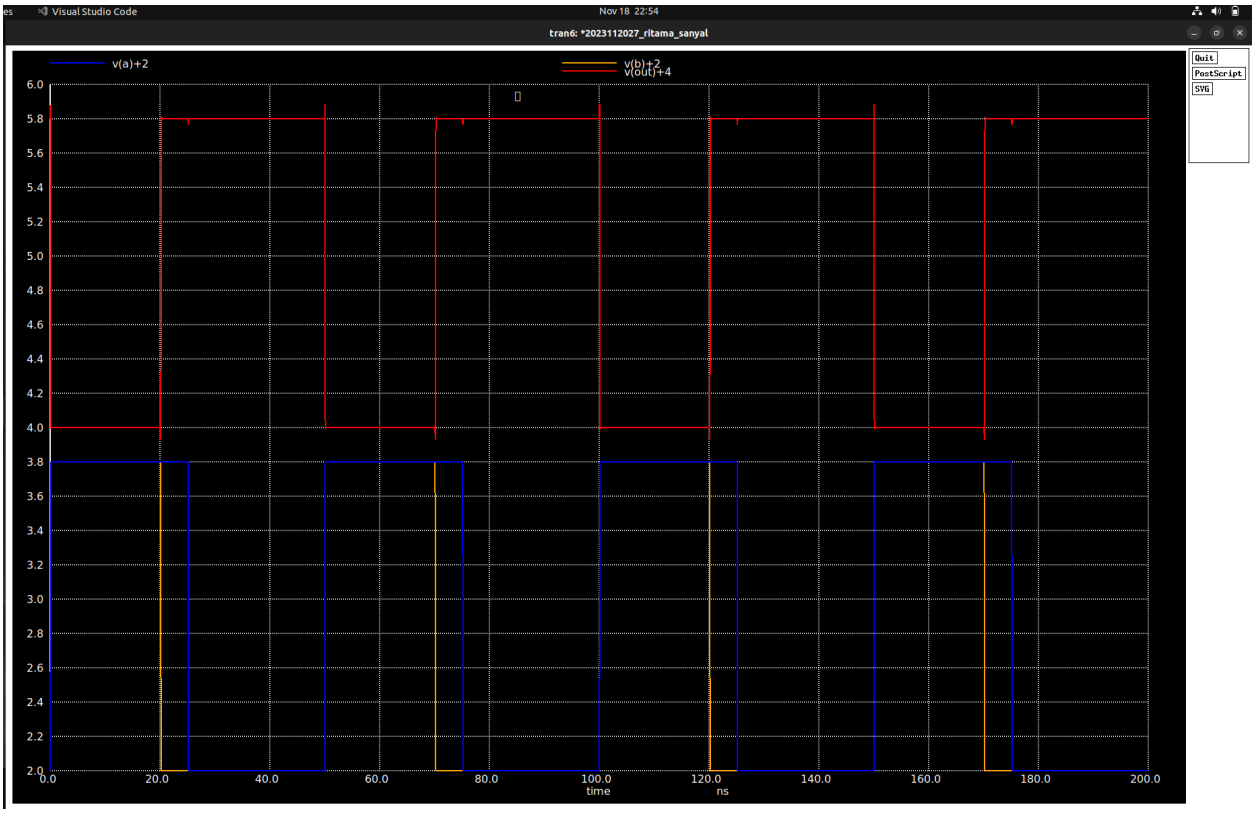
- NOR


vdd!
b
a
out
gnd!

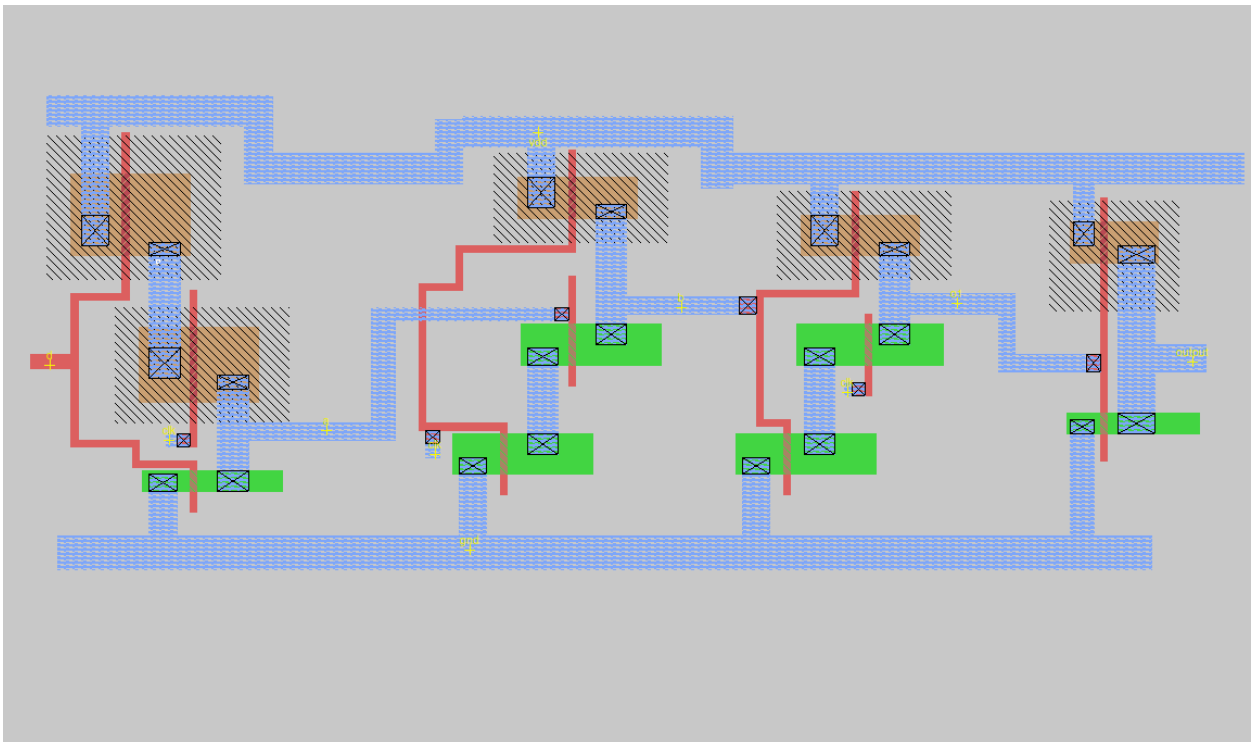

tran5: *2023112027_ritama_sanyal
v(a)+2
v(b)+2
v(out)+4
Quit
PostScript
SVG
6.2
6.0
5.8
5.6
5.4
5.2
5.0
4.8
4.6
4.4
4.2
4.0
3.8
3.6
3.4
3.2
3.0
2.8
2.6
2.4
2.2
2.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
time
ns

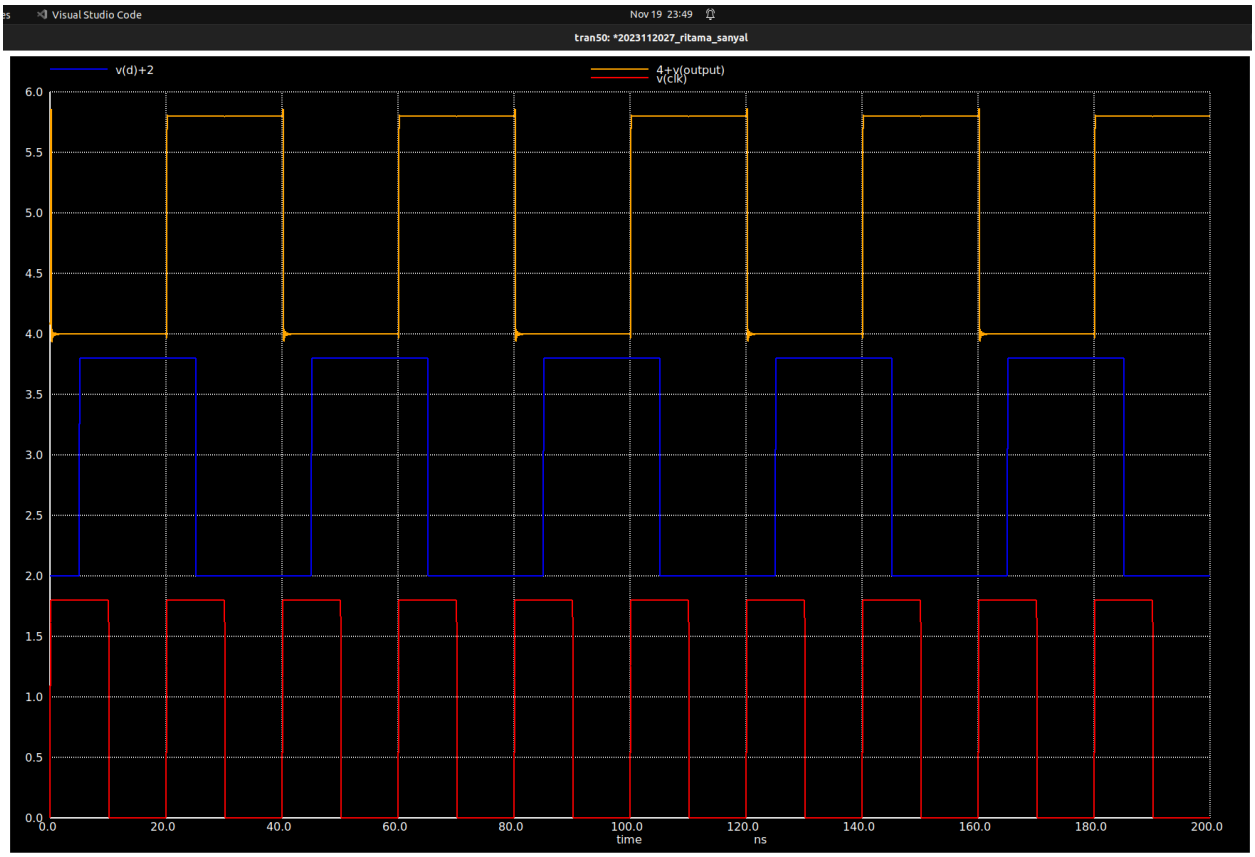
- NAND


Loaded: nand Editing: nand Tool: box Technology: scmos
vdd!
a
out
b
gnd!

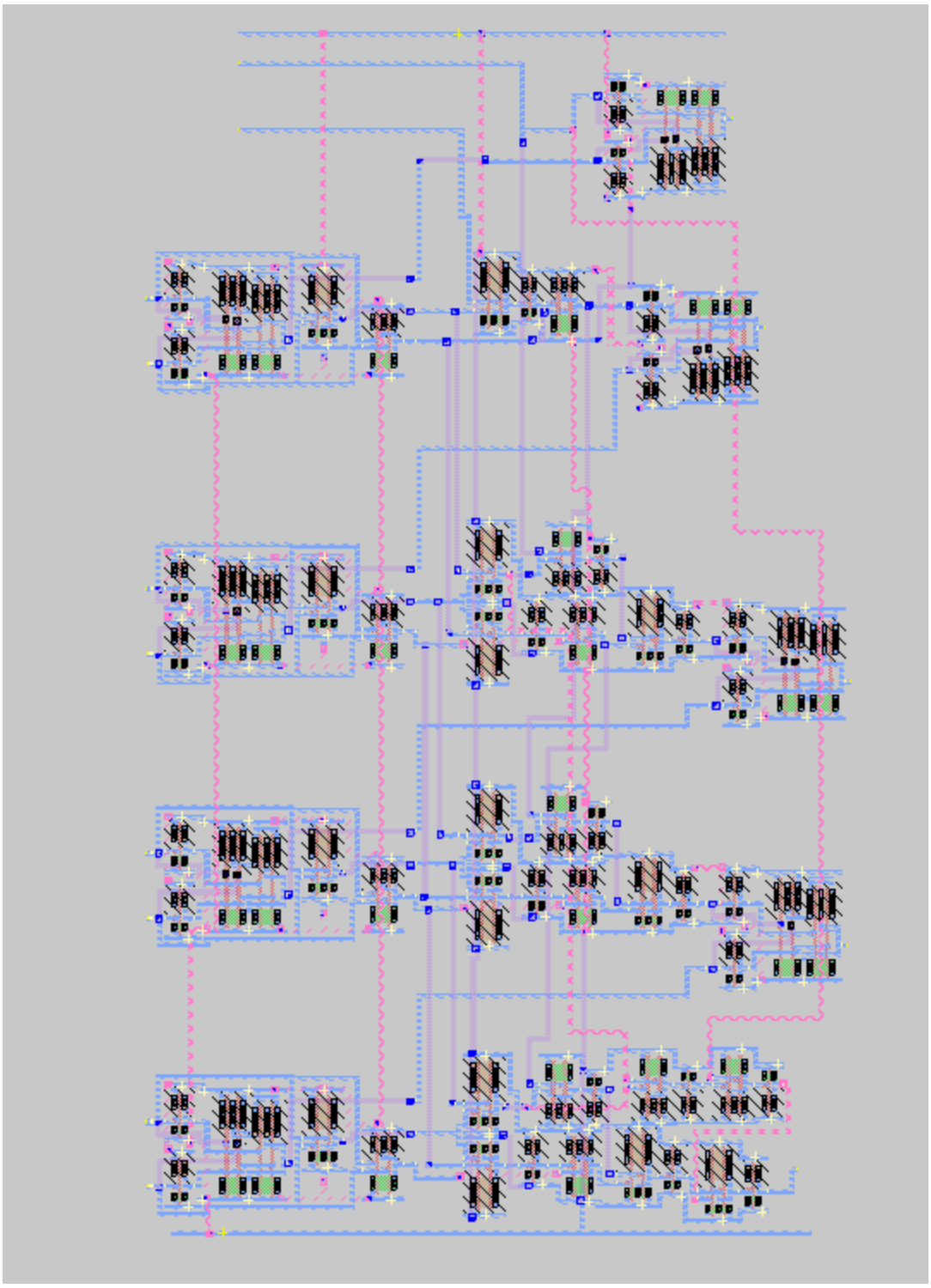

Visual Studio Code
Nov 18 22:54
tran6: *2023112027_ritama_sanyal
v(a)+2
v(b)+2
v(out)+4
Quit
PostScript
SVG
6.0
5.8
5.6
5.4
5.2
5.0
4.8
4.6
4.4
4.2
4.0
3.8
3.6
3.4
3.2
3.0
2.8
2.6
2.4
2.2
2.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
time
ns

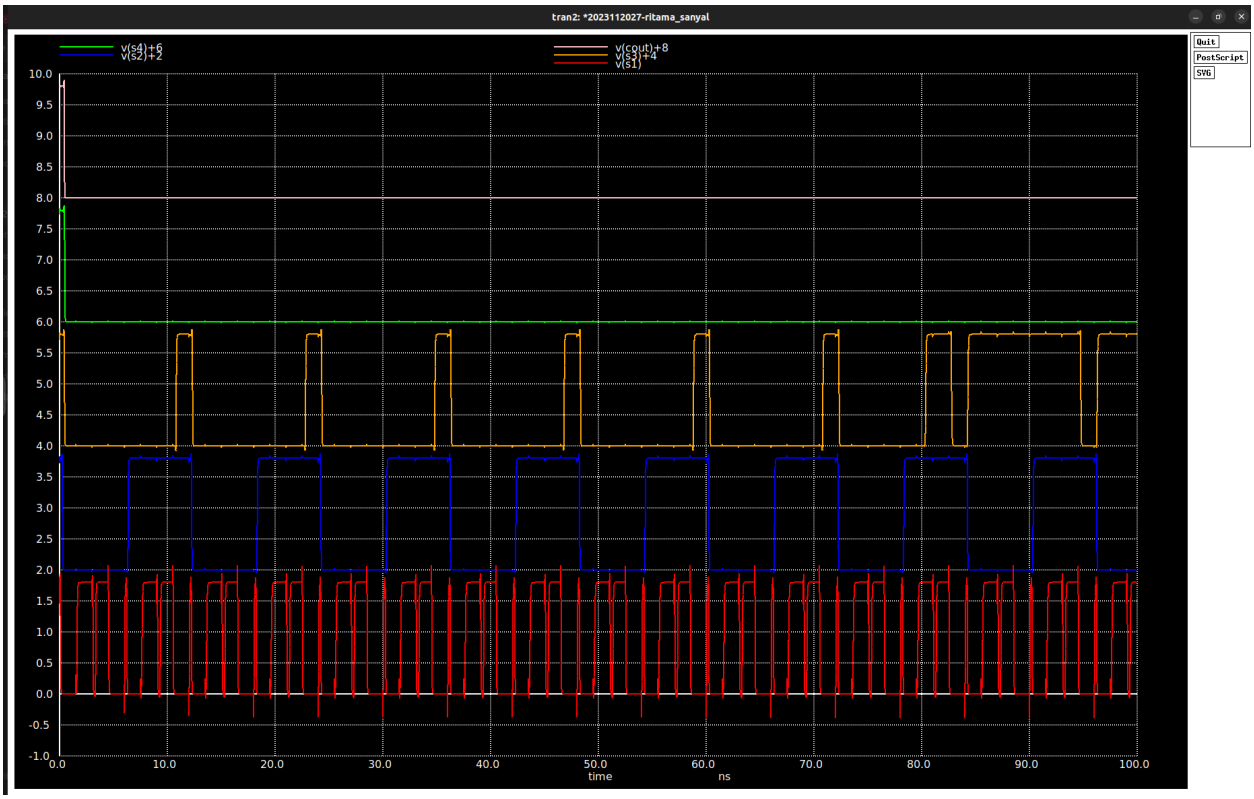
- TSPC

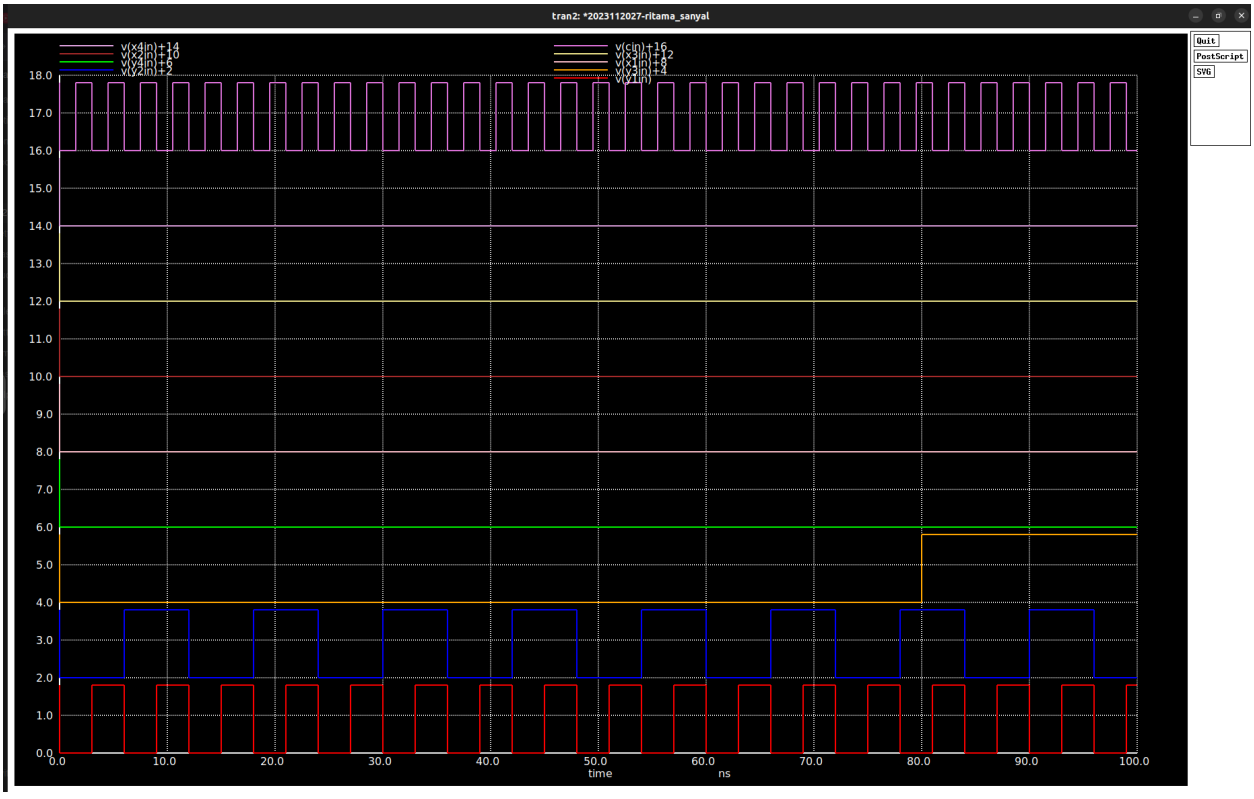

vdd
gnd
output


Visual Studio Code
Nov 19 23:49
tran50: *2023112027_ritama_sanyal
v(d)+2
4+v(output)
v(clk)
6.0
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
time
ns

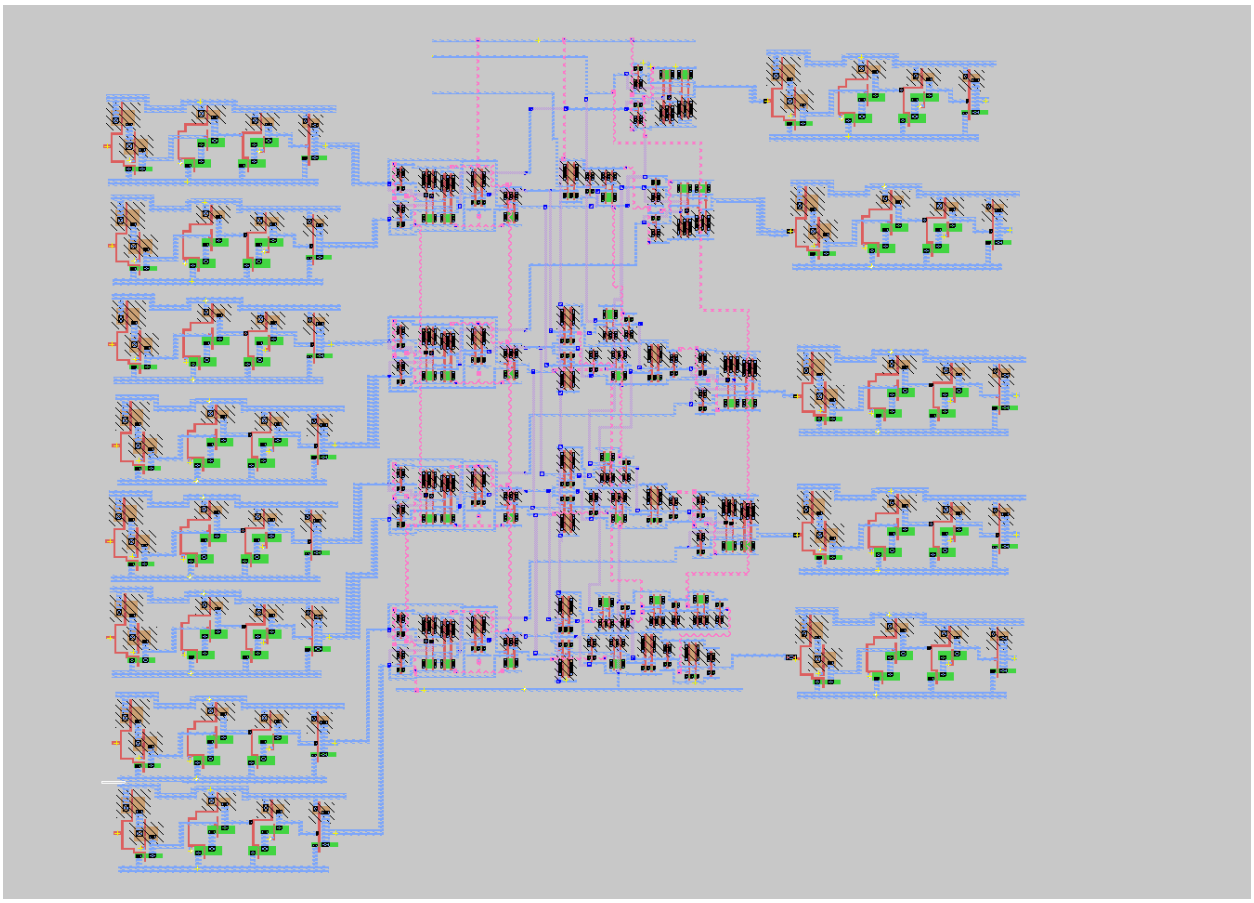
- ADDER

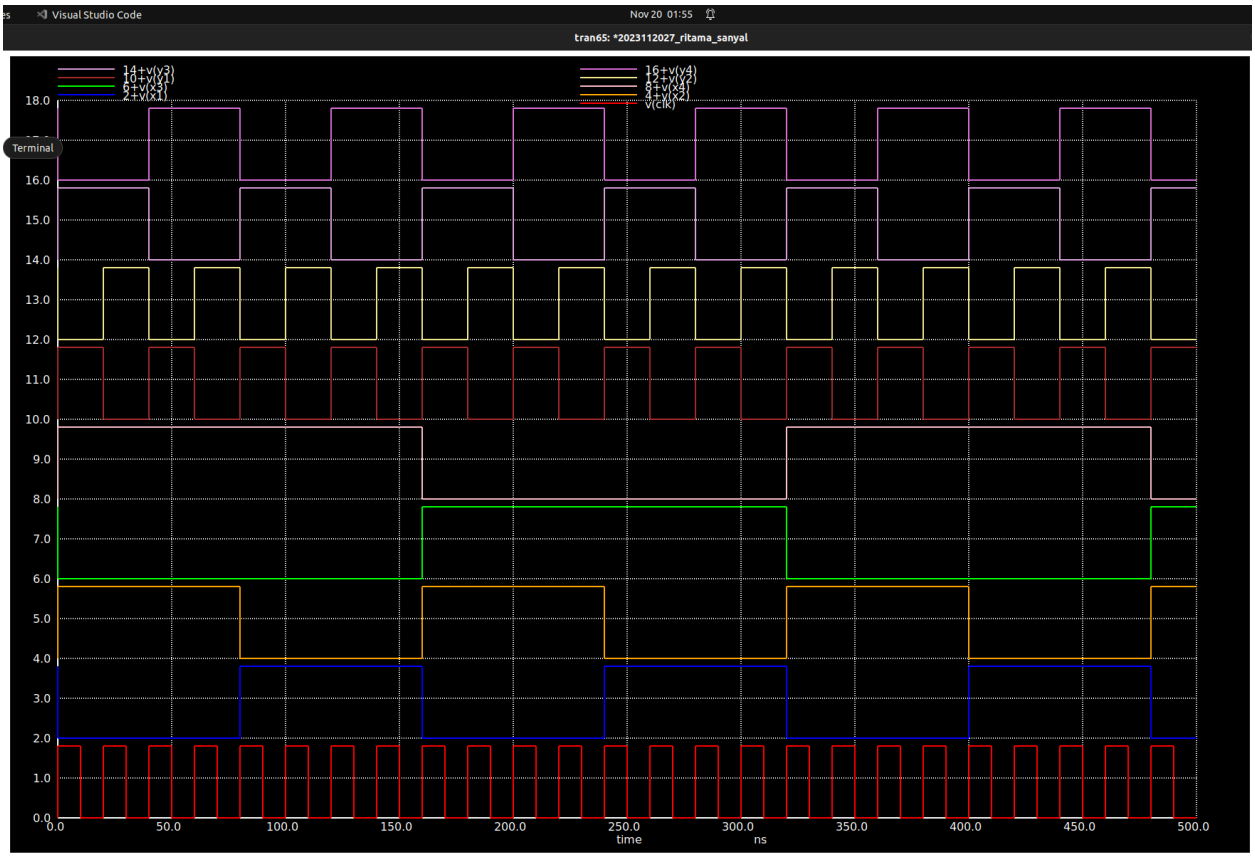


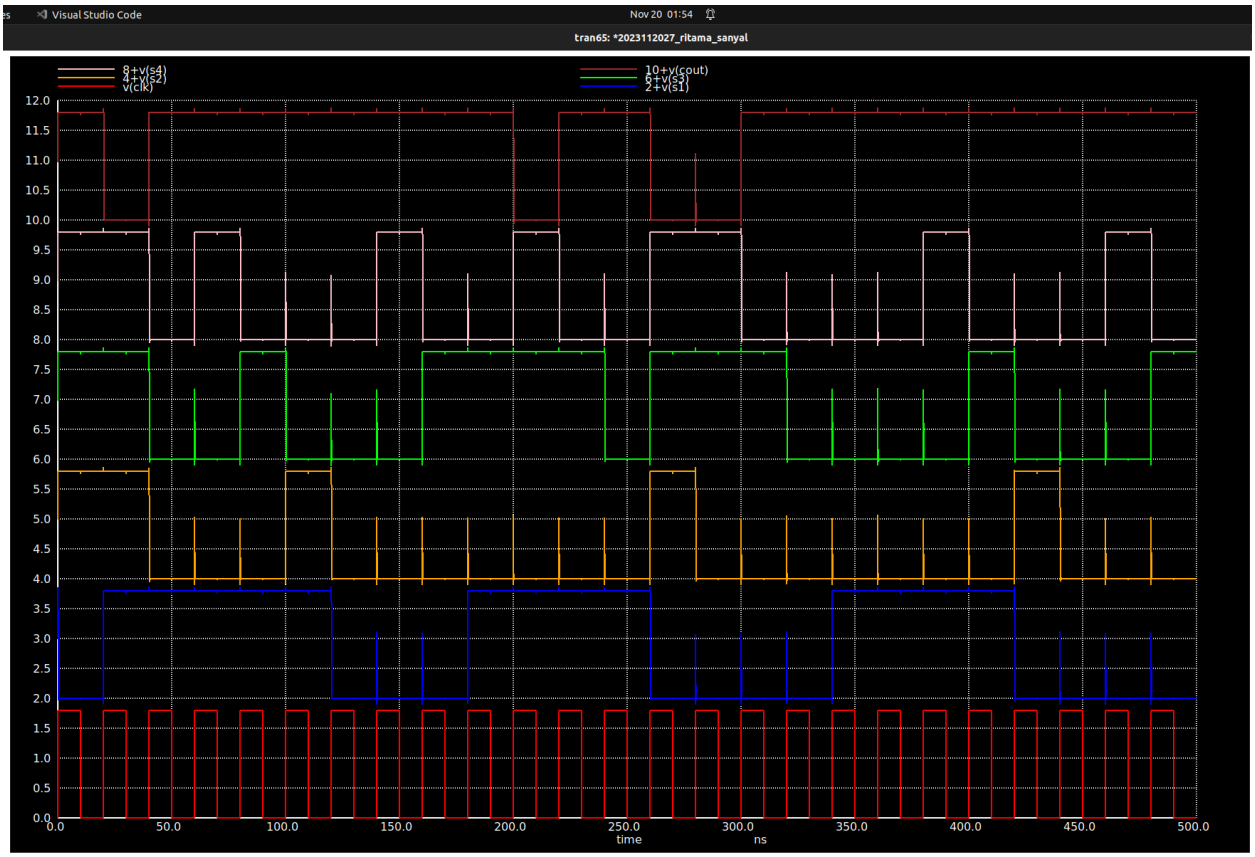




- FULL CIRCUIT

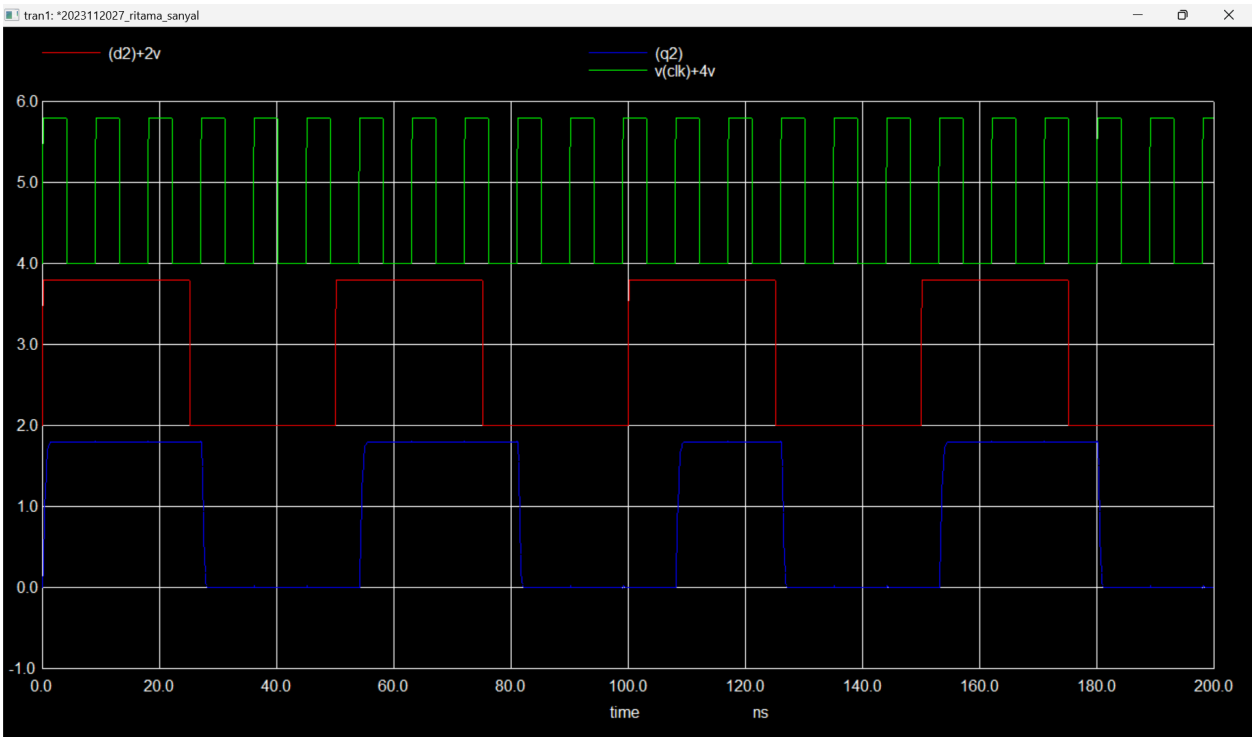



Visual Studio Code
Nov 20 01:55
tran65: *2023112027_ritama_sanyal
Terminal
14+v(y3)
10+v(y1)
6+v(x3)
2+v(x1)
16+v(y4)
12+v(y2)
8+v(x4)
4+v(x2)
v(clk)
18.0
16.0
15.0
14.0
13.0
12.0
11.0
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
time
ns

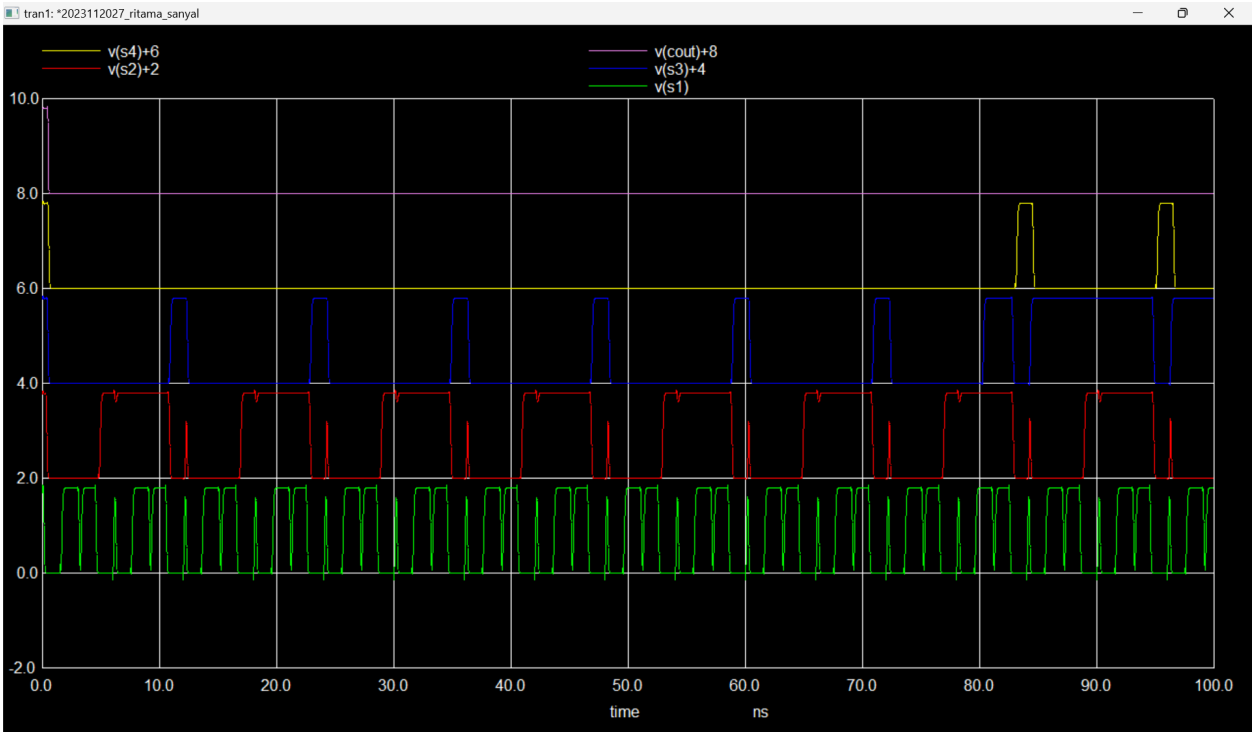


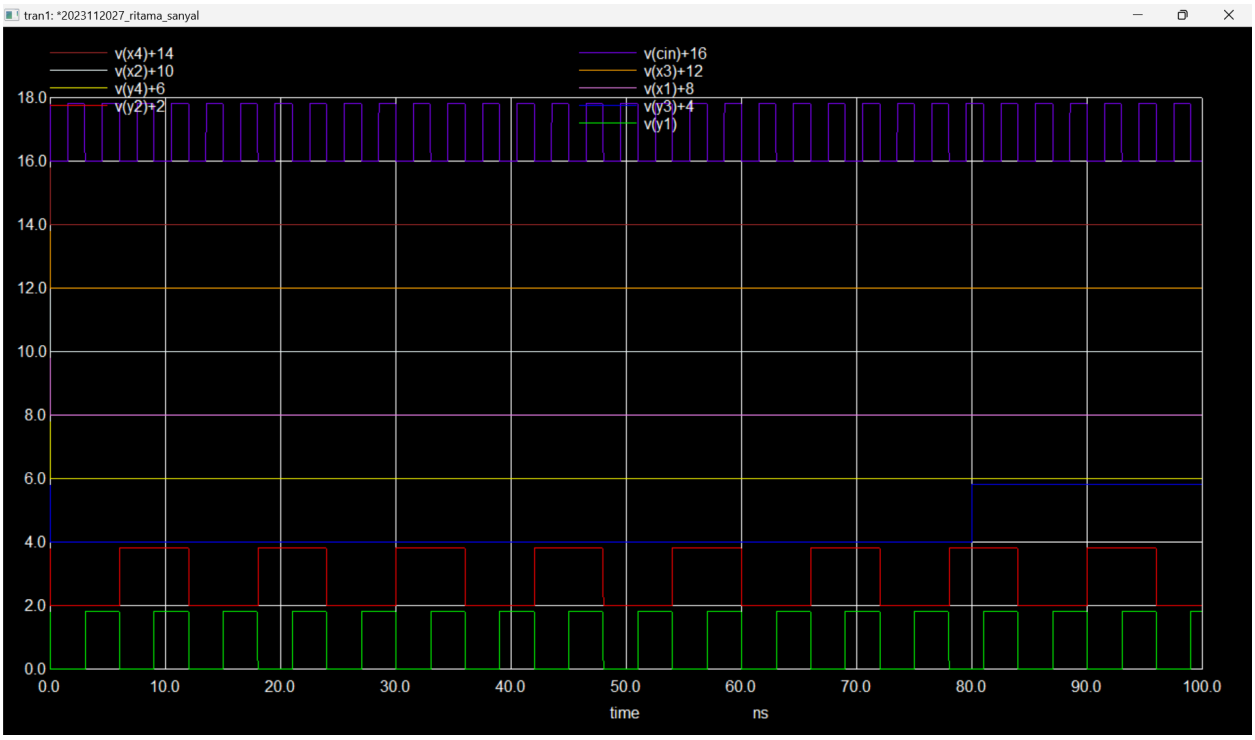
NGSPICE

- TSPC


tran1: *2023112027_ritama_sanyal
(d2)+2v
(q2)
v(clk)+4v
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
time
ns

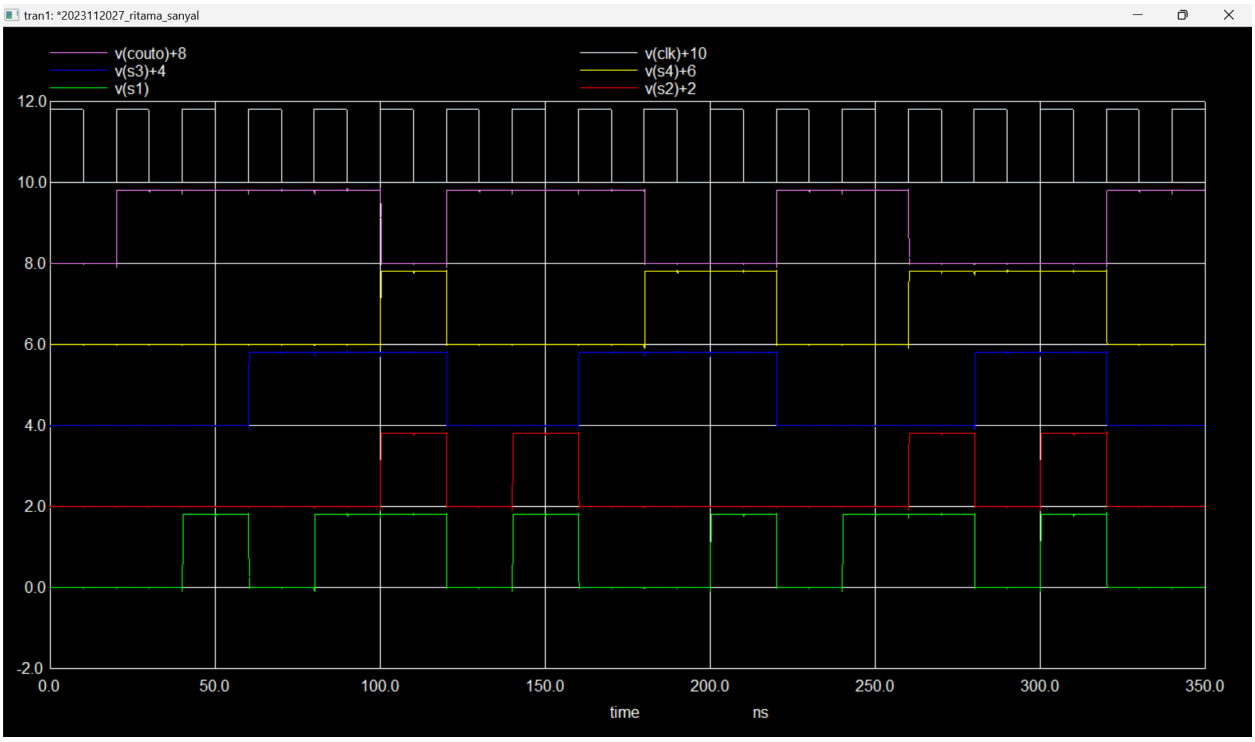
- ADDER

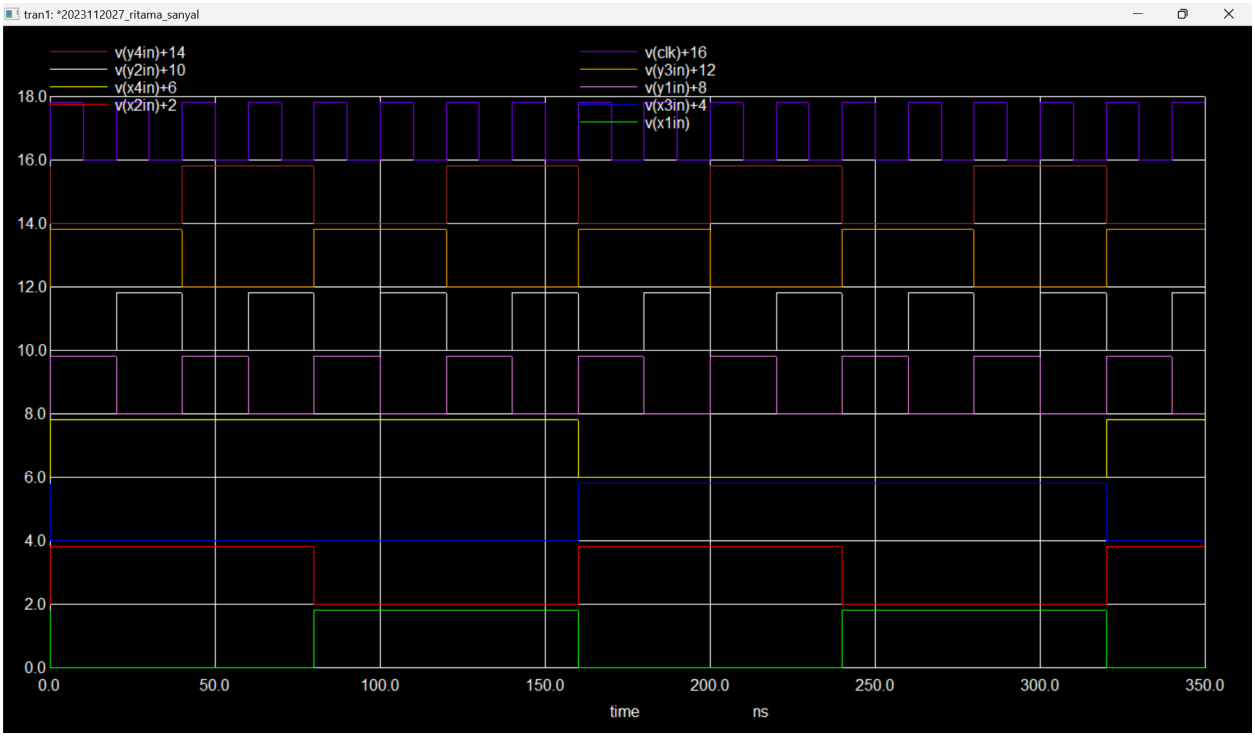

tran1: *2023112027_ritama_sanyal
v(s4)+6
v(s2)+2
v(cout)+8
v(s3)+4
v(s1)
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
time
ns




```
tpdr1                =  7.718883e-08 targ=  8.320483e-08 trig=  6.016000e-09
tpdf1                =  5.266701e-10 targ=  5.306701e-10 trig=  4.000000e-12
tpd1                 =  3.88578e-08
```

- FINAL CIRCUIT






```
  Measurements for Transient Analysis

tpdr1                =   2.010425e-08 targ=   2.010925e-08 trig=   5.000000e-12
tpdf1                =   8.015643e-08 targ=   1.001714e-07 trig=   2.001500e-08
tpd1                 =   5.01303e-08
```