1. 1. The five classic components of a computer are: (____).
   A: Qinput, Qoutput, Qmemory, Qstorage, Qcontrol, Qdatapath, QCPU, QBUS
   A: Q①③②⑦⑧ B: Q①②③⑦⑧ C: Q①③⑥④⑤ D: Q①②③④⑥

2. For a virtual memory with TLB, which of following will be run first during memory access? (____)
   A: test dirty bit   B: test cache hit
   C: test TLB hit   D: testphysical memory hit

3. In x86 real mode, according to the following memory data,the entry address of INT 21H should be (____).
   0000 0070 AD 06 14 04 00 F0 37 05 14 02F1 00 05 00
   0000 0080 72 10 A7 00 7C 10 A7 00 4F 03 80 058A 03 80 05
   A: 00A7 107C   B: 7C16 A700   C: A790 7C10   D: 107C 00A7

4. A floppy disk, double sides, 80 tracks, 18 sectors/track,512B per sector. So the Disk capacity is (____).
   A: 360 KB   B: 2.0MB   C: 1.44 MB   D: 1.68MB

5. MIPS Instruction: Beq $4,$t1,abel, Addressm?sr,ode is (____).
   A: Register addressing,   B: PC-relativeaddressing.
   C: Pseudodirect addressing. D: Immediataddressng.

6. Consider the multi-cycle implementation at the semester.Which of the following control lines is a "don't care" whileexecuting a BEQ instruction? (____)
   A: RegDst B: ALUop C: PCSource D: RegWrite

7. (____)is the best way for a keyboard to communicate witthe processor.
   A: Polling   B: DMA   C: Synchronous D: Interrupt

8. ASCII code of 'A' is (____).
   A: 97   B: 65   C: 41   D: 41

9. For 8-bit integers(2's complement) calculation, the (____)will both Overflow(OF=1) and Carry Out(CF=0).
   A: 0x12 + 0x78   B: 0x12 +0x34   C: 0x52 + 0x6F   D: 0x80 + 0x80

10. In MIPS, the register (____) is saved by the routine makinga procedure call. It is called a (____) register.
    A: $s, callee-saved   B: $t,caller-saved
    C: $t, callee-saved   D: $s,caller-saved

11. (____) is An occurrence in which the proper instructioncannot execute in the proper clock cycle because the instruction that wasfetched is not the one that is needed, that is, the flow of instructionaddresses is not what the pipeline expected.
    A: resource hazard   B: structuralhazard
    C: control hazard   D: datahazard

12. The 16-bit biased notation(偏码) representation of -1 is(____).
    A: 0x0001   B: 0x8080   C: 0x7FFF   D: 0x8001

13. According to the IEEE754 double precision, (____) is ==
    A: 0x7F80_0000_0000_0000   B: 0x7FFF_FFFF_FFFF_FFFF
    C: 0x7FF0_0000_0000_0000   D: 0x7FFF_0000_0000_0000

14. The sequence of MIPS instructions is equivalent of Cstatment (____).
    Sll a1,r1,$r5
    Bne a1,zero, Label
    A: If(r5 < r1) goto Label   B: If(r0 >r1) goto Label
    C: If(r0 >= r1) goto Label   D: If(r0 < r1) goto Label

15. (____) is A cache that has a fixed number of locations (atleast two) where each block can be placed.
    A: block-associative cache   B: fullyassociative cache
    C: set-associative cache   D: direct-mappedcache

16. Today's computers are built on 2 key principles: (____).
    ①Make the common case fast
    ②Instruction are represented as numbers.
    ③Every instruction can be conditionally executed.
    ④Programs can be stored in memory to be read or written justlike numbers.
    A: ①④   B: ①②   C: ①③   D: ②④

17. Consider a virtual memory system with 32-bit virtual byteaddress, 4KB/page, 64 bits each entry. The physical memory is 1024MB. Then, thetotal size of page table needs (____).
    A: 4MB   B: 32MB   C: about 32MB   D: 16MB

18. Memory (____) needs be refreshed periodically.
    A: EPROM   B: FLASH   C: SRAM   D: DRAM

19. There are two different conventions for ordering the byteswithin a word, Little Endian and Big Endian. In Little Endian, the byte orderfor data 0x12345678 in memory is(HEX):
    A: 87,65,43,21   B: 21,43,65,87   C: 78,56,34,12   D: 12,34,56,78

20. (____) is a cache miss caused by the first access to ablock that has never been in the cache.
    A: compulsory miss B: conflictmiss C: capacity miss D: collisionmiss

简答题 (40 分)

题81 □上传 删除平台/你的答案

2. II.1(5%), Show the IEEE754 binaryrepresentation for the floating-point number –12.34em in single precision.

                        ②=_____

简答题 (5 分)

题91 □上传 删除平台/你的答案

3. 3.2(5%), What is the average time toread or write a 512-byte sector for a typical disk rotating at 10000 RPM? Theaverage seek time is 12ms, the transfer rate is 5 MB/sec, and the controlleroverhead is 2ms. Assume the disk is idle so that there is no waiting time.

简答题 (5 分)

题91 □上传 删除平台/你的答案

4. II.3(5%), The C to Assemble: Convert the C function betwein MIPS or x86 assembly language. Make sure that your assembly language codecould be called from a standard C program.
   int gcd(char *p){ int i=–1; do{
        p[++i]=read_char(); #tsyscall / int 21h
        if(p[i]==13)p[i]=0;
        }while(p[i]!=0);
        return i; }

简答题 (5 分)

题91 □上传 删除平台/你的答案

5. II.1, (5%),The system has aXGB main memory and a cache with 4K blocks and 2-word blocks. 1word = 4Byte.
   1.(5%),Supposethe cache configured as fully-associative.
   1)Howmany bits for TAG:

   2)Howmany total bytes are required for the cache:

   2.(5%),Supposethe cache configured as 4-way set-associative.
   1)Howmany bits for TAG:

   2)Howmany total bytes are required for this cache:

   3.(5%),Supposethe cache configured as direct-mapped. What block number does byte address 0xFACE2BED map to?
   1)Tag:

   2)Index:

   3)offetch block:

简答题 (15 分)

题91 □上传 删除平台/你的答案

6. III.2, (5%),Consider avirtual memory system with the following properties:
   * 32-bitvirtual byte address
   * 16 KBpage
   * 1GBphysical memory(byte-addressing)
   Whatis the total size of the page table for each process on this processor,assuming that the valid, protection, dirty, and use bits take a total of 4 bitsand that all the virtual pages are in use? (Assume that disk addresses are notstored in the page table.)

简答题 (5 分)

题91 □上传 删除平台/你的答案

7. IV, (15%),Design: Multicycle CPU implementation
   Wewish to add the instruction Jalr tothe multicycle datapath. Add any necessary datapath and control signals to theFigure. The instruction is described as:
   Jalr   rd,rs
   Toexecute:
   $rd = PC;
   PC = $rs;

   1.(3%) Design theinstruction format in binary number;
   2.(4%) Design datapath: To add any necessaryelements and new signals and explain how to modify the data path; In thefollowing diagram Draw compatible Modification

   3.(8%) Complete this finite state machine diagram for thisinstruction. Draw State Machine Diagram

IV. (15%)Design: Multicycle CPU implementation
We wish to add the instruction Jalr to the multicycle datapath. Add any
necessary datapath and control signals to the Figure. The instruction is
described as:
     Jalr $rd, $rs
To execute:
     $rd = PC;
     PC = $rs;

1. (3%) Design the instruction format in binary number:

3	1	3	0	2	9	2	8	2	7	2	6	2	5	2	4	2	3	2	2	2	1	2	0	1	9	1	8	1	7	1	6	1	5	1	4	1	3	1	2	1	1	1	0	9	8	7	6	5	4	3	2	1	0

2. (4%) design datapath: To add any necessary elements and new signals and
explain how to modify the data path; In the following diagram Draw compatible
Modification

4. (8%) Complete this finite state machine diagram for this instruction. Be
sure to include any new control signals you may have added. For each state,
fill the output signal values in the following table(only this instruction
state).

1-	2-	3-

简答题 (15 分)

题91 □上传 删除平台/你的答案