1. 1. The five classic components of a computer are: [].
()rps. (ovps. ()menoy, ()mrays, (ovms. ()majoris, ()cPs. ()866 A: 0.08008 B: 0.00008 C: 0.00088 D: 0.00088
For a while memory with TLB, which of fillinging will be un that during memory access? () X. Weld day bit
In Add that mode, according to the following memory datable entry address of RPT 21th should be (). ODD 000714-00 do it 40 DA AFF OR FAST did it 400114-00 dod 0. ODD 00000000 71 to 47 OF 07 14 AFF OWN-000 dods 400 dod 0. AL ODAN-19TIC BI TOTAN-000 CC APOSITION D. 1007-00047
0000:0000 72 10 AT 00 TC 10 AT 00-4F 03 80 000A 03 00 05 A: 00AT:NETC 8: 7CT0:AT00 C: AT00:TCT0 D: NETC:00AT
A. Afoppy disk, double sides, 80 tracks, 16 sectors/freds_SCEE per sector-So the Disk capacity is
S, MPS intraction Deg All, 15, Label, Addressing mode in [].
Register addressing. B: PC-elaboraddressing. Pseudothext addressing. D: Immediateaddressing.
 Consider the multi-cycle implementation at the sementer-lithich of the following control lines is a "start card" whilesexculing a BIOQ instruction? (
[-] is the best way for a keyboard to communicate within processor. A: Polling B: DMA C: Synchronous D: Interrupt
8. ASCROOM: 6TW 8:
Por 6-bit Hopens/25 complement) calculation, the (bett bett Overflow(DF+1) and Carry DU(DF+0), X 0x22 + 0x78 (ii) 0x22 + 0x64 (iii) 0x24 + 0x64 (iii) 0x84 + 0x80
10. In MATS, the register is sweed by the readine multings procedure cell. It is called a register. A. So, collectured is (quite-calculated
 In Air occurrence in which the proper instructions densate in the proper double cycle beauser the instruction that washfulfed a not the cost that a revelled, that it, the five of instructional terrence is not what the pipeline expected.
C: corted hazard D: datahazard
12, The filed bload nation(\$840) representation of -1 in(), A: 0x0004 B: 0x0000 C: 0x70FF D: 0x0004
15. Autoriting to the EEE/164 dustine procisions () in ere A
14. The sequence of MIPS instructions is equivalent of Cristment (). Sit at /1, 50
Bre et_proc_label A: Infr0 <-rif_pop Laber B: Infr0 <-rif_pop Laber C: Infr0 <-rif_pop Laber D: Infr0 <-rif_pop Laber

16. Totaly's computers are but on 2 key principles: ().
16. Today's computers are built on 2 key principies: (
(SPrograms can be stated in remove to be reaction written justifier numbers. A: ((i)) B: ((i)) C: ((i)) C: ((i))
 Consider a virtial memory ryptom with 32-04 what lyheaddress, 4/35 page, 54 bits earliverity. The physical memory is 102465. Then, fielded size of page 1889 media []. All B. S. JOSE C. Book 15-566 D. 15866.
18. Mentory (needs be refreshed periodically. A: EFROM 8: RASH C: SRAM D: GRAM
 There are but different connections for extension the independence are not 1 life finding and the finding in 1 life finding the but carbotic right.
0x3246678 in nereny (kHEQ); A: 07,64,40,21 B: 21,43,64,87 C: 78,90,34,12 D: 52,94,94,78
 is a sold entire so caused by the first access to ablock that has never been in the cause. A: computacy note (it: confidence C: capacity nine D: califorancies
A: computary rates R: coefficients C: capacity miss D: callisionness 開西日 (40.5)
MAA STW MRATTWAND.
1. 1975. Show the IEEE/74 binary representation for the floating-point number -12.54km in single precision.
a. 1(A), a total track of the symptomic of the control of the cont
<u> </u>
MITTER (9:59)
RN: SIN MOTINGS
 ILADYSE, What is the average time toread or write a STU-byte exclur for a typical date schaling at 10000 RPMF Theoreties seek time in 12ms, the transfer rate is 5 Millions, and the controlleroverhead is 2ms. Assume the date is tide so that there is no earling time.
維質器 (5-5)
Mat_grip_min-it-leasants
4. ANNLY, his to Mexicology Companies (Annah Confidence of Mexicology on the sector) group of the sector for pure executing sequence of product (Fig. 164-5). did produced (Fig. 164-5).
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)while(pl)=0; ordun(:)
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RMS 国上的 组织工士的细胞时
ILI., (HSV)The system has a st-GR train memory and a cache with 4K biscles and 2 word biscles, twent in 48ps. INVM formation currier confinement in the New amongstille.
IL1, (192)The system has a 168 main memory and a cache with 4K blocks and 2 word blocks, twent + 48ps.
ILI., (HSV)The system has a st-GR train memory and a cache with 4K biscles and 2 word biscles, twent in 48ps. INVM formation currier confinement in the New amongstille.
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R. N. (PSI) in option to a roll in accountry and a case with 45 bits and 2 accritistic frame - dipa. 1/E/E/Committee case uniform for Mayerocoldie. 1/Everyor file for Tio.
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