Assignment 4

提交作业

截止时间 星期四，23:59 之前   **得分** 100   **提交** 一份上传文件   **文件类型** pdf

1. If the CPU only includes the adder and does not include subtracter, how would the CPU support the subtraction operation for integers?
2. For each of the following operation, please determine the CF, OF, SF, ZF, and PF in the flag register. a. 1234H + 4321H; b. 1000H+FFFFH; c. 1000H-2000H; d. F000H+F000H; e. 2000H-8000H.
3. Convert the following logical address to physical address and explain which segment each address belongs to.

   a.CS:IP = 1A00H:B000H; b. DS:DI = 1000H:2000H; c. SS:SP=2900H:3A00H.

4. Which pin of 8086 can be used for determining if an access is for the memory module?
5. Describe what is a bus cycle.
6. Assume SS=3500H, SP=0800H, if the 8086 CPU executes "PUSH AX" instruction 10 times, what are the values of SS and SP? After the 10 push instructions, what are the values of SS and SP if the CPU executes another "POP BX" instruction 6 times?
7. When the 8086 CPU is reset, registers like IP, DS, SS, and ES will be cleared (i.e, set to 0s), but the CS would be set to FFFFH. Can you determine what's the first instruction the CPU will execute every time when the CPU is reset? Can you explain the reason for such a design?
8. Assume DS=1000H，BX=0200H，SI=02H，the memory addresses of 10200H~10205H include values of 10H, 2AH, 3CH, 46H, 59H, 6BH. What would be value of AX after executing each of the following instruction?

   (1) MOV AX，0200H; (2) MOV AX，[200H]; (3) MOV AX，BX

   (4) MOV AX，3[BX]; (5) MOV AX，[BX+SI]; (6) MOV AX，2[BX+SI]