Assignment1 of EI209

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1. In Princeton architecture, programs and data are stored in a single memory.
   In Harvard architecture, programs are stored in program memory, data are stored in data memory; the two memory space interact with control unit separately.

2. RISC.

3. The data bus width would be $32 \times 8 = 256$ bit.
   The reason is that when transferring data, the CPU should acquire enough data to run fully, in order to raise the efficiency.

4. **Size**: disk > main memory > cache > register
   Access time: register > cache > main memory > disk

5. **Difference:**

   (a) **purpose**: Data bus is used to provide **a path for moving data** between system and modules.
   Address bus is used to **designate the source or destination of the data** on the data bus that the processor intends to communicate with.
   Control Bus is used to **control** each module and the use of data and address buses.

   (b) **direction**: Data bus is bidirectional: memory or I/O device $\leftrightarrow$ CPU.
   Address bus is unidirectional: only CPU $\rightarrow$ memory or I/O device.
   Control Bus is consisted of two unidirectional signals: for command signal: CPU $\rightarrow$ memory or I/O device; for state signal: memory or I/O device $\rightarrow$ CPU.

   (c) **width**: Data bus's width is the same as the width of register; it determines the data amount the processor can read or write in one memory or I/O cycle and the word of the computer.
   Address bus's width determines the memory capacity by a given CPU.

   Address bus determines the memory capacity.

6. The truth table is:

A	**B**	**F**
False	False	True
False	True	False
True	False	False
True	True	False

7. No. Because the the running time is affected by more things than the speed of executing the instruction.
   For this program, although RISC's execution time of one instruction is lower, but as it can only operate on the register, it may have more operation to fetch data between main memory and CPU, whose time cost is higher than that of CISC's operation on the main memory.

8. i,result,b.