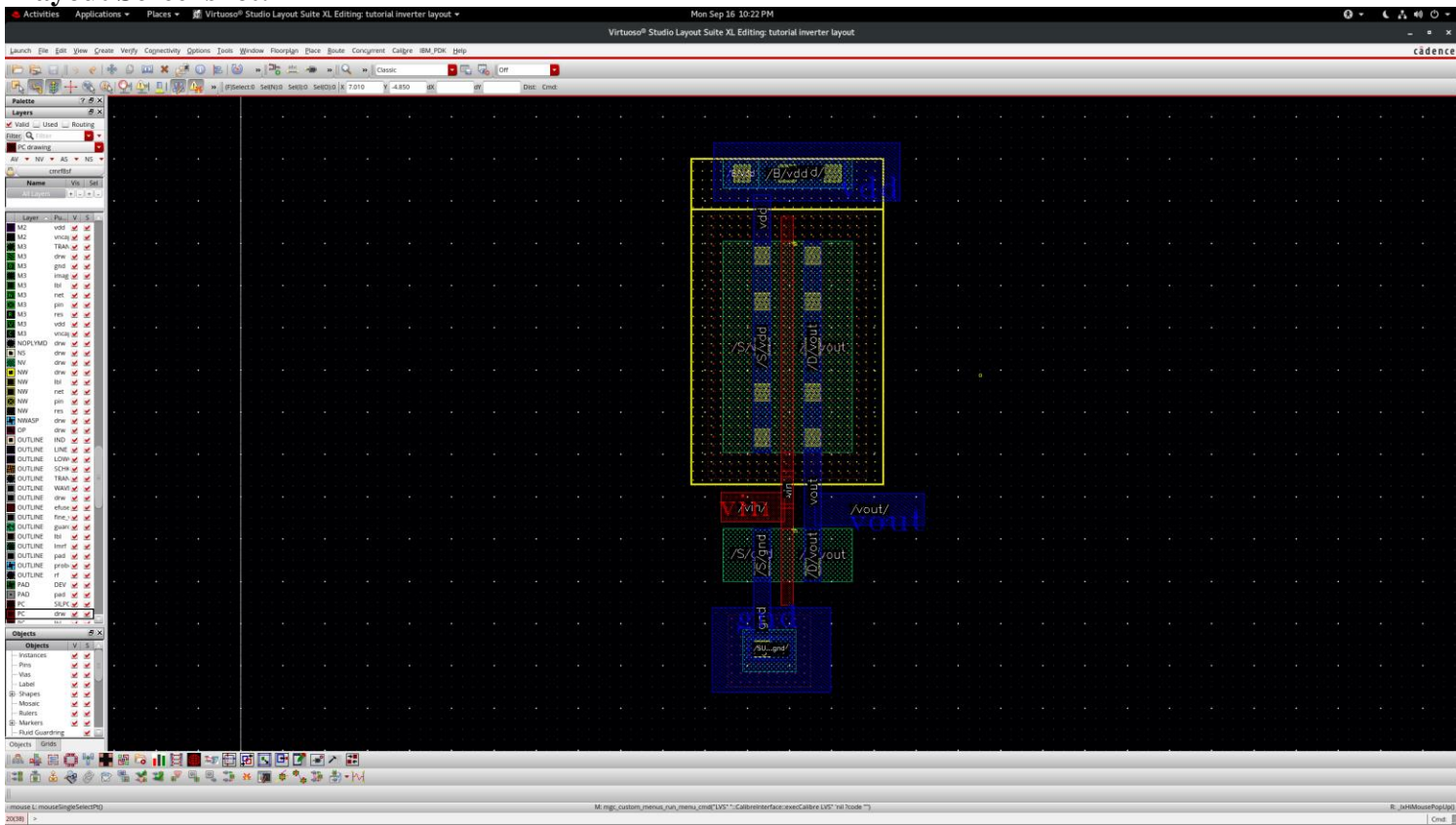


Layout Screenshot:



[illegible]

Mon Sep 16 10:24 PM
Calibre - RVE (2021.3.15.9) - vdb: inverter

File View Highlight Tools Window Setup Help

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ERC

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- ERC Paths: Nets Report

Reports

- Extraction Report
- LVS Report

File

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omatics

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Cell inverter Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

LAYOUT CELL NAME: inverter
SOURCE CELL NAME: inverter

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	4	4	
Beta:	5	5	
Instances:	1	1	NM (4 pins)
	1	0	OP (4 pins)
	1	1	P (3 pins)
	1	1	NMC (3 pins)
Total Inst:	4	3	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	4	4	
Beta:	5	5	
Instances:	1	1	nmos (2 pins)
	1	1	jump (0 pins)
Total Inst:	2	2	

* = Number of objects in layout different from number in source.

UNMATCHED AND WARNING

	Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type
Ports:	4	4	0	0	
Beta:	5	5	0	0	

LVS Report File - inverter.lvs.report

File Edit Options Windows

REPORT FILE NAME: inverter.lvs.rpt
LAYOUT NAME: /afs/umich.edu/class/eece413/FS4/students/omni/cadence/calibre/inverter.sp ('inverter')
SOURCE NAME: /afs/umich.edu/class/eece413/FS4/students/omni/cadence/calibre/inverter.sdc.net ('inverter')
HEAT FILE: /afs/umich.edu/class/eece413/FS4/students/omni/cadence/calibre/heats/heats.lvs
CREATION TIME: Mon Sep 16 10:24:54 2021
CONVERT DIRECTORY: /afs/umich.edu/class/eece413/FS4/students/omni/cadence/calibre
USER NAME: omni
ONLINE VERSION: v2021.3.15.9 Tue Jul 6 13:44:37 PDT 2021

OVERALL COMPARISON RESULTS

CELL SUMMARY

Result	Layout	Source
Correct	inverter	inverter

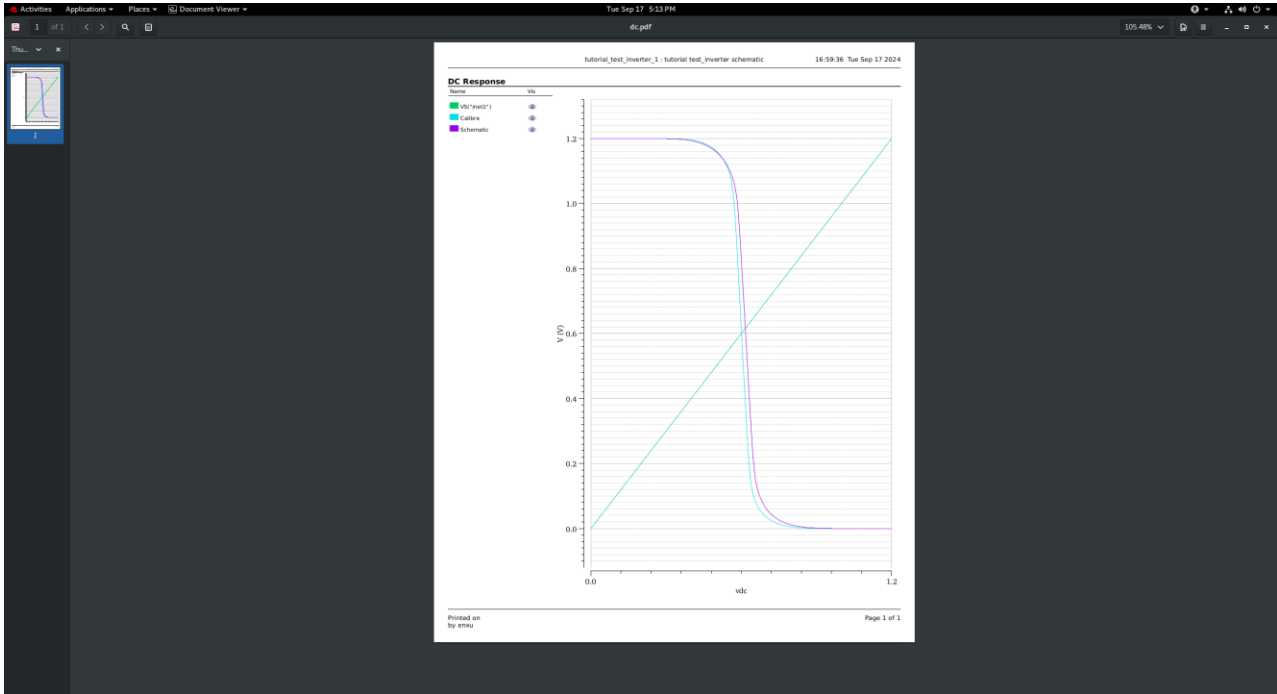
LVS PARAMETERS

LVS Setup:

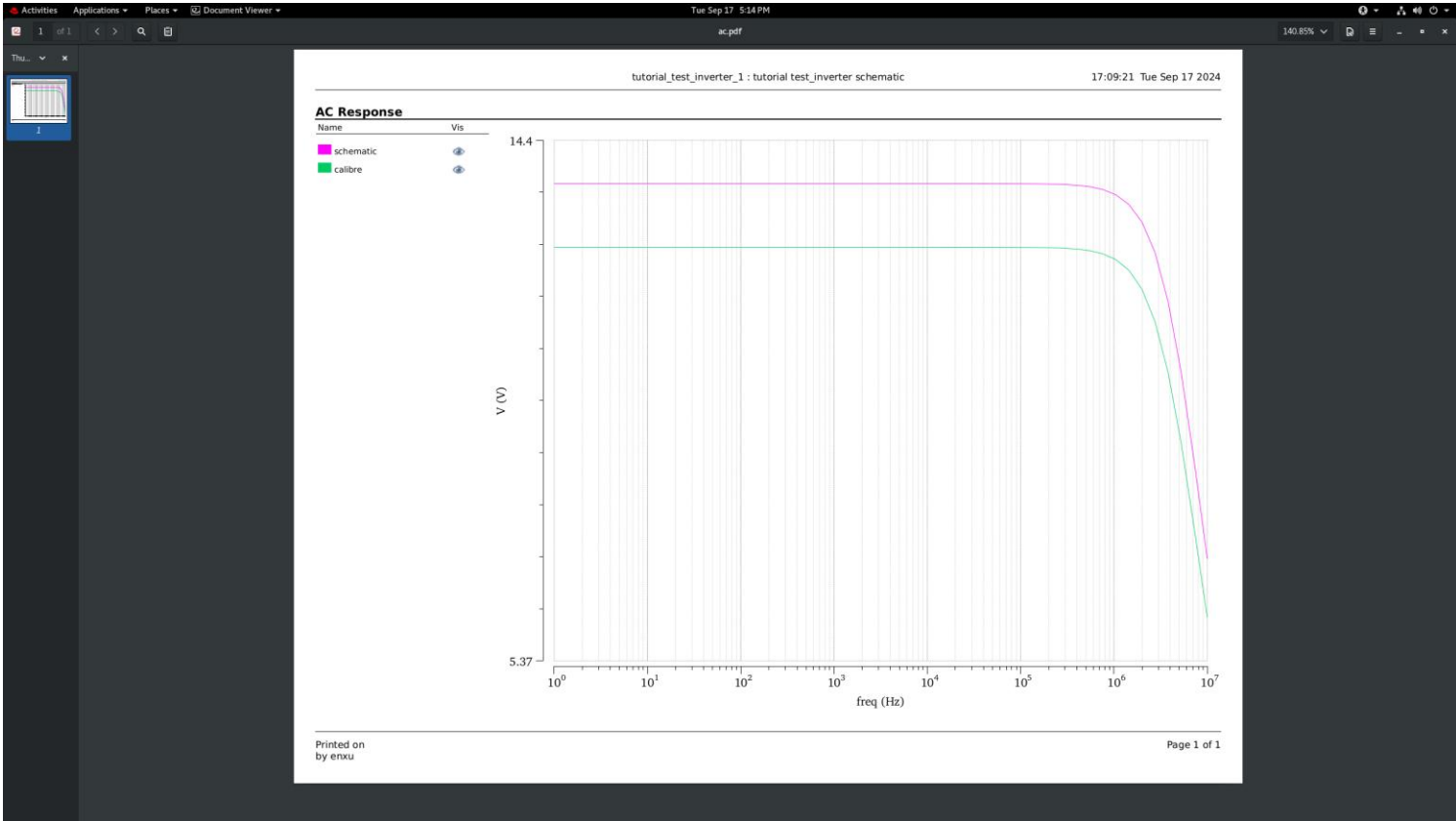
Row: 1 Col: 1

AC Gain magnitude for Schematic and PEX view:

test dc:



test ac:



The calibre generally has a lower magnitude than the schematic. This is because with the parasitic capacitors simulated, the low frequency signals are more attenuated.