

Ultra Lightweight Dehaze Methods for Robot Vision Using High-Level Synthesis

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內容從下一頁開始

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Using High-Level Synthesis

Subject:

11463154

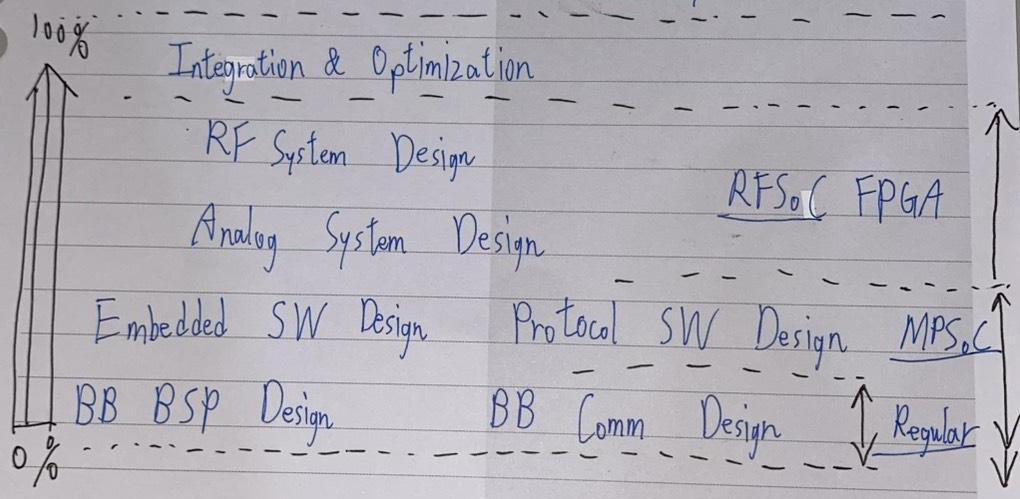
劉祐睿

No.:

Date: 2023.12.1.23

演講者: Chi-Chia Sun 教授
啟 嘉 宋

FPGA \Rightarrow SOPC \Rightarrow SoC \Rightarrow Cloud \Rightarrow RFSoC
since 1980 \downarrow 2012 ~ 2017 \downarrow 2017 ~ Today
2004 ~ 2012 \downarrow 2019 ~ Today



Dehaze Method

- ① Dark channel extraction
- ② Bright channel extraction
- ③ Transmission map estimation
- ④ Scene recovery

上課手寫筆記

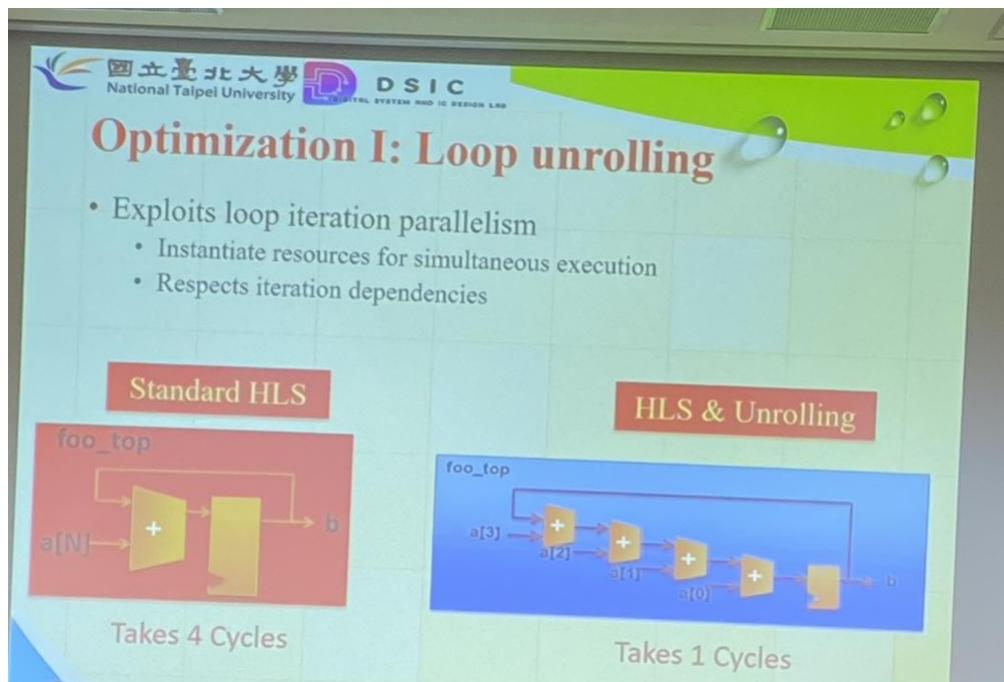


圖 1、迴圈運作示意圖

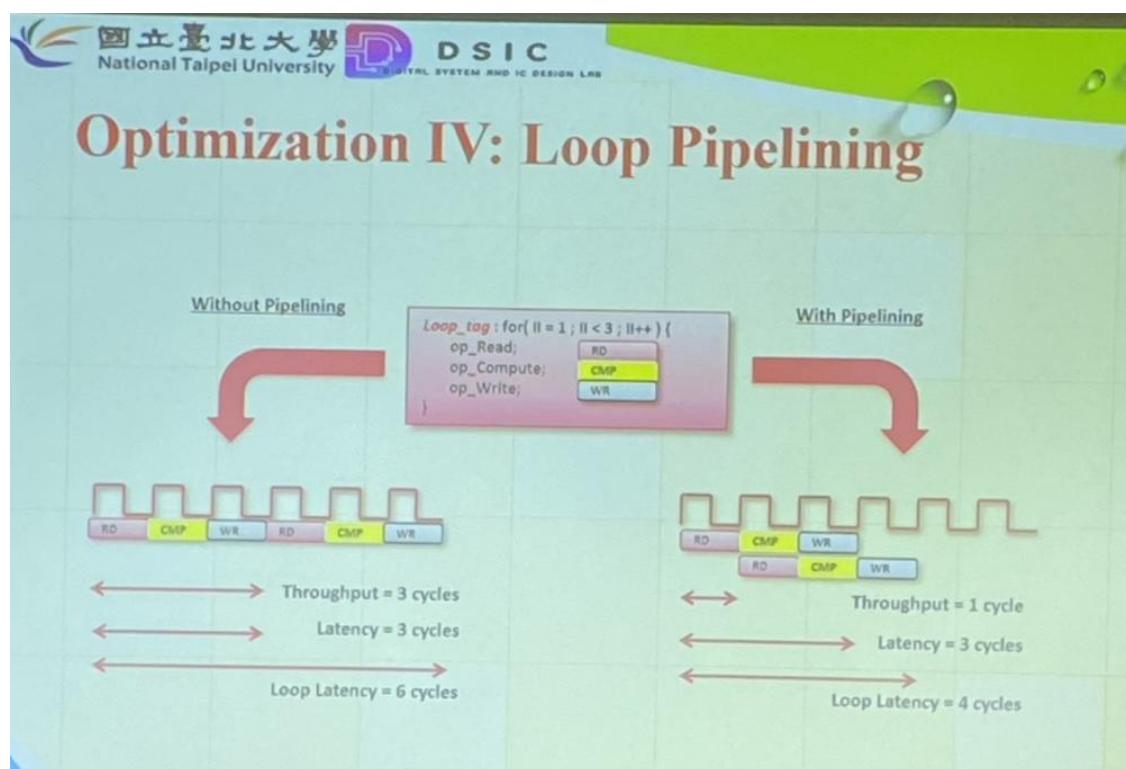


圖 2、指令管線化迴圈運作示意圖

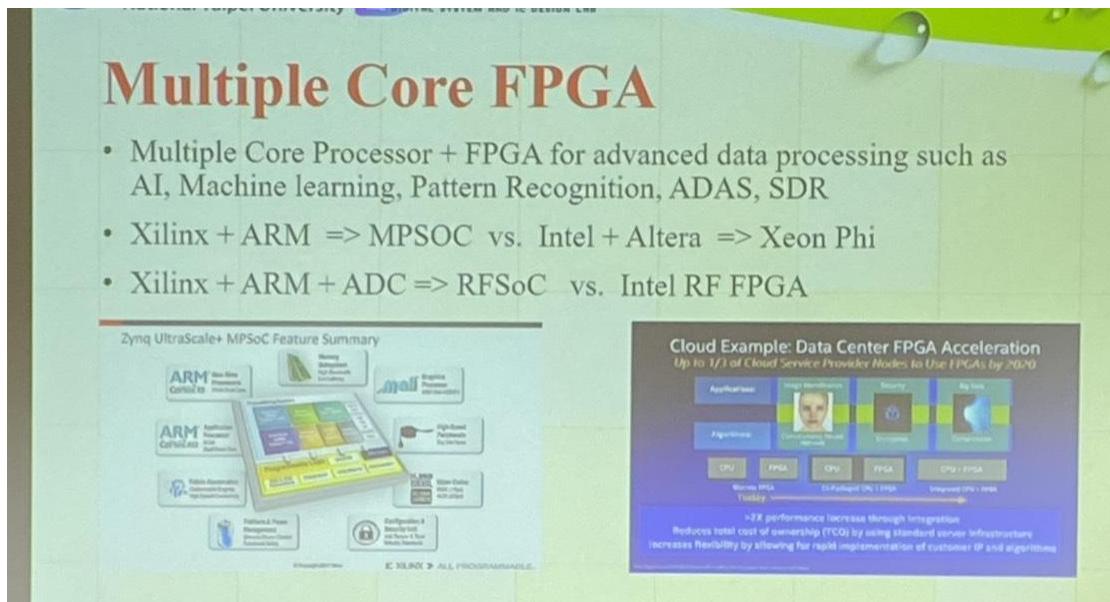


圖 3、多核心之 FPGA

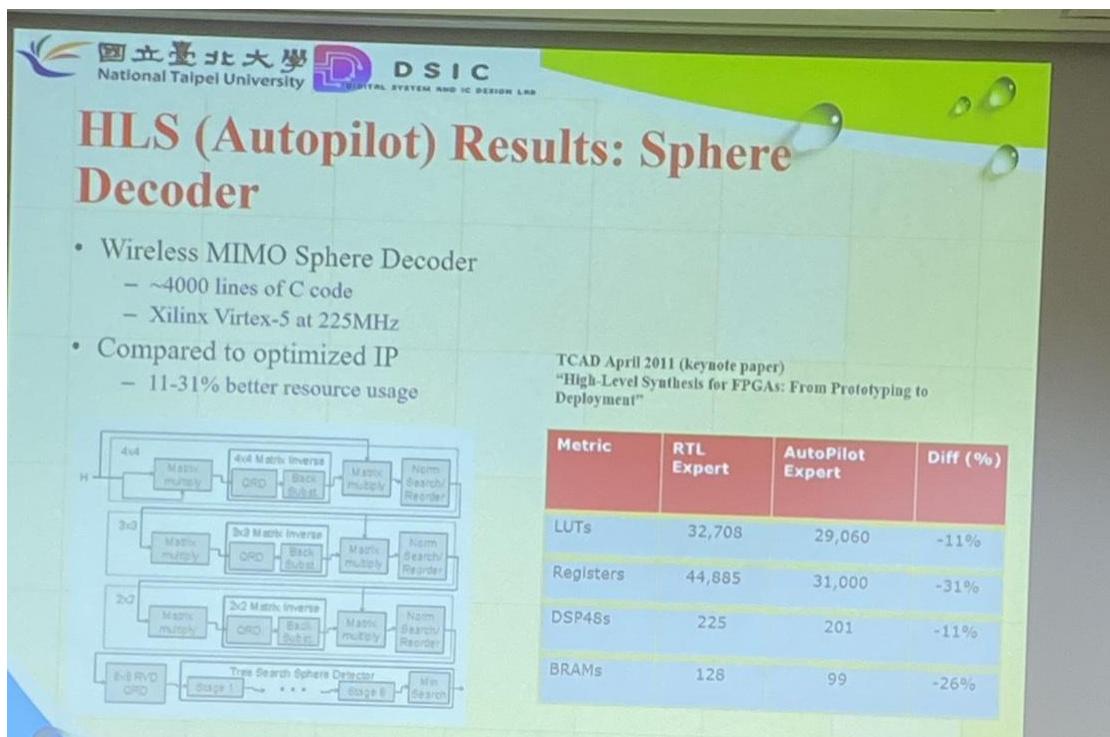


圖 4、Sphere Decoder

HLS (Autopilot) Results: QRD

2013 Xilinx All Programmer show that Vivado High Level Synthesis can achieve “For each project where we used Vivado HLS, we saved 2-3 weeks of engineering time.”

Radar Design 1024 x 64 QRD Floating Point data path	Conventional Hand-coded HDL Approach	Using Vivado High Level Synthesis
Design Language	VHDL (RTL)	C
Design Time (weeks)	12	1
Latency (ms)	37	21
Memory (RAMB1SE1)	134 (16%)	10 (1%)
Memory (RAMB36E1)	273 (65%)	138 (33%)
Registers	29686 (9%)	14263 (4%)
LUTs	28152 (18%)	24257 (16%)

CTO, Major broadcast equipment company “2013 Xilinx All Programmer”

圖 5、QRD

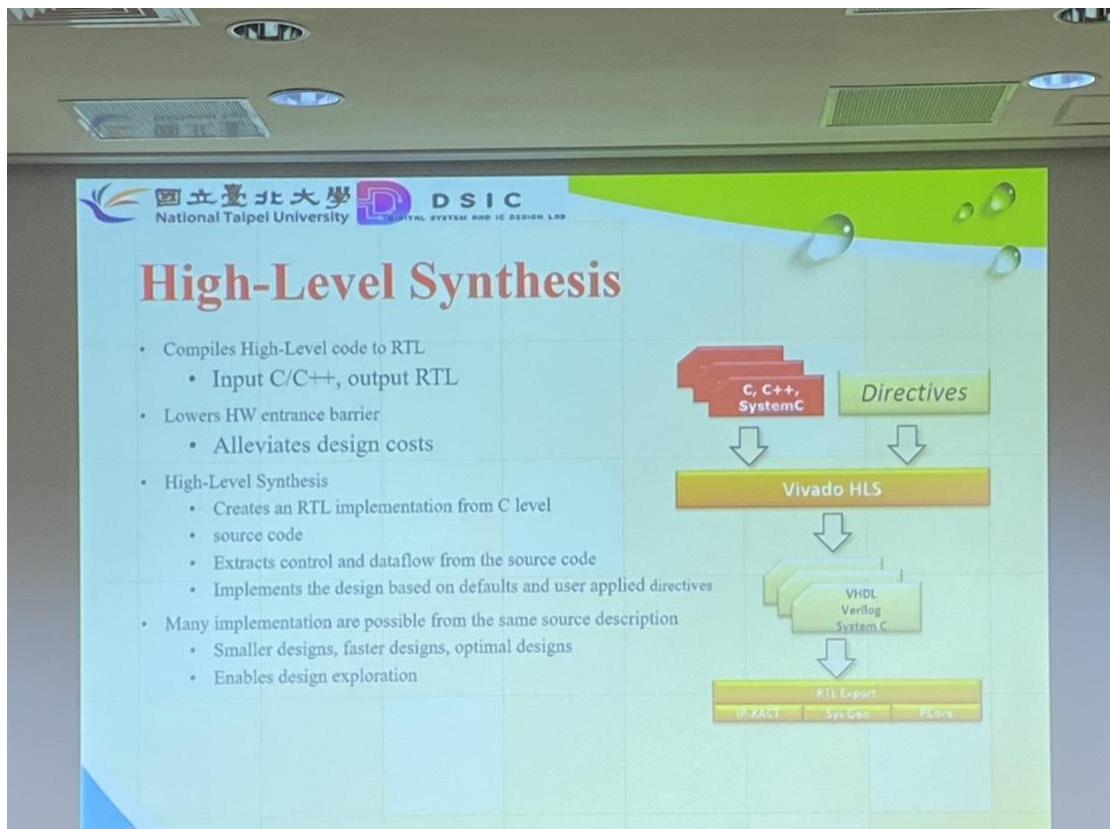


圖 6、C/C++語言與 FPGA 之關係

表 1、BenchMark 圖表

國立臺北大學
National Taipei University
DSIC
DIGITAL SYSTEM AND IC DESIGN LAB

Under Water Benchmark

- Dataset : UIEB dataset (890 images)(620x460)
- Acceptable PSNR in ~19db but ultra fast

Reference		MSE	PSNR	SSIM	FPS
RAW		1749.9235	17.4217	0.7696	
FE	2012 CVPR	908.2741	22.7601	0.8459	5.165
DILH	2016 TIP	1632.7069	19.9316	0.7905	1.406
HFM	2023 EAAI	1432.4021	17.9271	0.8203	1.590
WWPF	2024 TCSV	1207.9993	18.3705	0.7931	2.016
FUNIE_GAN	2020 RA-L	1512.4454	17.5479	0.6745	23.204
TACL_GAN	2022 TIP	595.1137	21.8242	0.7551	0.889
CCL-Net	2025 TMM	1110.7707	19.3194	0.7943	0.346
ours		975.3020	19.5485	0.8597	92.827