Modelling and Design of LCL-Filtered T-Type Inverters for Common-Mode Resonance Current Suppression in High-Power Applications

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***Abstract*—The three-level T-type inverter is a promising candidate in the photovoltaic (PV) field. However, it suffers from the leakage current problem, which can well be addressed by the improved *LCL* filter. Nonetheless, this improvement brings a new challenge of common-mode resonance current (CMRC). To deal with this issue, several CMRC suppression control strategies have been proposed. In high-power applications with low-switching frequencies, the conventional CMRC suppression control strategy becomes invalid, and hence the system stability degrades. To resolve this problem, this paper introduces a delay compensated CMRC (DCCMRC) suppression scheme. In this paper, the simplified model of the improved *LCL*-filtered T-type inverter is derived. Moreover, a delay compensation method is proposed to eliminate the unfavorable effect of the digital control delay. Finally, simulations and experiments are conducted to verify the effectiveness of the proposed method in stability improvement.**

Keywords—T-type inverters, LCL filters, leakage current suppression, resonance current suppression, control delay compensation

I. Introduction

In photovoltaic (PV) generation systems, the transformer-less three-level converter is widely used due to its benefits including lower switching stresses and costs as well as higher power quality [1]. However, in the absence of galvanic isolation, an undesired leakage current is generated when the common-mode (CM) circuit is formed between the inverter and the ground. This leakage current causes electromagnetic inferences, increases output current distortion, and poses safety hazards for humans [2]. Therefore, it is imperative to suppress the leakage current.

Various methods have been proposed to address the leakage current issue, including using novel topologies such as H7 and H8 [3], [4]. However, these methods necessitate complex modulation methods and additional power devices. In [5], by modifying the modulation algorithm, the amplitude of the common-mode voltage (CMV) can be reduced to suppress the leakage current with zero CMV vectors. However, partial vectors limit the modulation index and increase harmonics. In [6], a reduced CMV switching count strategy is proposed to lower the frequency of the CMV, but the complex modulation strategy increases computational burdens. Lately, a modified *LCL* filter is proposed to change the high-frequency leakage current path, leading to the reduction of the leakage current without additional switches or changes in modulation [7]. Therefore, the modified *LCL* filter is employed in this paper.

However, when using the modified *LCL* filter, the common-mode resonance current (CMRC) is generated, which causes inverter-side current oscillations and can lead to system instability. To solve the problem, passive damping methods are proposed in [8] and [9], yet suffering larger power losses. In [10], active damping methods are proposed, in which inverter-side differential mode current feedback and CM current feedback are simultaneously adopted. Unfortunately, these methods are not applicable to high-power applications, where the switching frequency must be low to avoid high switching losses. As the associated digital control delays in the low switching frequency range can be considerable, the bandwidth and stability margin of the CMRC suppression controller will be reduced, which means that the resonance current can hardly be suppressed.

To fill in the aforesaid research gap, a DCCMRC suppression strategy is proposed in this paper. With the proposed method, both the leakage current and resonance current can effectively be suppressed in high-power applications. The main contributions of this paper are threefold:

1) A simplified mathematical model of the three-level T-type inverter with the modified *LCL* filter is established.
2) The effect of the control delay on the stability of CMRC suppression controller is analyzed.
3) The DCCMRC control strategy is proposed and verified by simulations and experiments.

II. Modelling of The Improved *LCL*-Filtered T-Type Inverter

Fig. 1 shows the circuit diagram of the transformer-less T-type inverter. L is the inverter-side inductor, L_g is the grid-side inductor, C_f is the filter capacitor, C_{PV} is the parasitic capacitor, and C is the dc-link capacitor; n is the neutral point of the grid, O is the middle point of dc link, and N is the common point of the filter capacitors. We define the current flowing from point n to the earth as the common-mode current i_{cm}. It should be noted that, due to the absence of transformers, the leakage

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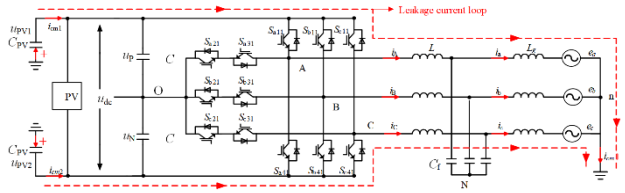
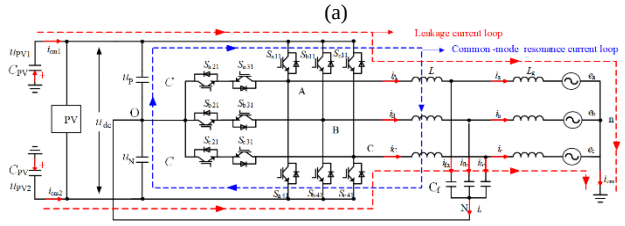
current path emerges, as depicted by the red dashed line in Fig.1 (a).



(a)



(b)

Fig.1 Grid-tied three-level T-type inverter structure with (a) the conventional *LCL* filter and (b) the modified *LCL* filter.

As shown in Fig. 1, based on Kirchhoff's law of voltage (KVL), the following equation can be derived:

$$\begin{cases} u_{AO} = L\dfrac{\mathrm{d}i_A}{\mathrm{d}t} + L_g\dfrac{\mathrm{d}i_a}{\mathrm{d}t} + e_a + u_{nO} \\ u_{BO} = L\dfrac{\mathrm{d}i_B}{\mathrm{d}t} + L_g\dfrac{\mathrm{d}i_b}{\mathrm{d}t} + e_b + u_{nO} \\ u_{CO} = L\dfrac{\mathrm{d}i_C}{\mathrm{d}t} + L_g\dfrac{\mathrm{d}i_c}{\mathrm{d}t} + e_c + u_{nO} \end{cases} \tag{1}$$

where u_{XO} (X = A, B, C) and i_X (X = A, B, C) are the inverter output voltages and inverter output currents, respectively. i_x (x = a, b, c) are the grid-side currents, e_x ($x = a, b, c$) are the grid voltages, and u_{nO} is the voltage between the grid neutral point n and the dc-link middle point O. Considering a balanced three-phase system, the sum of e_x is 0. Using this fact and summing up the three equations in (1), we have

$$\sum_{X=A,B,C} u_{XO} = \sum_{X=A,B,C} L\frac{\mathrm{d}i_X}{\mathrm{d}t} + \sum_{x=a,b,c} L_g\frac{\mathrm{d}i_x}{\mathrm{d}t} + 3u_{nO} \tag{2}$$

By use of Kirchhoff's law of current (KCL), $i_{cm} = i_a + i_b + i_c$ in Fig. 1. For the conventional *LCL* filter, it allows no zero-sequence current flowing through filter capacitors. Therefore, i_{cm} equals the sum of i_X (X = A, B, C), expressed as

$$i_{cm} = \sum_{x=a,b,c} i_x = \sum_{X=A,B,C} i_X \tag{3}$$

As shown in Fig. 1, i_{cm} can also be seen as the sum of the common-mode currents that flow through the parasitic capacitors connected to the positive and negative sides of the dc link. In this sense, i_{cm} can be expressed as

$$i_{cm} = i_{cm1} + i_{cm2} = 2C_{PV}\frac{\mathrm{d}u_{PV}}{\mathrm{d}t} \tag{4}$$

As illustrated in Fig. 1, the voltage between the neutral point of the grid *n* and the middle point of dc link O u_{nO} can be expressed as

$$\begin{cases} u_{nO} = u_{PV1} + u_P \\ u_{nO} = u_{PV2} - u_N \end{cases} \tag{5}$$

Summing up the two equations in (5) and divide both sides by 2, it yields

$$u_{nO} = u_{PV} + \frac{1}{2}(u_P - u_N) \tag{6}$$

Define u_d as the difference of the upper and lower capacitor voltages:

$$u_d = u_P - u_N \tag{7}$$

and define the common-mode voltage u_{cm} as

$$u_{cm} = \frac{1}{3}\sum_{X=A,B,C} u_{XO} \tag{8}$$

Substituting (3), (6), (7), and (8) into (2), the CM model of the conventional *LCL*-filtered T-type inverter can be obtained as

$$u_{cm} = \frac{1}{3}\left(L + L_g\right)\frac{\mathrm{d}i_{cm}}{\mathrm{d}t} + \frac{1}{2C_{pv}}\int i_{cm}\mathrm{d}t + \frac{1}{2}u_d \tag{9}$$

Fig. 2(a) depicts the equivalent circuit of the CM model corresponding to Fig. 1(a), in which the two voltage sources of the leakage current i_{cm} are revealed: the difference of two dc voltages u_d and the common mode voltage u_{cm}. Typically, the dc bus is balanced. Thus, the current introduced by u_d can be blocked by the capacitor, and hence ignored in the following analysis. As a result, it is concluded that u_{cm} is the primary factor that causes the leakage current, especially for its high-frequency components.

In order to suppress the leakage current i_{cm}, the modified *LCL* filter is implemented by connecting the common point of the filter capacitors N to the middle point of the dc-link O, leading to the formation of the inner common mode current path as the blue dashed loop drawn in Fig. 1(b). According to KVL, the following equations can be derived:

$$\begin{cases} u_{AO} = L\dfrac{\mathrm{d}i_A}{\mathrm{d}t} + \dfrac{1}{C_f}\int i_{fa}\mathrm{d}t \\ u_{BO} = L\dfrac{\mathrm{d}i_B}{\mathrm{d}t} + \dfrac{1}{C_f}\int i_{fb}\mathrm{d}t \\ u_{CO} = L\dfrac{\mathrm{d}i_C}{\mathrm{d}t} + \dfrac{1}{C_f}\int i_{fc}\mathrm{d}t \end{cases} \tag{10}$$

where i_{fx} (x = a, b, c) are the filter capacitor currents.

By summing up the three equations in (10), we have

$$\sum_{X=A,B,C} u_{XO} = \sum_{X=A,B,C} L\frac{\mathrm{d}i_X}{\mathrm{d}t} + \sum_{x=a,b,c}\int\frac{i_{fx}}{C_f}\mathrm{d}t \tag{11}$$

Using KCL, the following equation can be obtained from Fig. 1(b):

$$\sum_{X=A,B,C} i_X = \sum_{x=a,b,c} i_{fx} + \sum_{x=a,b,c} i_x \tag{12}$$

Define the sum of filter capacitor currents i_{fx} ($x = a, b, c$) as i_z, the CM model of the modified-*LCL*-filtered system can be derived as

$$u_{cm} = \frac{1}{3}L\frac{\mathrm{d}(i_{cm} + i_z)}{\mathrm{d}t} + \frac{1}{3}\frac{1}{C_f}\int i_z\mathrm{d}t \tag{13}$$

The equivalent model of (13) is presented in Fig. 2(b). It can be seen from Fig. 2(b) that the implementation of the modified *LCL* filter provides an alternative low impedance C_f (C_f >> C_{PV}) branch to the circuit, which can greatly suppress the leakage current i_{cm} by offering a path with much lower impedances. Although the modified *LCL* filter works well in leakage current attenuation, it brings a new challenge to the system stability. As shown in Fig. 2(b), the filter inductor L and filter capacitor C_f in the common mode equivalent circuit has an inherent risk of generating CMRC. The CMRC will cause significant inverter-side current oscillations and degrade system stability, even leading to system instability in the low frequency range if the phase lag caused by control delay was pronounced. To address the issue, a delay compensated common mode resonance current (DC-CMRC) controller is proposed and analyzed as follows.

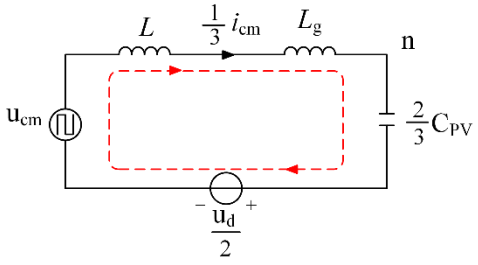


Fig. 2 Equivalent models of the CM circuits with (a) the conventional *LCL* filter and (b) the modified *LCL* filter.

III. Analysis and Design of the Proposed DCCMRC Control Strategy

To understand the influence of control delays on the CMRC control, Subsection-A first investigates the mechanism of control delays, followed by Subsection-B that establishes the model of the CMRC control, which takes delays into consideration and analyzes the negative effect of delays. To alleviate the adverse effect of delays, a simple and model-free compensation technique is introduced into the CMRC control design in subsection C. Finally, the stability analysis of the DCCMRC controller is given in subsection D.

A. Digital Control Delays

It has been fully investigated in the previous studies that digital control delays come from two sources, including modulation and calculation [12].

The process of modulation is typically modelled as an ideal sampler followed by a zero-order hold, which processes the modulating signal $m(t)$ to $m_s(t)$, and the PWM waveform is generated after the comparison of $m_s(t)$ and the carrier waveform $c(t)$. In this way, a delay can be introduced by the modulator for the time difference between $m(t)$ sampling instants and the instants when output pulses are determined. Consider the modulator to be characterized by the sample and hold delay, and define the sampling time as T_s, the transfer function of the modulation delay $G_{zoh}(s)$ can be approximated as

$$G_{zoh}(s) \approx \frac{1-e^{-T_s s}}{s} \tag{14}$$

Another source of delay to be dealt with is the calculation delay, i.e., the time required to commute a new m value, which takes up a significant fraction of modulation delay and is typically assumed to be equal to one sampling period as a worst case approximation:

$$G_{cal}(s) = e^{-sT_s} \tag{15}$$

B. Analysis of CMRC Controller

Assuming that the leakage current is well suppressed, i.e., $i_{cm} = 0$, (13) can be simplified as

$$3u_{cm} = L\frac{di_{cmz}}{dt} + \frac{1}{C_f}\int i_{cmz}dt \tag{16}$$

Taking the Laplace transform of (16), we derive

$$G_{plant}(s) = \frac{i_{cmz}(s)}{3u_{cm}(s)} = \frac{C_f s}{1+LC_f s^2} \tag{17}$$

For simplicity, define the resonance frequency of the added circuit as

$$\omega_{res} = \sqrt{\frac{1}{LC_f}} \tag{18}$$

The continuous-time domain model of the CMRC control loop is shown in Fig.3, wherein Reg(z) is the digital PI controller, and the PWM gain of the inverter is assumed to be equal to unity.

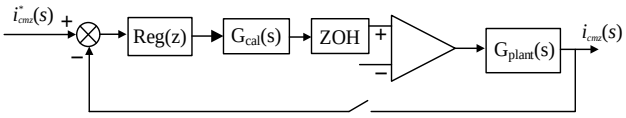


Fig. 3 Model of the CMRC control loop in continuous domain.

For the CMRC controller implemented in the discrete domain, its ZOH equivalent $G_{cmc}(z)$ will be

$$\begin{aligned} G_{cmc}(z) &= (1-z^{-1})Z\left\{L^{-1}\left[\frac{G_{plant}(s)}{s}\right]\right\} \\ &= (1-z^{-1})Z\left[\frac{1}{L\omega_{res}}\cdot\frac{\omega_{res}}{s^2+\omega_{res}^2}\right] \\ &= \frac{z-1}{zL\omega_{res}}\cdot\frac{\sin(\omega_{res}T_s)}{z^2-2z\cos(\omega_{res}T_s)+1} \end{aligned} \tag{19}$$

Define H_{i1} and H_{i2} to be

$$\begin{cases} H_{i1} = \sin(\omega_{res}T_s) \\ H_{i2} = \cos(\omega_{res}T_s) \end{cases} \tag{20}$$

(19) can be rewritten as

$$G_{cmc}(z)=\frac{H_{i1}z-H_{i1}}{L\omega_{res}z^2-2L\omega_{res}H_{i2}z+L\omega_{res}} \quad (21)$$

In order to simplify the analysis, assuming the gain of the integrator is properly designed, i.e., its phase lag is negligible, the PI controller can be considered as a simple proportional gain K_p, the system loop gain $G_{open}(z)$ can be written as

$$G_{open}(z)=z^{-1}K_pG_{cmc}(z)=\frac{K_pH_{i1}z-K_pH_{i1}}{L\omega_{res}z^3-2L\omega_{res}H_{i2}z^2+L\omega_{res}z} \quad (22)$$

The Bode diagram of (22) is plotted in Fig. 5 with the parameters listed in Table I. As seen, its phase curve has a sharp drop at the resonance frequency by 180° where the magnitude is greater than 0 dB. When the switching frequency drops from 10 kHz to 2 kHz, the phase curve continues to go down, and −180° crossing takes place at the frequency of 2 kHz. According to Nyquist stability criterion, the system is unstable when the phase curve takes a negative crossing at resonance frequency f_{res}, meaning that the CMRC can no longer be suppressed in the high power application unless the effect of control delay could be mitigated.

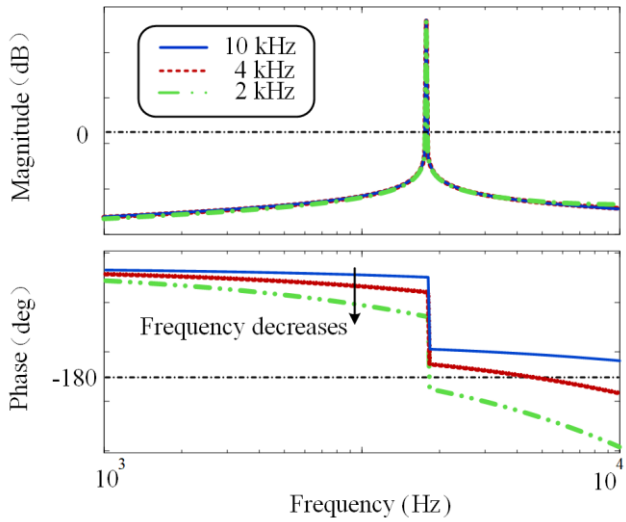


Fig. 4 Bode diagram of the loop gain of conventional CMRC controllers with different switching frequencies.

C. *Proposed delay compensated CMRC suppression method*

Many delay compensation methods have been explored in the previous studies. In [13], a multisampling method is proposed to compensate delays. However, the drawback of the approach is the need for proper filtering of switching noise, which may impair the system stability. Besides, the implementation of multisampling requires additional hardware, limiting the application of the method. In more recent studies, compensation techniques that can be implemented digitally are more favored especially in cost-sensitive applications.

From the above analysis in subsection B, it can be seen that the phase lag brought by the control delay is culprit of the system instability. A simple and intuitive way to cancel out the unfavorable effect of delay is to lift the phase curve to avoid −180° crossing at f_{res}. Therefore, a digital compensation method using the feedback of the previous step of error is introduced to offer a phase lead at the resonance frequency.

The discrete transfer function of the delay compensator $W(z)$ is expressed as

$$W(z)=\frac{1+K_c}{1+K_cz^{-1}} \quad (23)$$

where K_c is the compensation coefficient. The relationship between the compensated modulation signal $m_c(z)$ and the uncompensated modulation signal $m_u(z)$ can be expressed as

$$\frac{m_c(z)}{m_u(z)}=\frac{1+K_c}{1+K_cz^{-1}}z^{-1} \quad (24)$$

Rearranging (24), the following equation can be yielded as

$$m_c(k)=m_u(k-1)+K_c[m_u(k-1)-m_c(k-1)] \quad (25)$$

in which $m_u(k-1)$, $m_u(k)$, $m_c(k-1)$, and $m_c(k)$ represent the uncompensated modulation signal $m_u(z)$ and compensated signal $m_c(z)$ at (k-1)th and kth step, respectively. From (25), it is clear that the modulation signal compensation can be achieved by using information at the previous step.

To give an intelligible analysis of how the compensator works, we present a graphical representation of the delay compensation effect in Fig. 5. As shown in Fig. 5, the green line represents the uncompensated modulation signal $m_u(k)$, the red line(one step ahead) is the ideal modulation signal $m_i(k)$, and the blue line represents the compensated modulation signal. When applying the compensator into the control, the value of the modulation signal gets closer to its ideal condition, where the proximity depends on the compensator coefficient K_c.

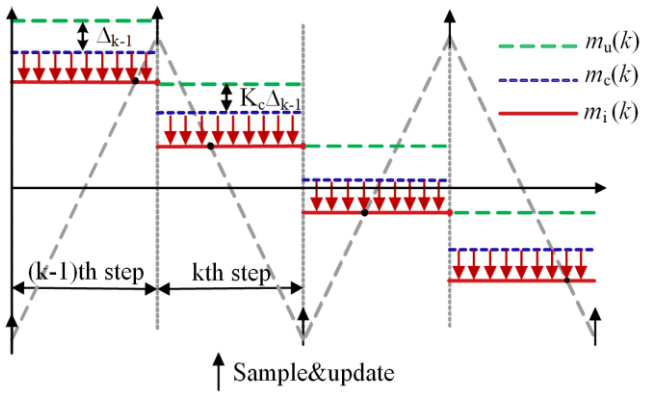


Fig. 5 Graphical illustration of the proposed compensation technique in PWM process.

In other words, the compensation coefficient K_c determines the extent to which the control delay is compensated. The larger the compensator coefficient K_c is, the closer the compensated modulation signal $m_i(k)$ gets to the ideal value, meaning that the better compensation effect of the phase lag can be achieved. However, it can also be observed from Fig.6 that while higher coefficient K_c contributes to better compensation effect, it would also have a lager magnitude for the compensator. When K_c =1, i.e., the critical value, the system becomes prone to noise around specific frequency [11]. Therefore, we select a K_c value lower than 1 to avert the dilemma.

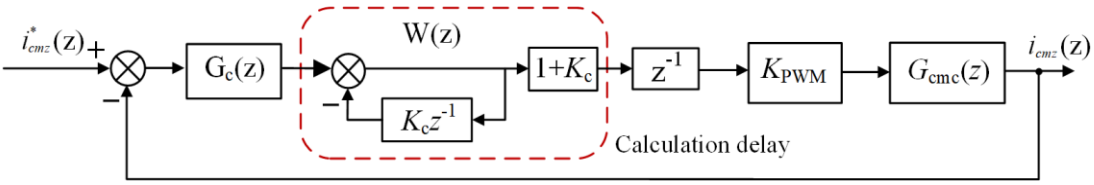


Fig. 7 Model of the DCCMRC control loop in discrete domain.

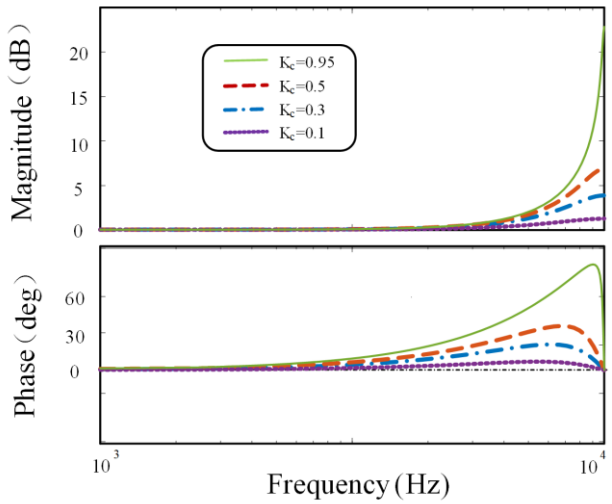


Fig. 6 Bode diagram comparison of different K_c.

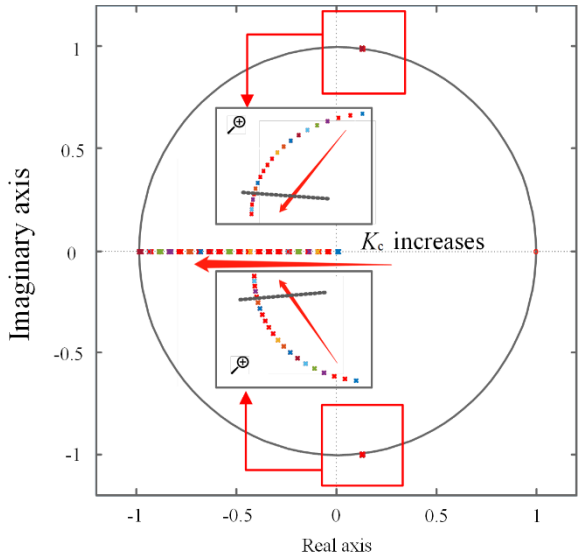


Fig.9 Pole-zero map for the DCCMRC controller with K_c increasing.

D. *Stability analysis of the DCCMRC control Strategy*

Fig.7 illustrates the control block of the DCCMRC controller. To verify its stability improvement performance, the open loop transfer function of the DCCMRC controller is re-derived in (26).

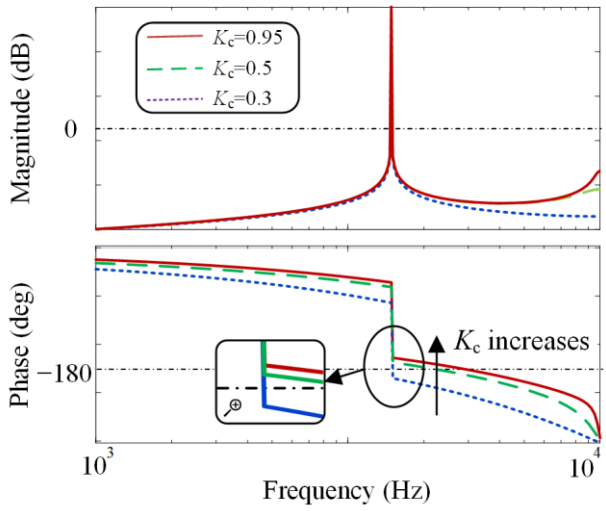


Fig.8 Bode diagram of the DCCMRC controller with different K_c.

Fig. 8 plots the Bode diagram of the DCCMRC controller with the parameters listed in Table I. As seen, the delay compensator effectively contributes to the system stability difference, and with K_c increases, the stability region is widened. When K_c is 0.95, the system is stable. Its corresponding root locus is presented in Fig.9, which again indicates the stability performance improvement when K_c increases as the poles move into the region of convergence.

IV. Simulation and Experimental Verifications

A. *Simulation Results*

Simulations have been performed to verify the proposed method using the parameters in TABLE I. The simulation results of the grid current and the inverter current as well as the leakage current are presented in Fig.10. The switching frequency is set to 4 kHz, and the compensation coefficient is set to 0.95. Look at the current behavior after switching to non-DCCMRC control mode, it can be observed that the inverter current exhibits great oscillation caused by CMRC, leading to deterioration of the grid-connected current and spike of leakage current.

$$G_{open}(z) = z^{-1}K_pG_{cmc}(z) = \frac{K_pH_{i1}z - K_pH_{i1}}{L\omega_{res}z^3 - 2L\omega_{res}H_{i2}z^2 + L\omega_{res}z} \tag{26}$$

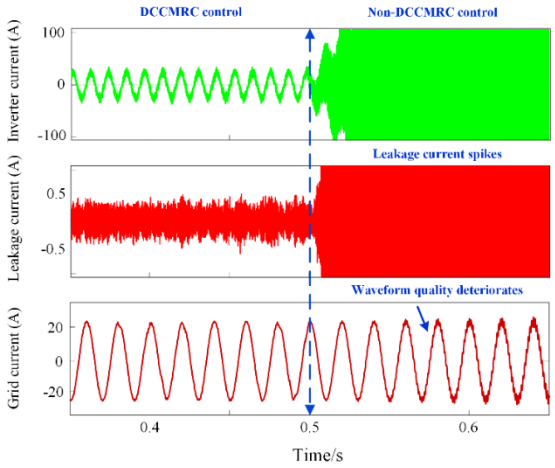


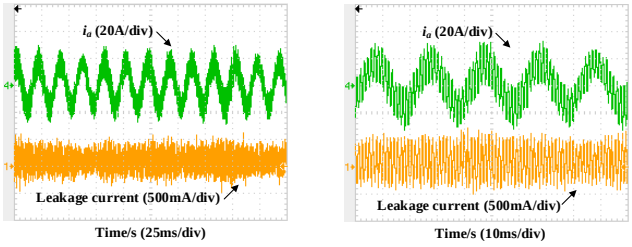
Fig.10 Simulation results of leakage current and grid current.

B. *Experimental Results*

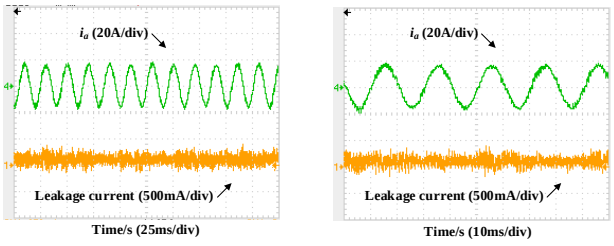
The experimental parameters are listed in TABLE I.

TABLE I. EXPERIMENTAL PARAMETERS

C	1500 μF
C_{PV}	0.15 μF
C_f	10 μF
L	3 mH
L_g	3 mH
T_s	250 μs
V_{dc}	700 V
e_{abc} (Phase-to-phase)	380 V (Peak)
Line resistance	1 Ω



(a)



(b)

Fig. 11. The experimental results of (a) the resonance current and the leakage current without using the DCCMRC control scheme and (b) the output current and the leakage current after using the DCCMRC control scheme.

As shown in Fig.11 (a), For low switching frequency, the conventional method for suppressing the resonance current is invalid and the leakage current increases correspondingly. After applying the proposed DCCMRC controller as shown in Fig.11 (b), the inverter current quality is enhanced with the resonance current largely mitigated, and the leakage current is effectively suppressed. In conclusion, the proposed DCCMRC controller has a good performance for resonance current and leakage current suppression in low switching frequencies.

V. CONCLUSION

This paper proposes a DCCMRC control scheme for three-level T-type inverters with the modified *LCL* filter. By investigating the stability issues of the system, the compensation coefficient K_c of the DCCMRC controller is well selected. With the proposed scheme, both leakage current and resonance current can effectively be suppressed in high power applications.

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