Modeling and Design of *LCL*-Filtered T-Type Inverters for Common-Mode Resonance Current Suppression in High-Power Applications

Bei Liu
School of Control Science and Engineering
Shandong University
Jinan, China
beiliu@mail.sdu.edu.cn

Xiangyang Xing
School of Control Science and Engineering
Shandong University
Jinan, China
xyxing@sdu.edu.cn

Rui Zhang
School of Control Science and Engineering
Shandong University
Jinan, China
sduzr2021@mail.sdu.edu.cn

Chang Liu
School of Control Science and Engineering
Shandong University
Jinan, China
202220688@mail.sdu.edu.cn

Chuangping Wen
School of Control Science and Engineering
Shandong University
Jinan, China
202114740@mail.sdu.edu.cn

***Abstract*—In the photovoltaic (PV) field, the three-level T-type inverter has largely been accepted as a promising candidate. However, it suffers from the leakage current problem, which can well be addressed by the modified *LCL* filter. Nonetheless, this modification brings a new challenge of common-mode resonance current (CMRC). To deal with this issue, several CMRC suppression control strategies have been proposed. In high-power applications with low-switching frequencies, the conventional CMRC suppression control strategy becomes invalid, and hence the system stability degrades. To resolve this problem, this paper introduces a delay compensated CMRC (DCCMRC) suppression scheme. In this paper, the simplified model of the modified *LCL*-filtered T-type inverter is derived. Later, a delay compensation method is proposed to eliminate the unfavorable effect of the digital control delay. Finally, the efficacy of the proposed methodology is validated through a set of simulations and experiments.**

Keywords—T-type inverters, LCL filters, leakage current suppression, resonance current suppression, control delay compensation

I. Introduction

In the field of photovoltaic (PV) power generation, the transformer-less three-level converter is widely used due to its benefits including lower switching stresses and costs as well as higher power quality [1]. However, in the absence of galvanic isolation in this setup leads to an undesired leakage current when the common-mode (CM) circuit forms between the inverter and the ground. The leakage current has the potential of causing electromagnetic interferences, increasing grid-connected current harmonics, and poses safety hazards for humans [2]. Therefore, it becomes essential to mitigate this leakage current.

Various methods have been proposed to cope with the aforementioned issue, including using novel topologies such as H7 and H8 [3], [4]. However, these methods necessitate complex modulation methods and additional power devices. In [5], modifying the modulation algorithm can reduce the amplitude of the common-mode voltage (CMV) to suppress the leakage current while using zero CMV vectors. However, partial vectors limit the modulation index and increase harmonics. Another strategy proposed in [6] introduces a reduced CMV switching count approach to decrease the CMV frequency, but the complex modulation strategy increases computational burdens. Recently, a modified *LCL* filter has been proposed in [7], which alters the circulating path of the leakage current without the need for additional switches or changes in modulation [7]. Hence, the modified *LCL* filter is utilized in this paper.

However, the use of the modified *LCL* filter inevitably leads to the generation of CMRC, and this can cause inverter-side current oscillations and even system instability. To solve the problem, passive damping methods are proposed in [8] and [9], yet suffering larger power losses. In [10], active damping methods are proposed, in which inverter-side differential mode current feedback and CM current feedback controllers are simultaneously adopted. Unfortunately, these methods are not feasible in high-power applications, where low switching frequencies are necessary to mitigate high switching losses. Nevertheless, the associated digital control delays at lower switching frequencies can be significant, rendering the effective suppression of CMRC a challenge unless the CMRC controller can be re-designed.

To fill in the aforesaid research gap, this paper presents a novel strategy for DCCMRC suppression. The proposed methodology mitigates both the leakage current and resonance current issues in high-power applications. The key contributions of this paper are delineated as follows:

1) Establishing a simplified mathematical model of the three-level T-type inverter integrated with the modified *LCL* filter.

2) Analyzing the performance limitations of the control delays on the stability of CMRC suppression controller.

3) Proposing and verifying the DCCMRC control strategy through simulations and experiments.

II. Modelling of The Modified *LCL*-Filtered T-Type Inverter

Figure 1 shows the circuit configuration of the transformer-less T-type inverter. Within the diagram, we designate inverter-side inductance as L, the grid-side inductance as L_g, the filter capacitance as C_f, the parasitic capacitance as C_{PV}, and the dc-link capacitance as C. Additionally, certain critical points within the circuit are defined for reference: the neutral point of the grid is referred as ‘n’, the midpoint of the dc link is referred to as ‘O’, and the

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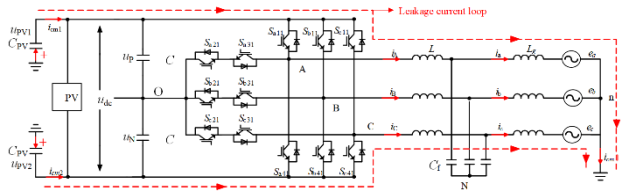
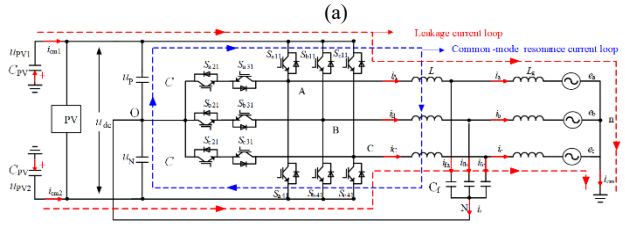
common junction of the filter capacitors is referred as 'N'. We define the current flowing from point n to the earth as the common-mode current i_{cm}. It should be noted that, owing to the absence of transformers, a leakage current path emerges, as indicated by the red dashed line in Fig.1 (a).



(a)



(b)

Fig.1 Grid-connected three-level T-type inverter structure with (a) the conventional *LCL* filter and (b) the modified *LCL* filter.

In accordance of Kirchhoff's law of voltage (KVL), as depicted in Fig.1, we can derive the following equation:

$$\begin{cases} u_{AO} = L\dfrac{\mathrm{d}i_A}{\mathrm{d}t} + L_g\dfrac{\mathrm{d}i_a}{\mathrm{d}t} + e_a + u_{nO} \\ u_{BO} = L\dfrac{\mathrm{d}i_B}{\mathrm{d}t} + L_g\dfrac{\mathrm{d}i_b}{\mathrm{d}t} + e_b + u_{nO} \\ u_{CO} = L\dfrac{\mathrm{d}i_C}{\mathrm{d}t} + L_g\dfrac{\mathrm{d}i_c}{\mathrm{d}t} + e_c + u_{nO} \end{cases} \tag{1}$$

Here, u_{XO} (X = A, B, C) and i_X (X = A, B, C) represent the inverter output voltages and currents, respectively. i_x (x = a, b, c) are the grid-side currents, e_x ($x = a, b, c$) represents the grid voltages, and u_{nO} represents the voltage between points n and O. For a balanced three-phase system, the sum of e_x is 0. Using this fact and summing up the three equations in (1), we have

$$\sum_{X=A,B,C} u_{XO} = \sum_{X=A,B,C} L\frac{\mathrm{d}i_X}{\mathrm{d}t} + \sum_{x=a,b,c} L_g\frac{\mathrm{d}i_x}{\mathrm{d}t} + 3u_{nO} \tag{2}$$

By use of Kirchhoff's law of current (KCL), $i_{cm} = i_a + i_b + i_c$ in Fig. 1. For the conventional *LCL* filter, it allows no zero-sequence current flowing through filter capacitors. Therefore, i_{cm} equals the sum of i_X (X = A, B, C), expressed as

$$i_{cm} = \sum_{x=a,b,c} i_x = \sum_{X=A,B,C} i_X \tag{3}$$

As depicted in Fig. 1, i_{cm} can also be seen as the aggregate of the common-mode currents coursing through the parasitic capacitors linked to both the positive and negative terminals of the dc link. In this sense, i_{cm} can be expressed as

$$i_{cm} = i_{cm1} + i_{cm2} = 2C_{PV}\frac{\mathrm{d}u_{PV}}{\mathrm{d}t} \tag{4}$$

As illustrated in Fig. 1, u_{nO} can be expressed as

$$\begin{cases} u_{nO} = u_{PV1} + u_P \\ u_{nO} = u_{PV2} - u_N \end{cases} \tag{5}$$

Summing up the two equations in (5) and divide both sides by 2, it yields

$$u_{nO} = u_{PV} + \frac{1}{2}(u_P - u_N) \tag{6}$$

Define u_d as the difference of the upper and lower capacitor voltages:

$$u_d = u_P - u_N \tag{7}$$

and define the common-mode voltage u_{cm} as

$$u_{cm} = \frac{1}{3}\sum_{X=A,B,C} u_{XO} \tag{8}$$

Substituting (3), (6), (7), and (8) into (2), we can derive the common-mode(CM) model of the conventional *LCL*-filtered T-type inverter as follows:

$$u_{cm} = \frac{1}{3}\left(L + L_g\right)\frac{\mathrm{d}i_{cm}}{\mathrm{d}t} + \frac{1}{2C_{pv}}\int i_{cm}\mathrm{d}t + \frac{1}{2}u_d \tag{9}$$

Fig. 2(a) shows the CM model that corresponds to Fig. 1(a), which reveals the sources of the leakage current i_{cm}: the difference of two dc voltages u_d and the common mode voltage u_{cm}. Typically, the dc bus is in a balanced state, and the capacitor can block the current introduced by u_d, which can thus be ignored in subsequent analysis. Therefore, u_{cm} is the primary factor that causes the leakage current, particularly its high-frequency components.

In order to mitigate the leakage current i_{cm}, the modified *LCL* filter is implemented, connecting N and O. As a result, this modification establishes an alternative inner path for the common-mode current, as indicated by the blue dashed loop in Fig. 1(b). By applying KVL, we can derive the following set of equations:

$$\begin{cases} u_{AO} = L\dfrac{\mathrm{d}i_A}{\mathrm{d}t} + \dfrac{1}{C_f}\int i_{fa}\mathrm{d}t \\ u_{BO} = L\dfrac{\mathrm{d}i_B}{\mathrm{d}t} + \dfrac{1}{C_f}\int i_{fb}\mathrm{d}t \\ u_{CO} = L\dfrac{\mathrm{d}i_C}{\mathrm{d}t} + \dfrac{1}{C_f}\int i_{fc}\mathrm{d}t \end{cases} \tag{10}$$

where i_{fx} (x = a, b, c) are the filter capacitor currents.

By summing up the three equations in (10), we have

$$\sum_{X=A,B,C} u_{XO} = \sum_{X=A,B,C} L\frac{\mathrm{d}i_X}{\mathrm{d}t} + \sum_{x=a,b,c}\int\frac{i_{fx}}{C_f}\mathrm{d}t \tag{11}$$

Using KCL, the following equation can be obtained from Fig. 1(b):

$$\sum_{X=A,B,C} i_X = \sum_{x=a,b,c} i_{fx} + \sum_{x=a,b,c} i_x \tag{12}$$

Define the sum of filter capacitor currents i_{fx} ($x = a, b, c$) as i_z, the CM model of the modified-*LCL*-filtered system can then be derived as

$$u_{cm} = \frac{1}{3}L\frac{\mathrm{d}(i_{cm} + i_z)}{\mathrm{d}t} + \frac{1}{3}\frac{1}{C_f}\int i_z\mathrm{d}t \tag{13}$$

The equivalent model of (13) is presented in Fig. 2(b). It is clear from Fig. 2(b) that the implementation of the modified *LCL* filter introduces an alternative low impedance C_f ($C_f >> C_{PV}$) branch to the circuit, which can greatly suppress the leakage current i_{cm} by offering a path with much lower impedances. Although the modified *LCL* filter works well in leakage current attenuation, it brings a new challenge to the system stability. As shown in Fig. 2(b), the filter inductor L and filter capacitor C_f in the common mode equivalent circuit has an inherent risk of generating CMRC. The CMRC will result in significant inverter-side current oscillations and degrade system stability, even leading to system instability particularly in the low frequency range where the control delay is pronounced. To address this issue, a delay compensated common mode resonance current (DC-CMRC) controller is proposed and analyzed as follows.

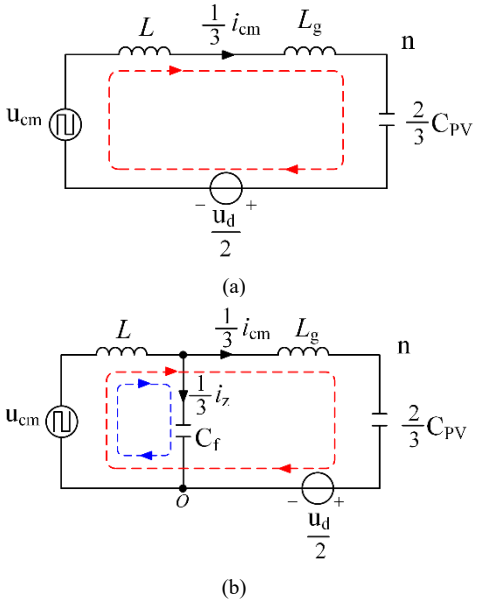


Fig. 2 Equivalent models of the CM circuits with (a) the conventional *LCL* filter and (b) the modified *LCL* filter.

III. Analysis and Design of the Proposed DCCMRC Control Strategy

To understand the influence of control delays on the CMRC control, Subsection-A first investigates the mechanism of control delays, followed by Subsection-B that establishes the model of the CMRC control, which takes delays into consideration and analyzes the negative effect of delays. To alleviate the adverse effect of delays, a simple and model-free compensation technique is introduced into the CMRC control design in subsection C. Finally, the stability analysis of the DCCMRC controller is given in subsection D.

A. Digital Control Delays

It has been fully investigated in the previous studies that digital control delays come from two sources, including modulation and calculation [12].

The process of modulation is typically modelled as an ideal sampler followed by a zero-order hold, which processes the modulating signal $m(t)$ to $m_s(t)$, and the PWM waveform is generated after the comparison of $m_s(t)$ and the carrier waveform $c(t)$. In this way, a delay can be introduced by the modulator for the time difference between $m(t)$ sampling instants and the instants when output pulses are determined. Consider the modulator to be characterized by the sample and hold delay, and define the sampling time as T_s, the transfer function of the modulation delay $G_{zoh}(s)$ can be approximated as

$$G_{zoh}(s) \approx \frac{1-e^{-T_s s}}{s} \tag{14}$$

Another source of delay to be dealt with is the calculation delay, i.e., the time required to commute a new m value, which takes up a significant fraction of modulation delay and is typically assumed to be equal to one sampling period as a worst case approximation:

$$G_{cal}(s) = e^{-sT_s} \tag{15}$$

B. Analysis of CMRC Controller

Assuming that the leakage current is well suppressed, i.e., $i_{cm} = 0$, (13) can be simplified as

$$3u_{cm} = L\frac{di_{cmz}}{dt} + \frac{1}{C_f}\int i_{cmz}dt \tag{16}$$

Taking the Laplace transform of (16), we derive

$$G_{plant}(s) = \frac{i_{cmz}(s)}{3u_{cm}(s)} = \frac{C_f s}{1+LC_f s^2} \tag{17}$$

For simplicity, define the resonance frequency of the added circuit as

$$\omega_{res} = \sqrt{\frac{1}{LC_f}} \tag{18}$$

The diagram in Fig.3 illustrates the continuous-time domain representation of the CMRC control loop, wherein Reg(z) denotes the digital PI controller, and the PWM gain of the inverter is assumed to be equal to unity.

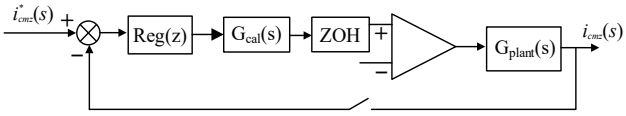


Fig. 3 Model of the CMRC control loop in continuous domain.

When we implement the CMRC controller in the discrete domain, its zero-order hold equivalent, denoted as $G_{cmc}(z)$, can be expressed as follows:

$$\begin{aligned} G_{cmc}(z) &= (1-z^{-1})Z\left\{L^{-1}\left[\frac{G_{plant}(s)}{s}\right]\right\} \\ &= (1-z^{-1})Z\left[\frac{1}{L\omega_{res}}\cdot\frac{\omega_{res}}{s^2+\omega_{res}^2}\right] \\ &= \frac{z-1}{zL\omega_{res}}\cdot\frac{\sin(\omega_{res}T_s)}{z^2-2z\cos(\omega_{res}T_s)+1} \end{aligned} \tag{19}$$

Define H_{i1} and H_{i2} to be

$$\begin{cases} H_{i1} = \sin(\omega_{res}T_s) \\ H_{i2} = \cos(\omega_{res}T_s) \end{cases} \tag{20}$$

(19) can be rewritten as

$$G_{cmc}(z)=\frac{H_{i1}z-H_{i1}}{L\omega_{res}z^2-2L\omega_{res}H_{i2}z+L\omega_{res}} \quad (21)$$

To streamline the analysis, assuming that the integrator has been properly suitably with negligible phase lag. Thus we can simplify the PI controller to a basic proportional gain, denoted as K_p. The allows us to represent the system loop gain $G_{open}(z)$ as follows:

$$G_{open}(z)=z^{-1}K_pG_{cmc}(z)=\frac{K_pH_{i1}z-K_pH_{i1}}{L\omega_{res}z^3-2L\omega_{res}H_{i2}z^2+L\omega_{res}z} \quad (22)$$

The Bode plot for equation (22) is illustrated in Fig. 4, utilizing the parameters detailed in Table I. Notably, its phase curve exhibits a sharp decline at the resonance frequency, reaching a 180° phase shift, while maintaining its magnitude greater than 0 dB. As the switching frequency decreases from 10 kHz to 2 kHz, the phase curve continues to go down, and −180° crossing takes place at the frequency of 2 kHz. Applying the Nyquist stability criterion, it is evident that the system becomes unstable when the phase curve takes a negative crossing at the resonance frequency f_{res}, meaning that the CMRC can no longer be suppressed in the high power application unless the effect of control delay could be mitigated.

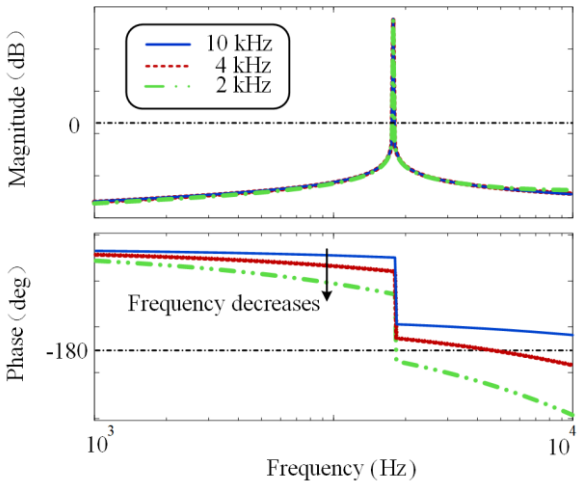


Fig. 4 Bode diagram of the loop gain of conventional CMRC controllers with different switching frequencies.

C. *Proposed delay compensated CMRC suppression method*

Numerous methods for compensating delays have been explored in the previous studies. In [13], a multisampling method is proposed to compensate delays. However, the drawback of the approach is the need for proper filtering of switching noise, which may impair the system stability. Besides, the implementation of multisampling requires additional hardware, limiting the application of the method. In more recent studies, compensation techniques that can be implemented digitally are more favored especially in cost-sensitive applications.

From the above analysis in subsection B, it can be seen that the phase lag induced by the control delay is culprit of the system instability. A simple and intuitive way to cancel out the unfavorable effect of delay is to lift the phase curve to avoid −180° crossing at f_{res}. Therefore, we introduce a digital compensation method that relies on the feedback from the previous step of error to offer a phase lead at the resonance frequency.

The discrete transfer function of this delay compensator, denoted as $W(z)$, is expressed as

$$W(z)=\frac{1+K_c}{1+K_cz^{-1}} \quad (23)$$

Here, K_c represents the compensation coefficient. We can describe the relationship between the compensated modulation signal $m_c(z)$ and the uncompensated modulation signal $m_u(z)$ as follows:

$$\frac{m_c(z)}{m_u(z)}=\frac{1+K_c}{1+K_cz^{-1}}z^{-1} \quad (24)$$

Rearranging (24), the following equation can be yielded as

$$m_c(k)=m_u(k-1)+K_c[m_u(k-1)-m_c(k-1)] \quad (25)$$

in which $m_u(k-1)$, $m_u(k)$, $m_c(k-1)$, and $m_c(k)$ represent the uncompensated modulation signal $m_u(z)$ and compensated signal $m_c(z)$ at (k-1)th and kth step, respectively. From (25), it is clear that the modulation signal compensation can be achieved by using information at the previous step.

To give an intelligible analysis of how the compensator works, we present a graphical representation of the delay compensation effect in Fig. 5. In Fig. 5, the green line represents the uncompensated modulation signal $m_u(k)$, the red line (one step ahead) represents the ideal modulation signal $m_i(k)$, and the blue line represents the compensated modulation signal. When applying the compensator into the control, the value of the modulation signal gets closer to its ideal condition, where the proximity depends on the compensator coefficient K_c.

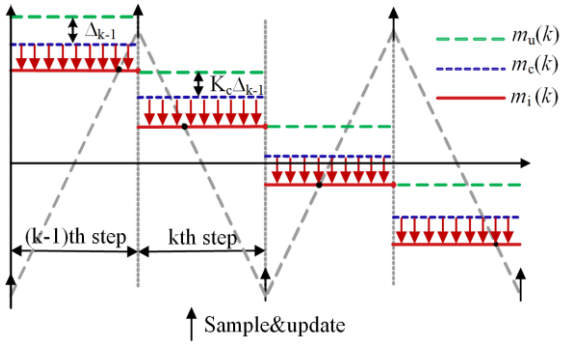


Fig. 5 Graphical illustration of the proposed compensation technique in PWM process.

In other words, the compensation coefficient K_c determines the extent to which the control delay is compensated. The larger the compensator coefficient K_c is, the closer the compensated modulation signal $m_i(k)$ gets to the ideal value, meaning that the better compensation effect of the phase lag can be achieved. However, it is worth noting, as shown in Fig.6, that while a higher coefficient K_c contributes to better compensation effect, it also leads to a lager magnitude for the compensator. When K_c =1, i.e., the critical value, the system becomes prone to noise around specific frequency [11]. Therefore, we select a K_c value lower than 1 to avert the dilemma.

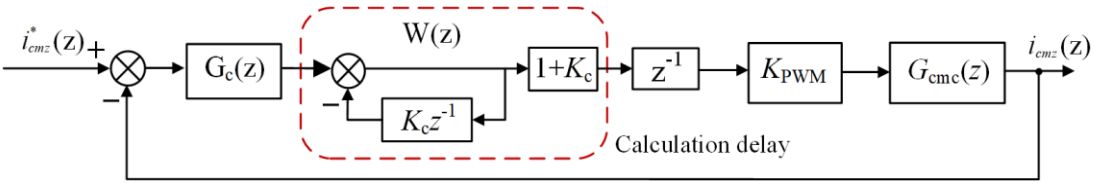


Fig. 7 Model of the DCCMRC control loop in discrete domain.

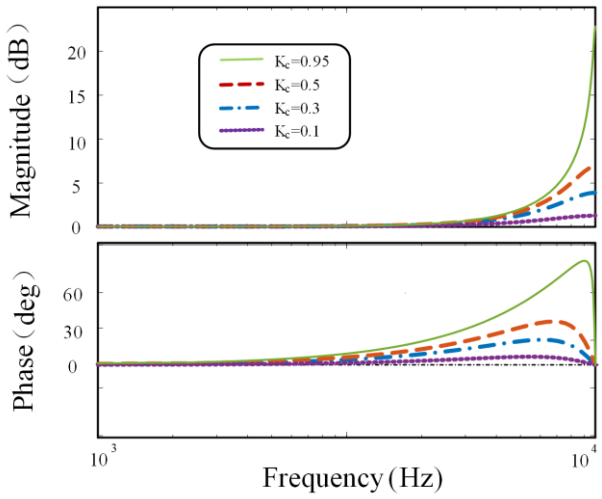


Fig. 6 Bode diagram comparison of different K_c.

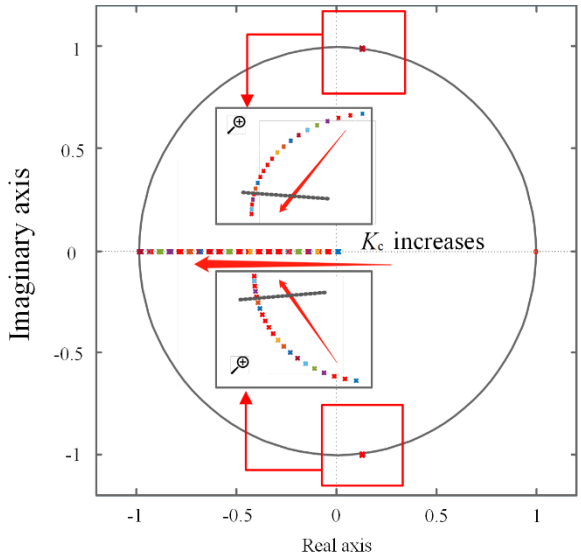


Fig.9 Pole-zero map for the DCCMRC controller with K_c increasing.

D. Stability analysis of the DCCMRC control Strategy

Fig.7 presents the control block diagram of the DCCMRC controller. In order to assess its efficacy in enhancing system stability, we have re-evaluated the open loop transfer function of the DCCMRC controller, as depicted in (26).

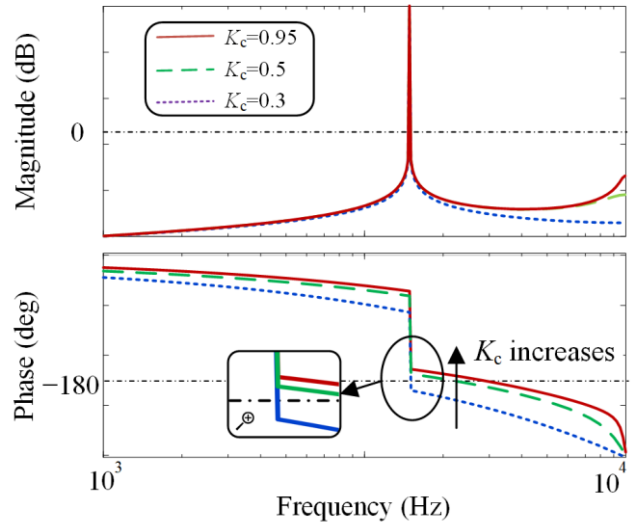


Fig.8 Bode diagram of the DCCMRC controller with different K_c.

Furthermore, Fig. 8 plots the Bode diagram of the DCCMRC controller employing the parameters outlined in Table I. As evident in the diagram, the delay compensator plays a pivotal role in improving system stability difference, and an increase in the compensation coefficient K_c leads to an expansion of the stability region. Notably, with K_c set at 0.95, the system is stable.

To delve deeper into the stability analysis, Fig.9 portrays the root locus of the system. This visualization reveals the evident improvement in system stability performance as the system poles migrate into the region of convergence when K_c increases.

IV. Simulation and Experimental Verifications

A. Simulation Results

Simulations were carried out to prove the efficacy of the redesigned controller, employing the parameters in TABLE I. The simulation outcomes for the grid current, inverter current and leakage current are presented in Fig.10.Within the simulation environment, the switching frequency was configured to 4 kHz, and the compensation coefficient was set to 0.95. Look at the current behavior upon transitioning to non-DCCMRC control mode, it becomes evident that the inverter current exhibits substantial oscillation induced by CMRC, consequently resulting in a deterioration of the grid-connected current and a spike of leakage current.

$$G_{open}(z) = z^{-1}K_pG_{cmc}(z) = \frac{K_pH_{i1}z - K_pH_{i1}}{L\omega_{res}z^3 - 2L\omega_{res}H_{i2}z^2 + L\omega_{res}z} \tag{26}$$

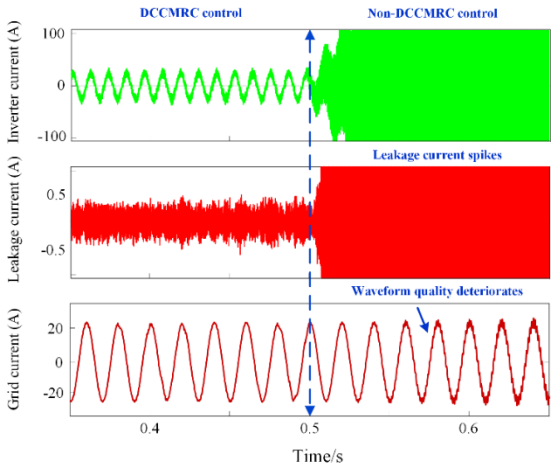


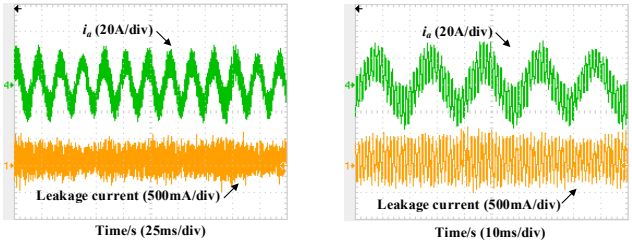
Fig.10 Simulation results of leakage current and grid current.

B. *Experimental Results*

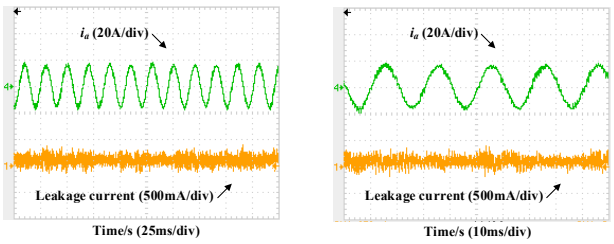
The experimental parameters are listed in TABLE I.

TABLE I. EXPERIMENTAL PARAMETERS

C	1500 μF
C_{PV}	0.15 μF
C_f	10 μF
L	3 mH
L_g	3 mH
T_s	250 μs
V_{dc}	700 V
e_{abc} (Phase-to-phase)	380 V (Peak)
Line resistance	1 Ω



(a)



(b)

Fig. 11. The experimental results of (a) the resonance current and the leakage current without using the DCCMRC control scheme and (b) the output current and the leakage current after using the DCCMRC control scheme.

As shown in Fig.11 (a), For low switching frequency, the conventional method for suppressing the resonance current is invalid, and this leads to a corresponding increase in the leakage current. However, after implementing the proposed DCCMRC controller as shown in Fig.11 (b), the inverter current quality is enhanced with the resonance current largely mitigated, and the leakage current effectively suppressed. In conclusion, the proposed DCCMRC controller demonstrates good performance in terms of resonance current and leakage current suppression at low switching frequencies.

V. CONCLUSION

In this paper, a novel DCCMRC control scheme is introduced tailored for three-level T-type converters with modified *LCL* filter. By delving into the system's stability aspect, the compensation coefficient K_c of the DCCMRC controller is carefully selected. With the proposed scheme, both leakage current and resonance current can effectively be suppressed in high power applications.

REFERENCES

[1] U.M. Choi, H. H. Lee, and K. B. Lee, "Simple neutral-point voltage control for three-level inverters using a discontinuous pulse width modulation," *IEEE Trans. Energy Convers*., vol. 28, no. 2, pp. 434–443, Jun. 2013

[2] C. Liu *et al*., "Leakage Current Suppression of Transformerless 5L-ANPC Inverter With Lower Ripple Model Predictive Control," *IEEE Ind. Appl.*, vol. 58, no. 5, pp. 6297-6309, Sept.-Oct. 2022.

[3] T. K. S. Freddy, N. A. Rahim, W. P. Hew, and H. S. Che, "Modulation techniques to reduce leakage current in three-phase transformerless H7 photovoltaic inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 322– 331, Jan. 2015

[4] C. Morris, D. Han, and B. Sarlioglu, "Reduction of common mode voltage and conducted EMI through three-phase inverter topology," *IEEE Trans. Power Electron*., vol. 32, no. 3, pp. 1720–1724, Mar. 2017

[5] X. Xing, X. Li, F. Gao, C. Qin and C. Zhang, "Improved Space Vector Modulation Technique for Neutral-Point Voltage Oscillation and Common-Mode Voltage Reduction in Three-Level Inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8697-8714, Sept. 2019.

[6] X. Zhu *et al*., "Leakage Current Suppression of Single-Phase Five-Level Inverter for Transformerless Photovoltaic System," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 10422-10435, Nov. 2021.

[7] X. Li, X. Xing, C. Zhang, A. Chen, C. Qin and G. Zhang, "Simultaneous Common-Mode Resonance Circulating Current and Leakage Current Suppression for Transformerless Three-Level T-Type PV Inverter System," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4457-4467, June 2019.

[8] H. Akagi and S. Tamura, "A Passive EMI Filter for Eliminating Both Bearing Current and Ground Leakage Current From an Inverter-Driven Motor," *IEEE Trans. Power Electron*., vol. 21, no. 5, pp. 1459-1469, Sept. 2006.

[9] A. Kouchaki and M. Nymand, "Analytical Design of Passive LCL Filter for Three-Phase Two-Level Power Factor Correction Rectifiers," *IEEE Trans. Power Electron*., vol. 33, no. 4, pp. 3012-3022, April 2018

[10] L. Zhang, K. Sun, Y. Xing and J. Zhao, "Parallel Operation of Modular Single-Phase Transformerless Grid-Tied PV Inverters With Common DC Bus and AC Bus," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 4, pp. 858-869, Dec. 2015.

[11] X. Li, X. Wu, Y. Geng, X. Yuan, C. Xia, and X. Zhang, "Wide damping region for LCL-type grid-connected inverter with an improved capacitor current-feedback method," IEEE Trans. Power Electron., vol. 30, no. 9, pp. 5247–5259, Sep. 2015.

[12] B. S. Buso and P. Mattavelli, "Digital control in power electronics," in Synthesis Lectures on Power Electronics. San Rafael, CA, USA: Morgan& Claypool, 2006.

[13] R. Zhang, C. Zhang, X. Xing, Z. Chen and X. Liu, "Modeling and Control Method to Suppress Common-Mode Resonance Circulating Current for High-Power Parallel Three-Level Inverters System With Improved LCL Filter," in IEEE Transactions on Industrial Electronics, vol. 70, no. 3, pp. 2484-2496, March 2023.