

# Hanzhang Liu

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## EDUCATION

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### University of Electronic Science and Technology of China (UESTC)

Chengdu, China

*B.E., Communication Engineering (Yingcai Honors College)*

*Sep. 17 - Jun. 21 (Expected)*

- **GPA:** 3.98/4.0
- Outstanding Students Scholarship of UESTC (2017-2018, 2018-2019, 2019-2020)
- Selected Courses: Linear Algebra (96), Mathematical Analysis II (94), Physics II (92), Signals and Systems (96), Digital Design and MCU System (89), Digital Signal Processing (93), ACM-ICPC Algorithm and Program Design (90)

## SELECTED PROJECTS

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### Ethereum Token

2020 Spring

*Course: Blockchain Technology: Principles and Applications | Instructor: Prof. Liaoyuan Zeng*

- Wrote and deployed a smart contract
- Published the contract and transacted with others

### Object Detection Methods Implementation

2020 Spring

*Instructor: Prof. Yuming Jia*

- Learned object detection algorithms and implemented YOLOv3 on the COCO dataset

### Dual-frequency Ultrasound Gesture Recognition System

2019 Fall

*Course: Digital Signal Processing (H) | Instructor: Prof. Chang Wu*

- Designed real-time audio processing system that extracted feature sequences from ultrasound based on doppler effect and DSP techniques
- Classified gestures based on kNN
- Implemented the system and demonstrated its applications on sokoban games

### Wireless Video Communication System Based on Software-Defined Radio (SDR)

2019 Fall

*Course: Principle of Communications (H) | Instructor: Prof. Xiaofeng Li*

- Developed an FM stereo receiver
- Built a QPSK-based video communication system on Simulink with SDR. Realized 2.5 fps  $240 \times 160$  resolution 8-bit color video transmission between the fourth floor and the ground
- Implemented video intraframe compression based on discrete cosine transform and run-length encoding
- Explored motion estimation methods
- Formulated a reliable video streaming protocol

### Microprocessor Design

2019 Spring

*Course: Digital Design and MCU System (H) | Instructor: Prof. Jianhao Hu*

- Developed a 4-issue, 6-stage pipelined microprocessor that performed sorting and matrix multiplication algorithm. It passed FPGA verification at 125MHz clock frequency
- Designed a vectorized sorting algorithm suitable for superscalar microarchitecture
- Created a compact instruction set
- Designed the datapath and control unit and coped with hazards

## TECHNICAL SKILLS

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**Languages:** C, C++, Python, Matlab, Verilog, Assembly (MIPS)

**Tools:** Git, L<sup>A</sup>T<sub>E</sub>X

**Libraries & Frameworks:** pandas, NumPy, Matplotlib, PyTorch, OpenCV