Ice Lithography for Nanodevices

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ABSTRACT We report the successful application of a new approach, ice lithography (IL), to fabricate nanoscale devices. The entire IL process takes place inside a modified scanning electron microscope (SEM), where a vapor-deposited film of water ice serves as a resist for e-beam lithography, greatly simplifying and streamlining device fabrication. We show that labile nanostructures such as carbon nanotubes can be safely imaged in an SEM when coated in ice. The ice film is patterned at high e-beam intensity and serves as a mask for lift-off without the device degradation and contamination associated with e-beam imaging and polymer resist residues. We demonstrate the IL preparation of carbon nanotube field effect transistors with high-quality trans-conductance properties.

KEYWORDS Carbon nanotube, e-beam lithography, nanodevice, field effect transistor

I t was recently shown that water ice can serve as a resist during high-resolution e-beam lithography,[1] easily achieving sub-10-nm features. The special properties of water ice allow direct application in a vacuum environment, conformal coating of complex three-dimensional structures, through-resist mapping and registration of nanostructures, and simple, contamination-free removal. Here we demonstrate that high-quality carbon nanotube FETs can be fabricated with ice lithography.

We extensively modified a field emission scanning and e-beam writing electron microscope (SEM) for device fabrication using IL (Figure 1). On the basis of our previous work fabricating sub-20-nm-wide metal lines by nanopatterning ice,[1] our new instrument is a cluster tool that allows the entire IL process to be effected and examined within one vacuum system.[2] A sample containing the desired nanodevice elements is first cooled to cryogenic temperatures in the microscope vacuum (for detailed methods, see Supporting Information). Our sample consists of single-walled carbon nanotubes (SWCNTs) grown by chemical vapor deposition (CVD) from an iron catalyst pad.[3,4] When cooled to ∼110 K the sample is exposed to water vapor from a gas injection system. A thin, conformal layer of amorphous ice, several tens of nanometers thick, forms on the surface of the sample. The nanotubes are then located by imaging through the ice layer with a low intensity e-beam. As shown below, typical damage and contamination associated with direct e-beam exposure are eliminated when imaging through ice. The ice resist is then appropriately patterned relative to the underlying nanostructures with a high intensity e-beam guided by an e-beam writing system built into the SEM. The patterning removes ice from those regions where metallic contacts are desired. The cold sample is then rapidly trans-ferred through the vacuum onto a second cryostage located in a specially designed metal deposition chamber that had been incorporated onto the SEM. Here, metal films are plasma sputter-deposited onto the ice patterned sample surface. Two different metals can be deposited, including an adhesion layer which is critical for noble metal adhesion onto dielectric surfaces. Finally, the device is removed from the metal deposition chamber and immersed into 2-propanol, which lifts off the metal where no ice had been removed. Thus, the standard processes of mapping SWCNT, poly(methyl methacrylate) (PMMA) resist spinning, resist baking, e-beam exposure, development, and metal evaporation, which normally use six different instruments, are accomplished using the IL process in one instrument.

To electrically connect a CVD grown SWCNT to a pre-existing metal contact pad, the first step is to locate a SWCNT and map its position on the device substrate surface.

Figure 2 demonstrates that all SWCNTs visible in an AFM image can also be visualized through ice with the SEM. It normally takes 4 h to image and map a 50×50 μm area with an AFM. We can easily map this area through ice in the SEM in just a few minutes. The e-beam dose used for imaging is 4 orders of magnitude smaller than that required for actual patterning, so no significant ice removal occurs during imaging. Aside from the time saving aspects of in situ SEM imaging, e-beam damage and contamination[5] that have previously limited the usefulness of SEM mapping are avoided (see below).

Contrast for imaging SWCNT in the SEM is the result of dynamic charging of insulating layers by the incident e-beam.[6−9] Here, the underlying SiO_2 back gate insulator and the amorphous ice serve as the charged insulator layer, whereas the conducting SWCNTs are electrically grounded through the iron catalyst pad from which they grow. The insulating layers become negatively charged by exposure to the primary e-beam, and the SWCNT remains at ground potential. Consequently, low-energy secondary electrons
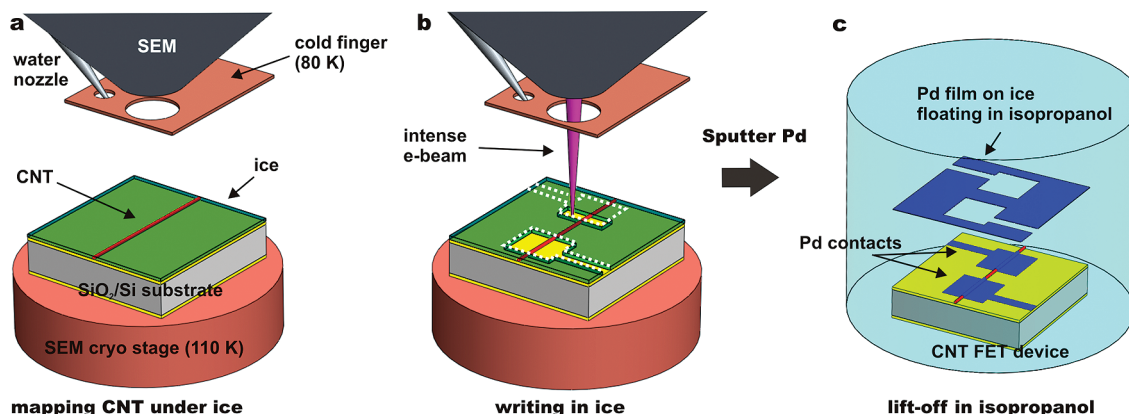
FIGURE 1. IL process. (a) The sample with preformed Mo microleads and SWCNT on the SiO_2-coated Si substrate is loaded into the SEM via the load-lock and cooled down to ~110 K on the SEM cryo-stage. Water vapor is leaked into the SEM through a nozzle just above the sample and condenses as amorphous ice on the cold sample. Typically, 80 nm of ice is deposited in 30 s. The location of a SWCNT under the ice is mapped. (b) An intense e-beam draws patterns for the contacts (white dotted line) and removes ice, forming a mask for metal electrodes contacting the SWCNT. (c) The sample with nanopatterned ice resist is transferred onto the metal deposition chamber, and Pd is sputtered over the entire sample. The sample is removed from the metal deposition chamber and, while still frozen, immediately immersed into 2-propanol held at room temperature, whereupon the Pd film on top of the ice resist drifts away, leaving the preformed Mo leads connected to the SWCNT with Pd interconnections only where the ice had been removed by the e-beam.
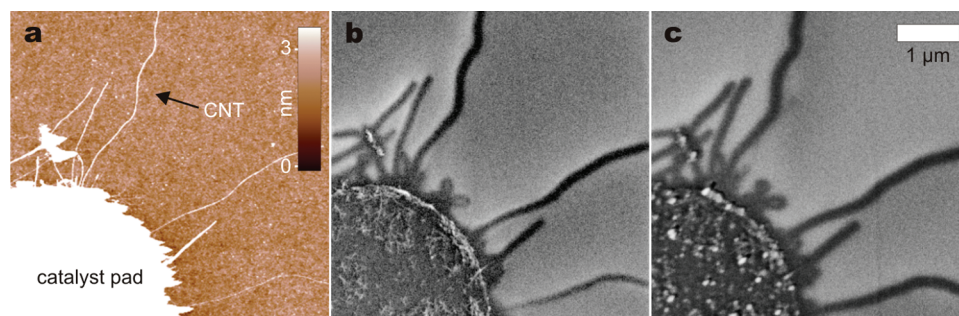

FIGURE 2. Imaging CVD SWCNT through ice on 300 nm thick SiO_2-coated Si substrates. (a) Tapping mode AFM image of nanotubes grown from a catalyst pad on a grounded lead. (b) SEM image of same area as in (a) with sample at ~110 K before ice deposition (primary beam energy 2 keV; probe current 17 pA). (c) As in (b), but SEM imaged after deposition of a 25 nm ice layer (primary beam energy, 1.35 keV; probe current, 20 pA).

emitted near the nanotube are collected by the nanotube rather than the microscope's secondary electron detector. This visibly distinguishes the nanotubes as dark lines (Figure 2). Note that the image of the nanotube diameter can be much greater than its geometrical diameter, enabling even low-resolution microscopes to image carbon nanotubes. Imaging the SWCNT through a thin dielectric layer can also be used as a noninvasive method for rapid quality control of the electrical integrity of nanodevices after dielectric coating and passivation.

The next step of IL is patterned ice removal to form the mask for metal deposition.[1] Guided by the SEM image of the nanotubes, the e-beam patterning system selectively removes ice to form the designed mask (Figure 1b). At 20 kV e-beam energy, typically a dose of 1 C/cm^2 is required to remove 80 nm thick ice. After the writing process, the sample can be immediately imaged again, at low SEM beam intensity to inspect the writing quality. Such inspection, which is not possible with standard lithography, provides a valuable opportunity to make minor corrections or abort further processing.

The patterned sample is next transferred onto the metal deposition cryostage held at 165 K. At this temperature, 14 nm of ice sublimes in 1 min. Five nanometers of ice is allowed to sublime from the entire sample surface to ensure that any remaining ice at the bottom of the patterned mask wells is removed before depositing metals, and lift-off is finally carried out in 2-propanol (Figure 1c).

Two methods were used to evaluate e-beam induced defects or contaminants on the finished device. First, tapping mode AFM was used to inspect and compare SWCNT−metal nanostructures made by IL versus standard e-beam lithography using a PMMA resist (Figure 3a−e). Following IL, the root-mean-square surface roughness of the device surfaces barely increases from its initial value of 0.25−0.27 nm to a value of 0.31 nm. This small increase in surface roughness using IL contrasts with the much greater increase to 0.81 nm after using a standard PMMA resist. Second, we tested the ability of free-standing nanotubes to nucleate the growth of Al_2O_3 during atomic layer deposition (ALD) of Al_2O_3 on the entire sample. Pristine, defect-free nanotubes do not nucleate the growth of Al_2O_3 whereas contaminants or SEM-
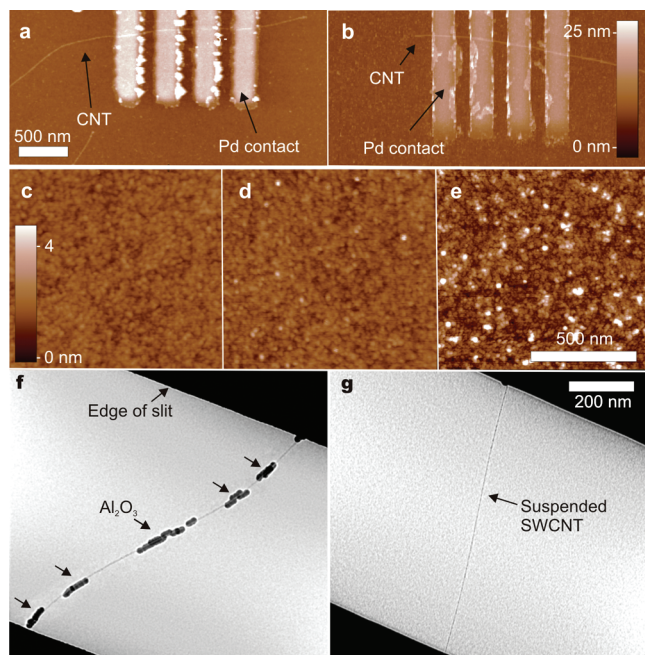
FIGURE 3. Detecting contaminants and e-beam damage. Tapping mode AFM images of SWCNT contacted by four 200-nm-wide Pd electrodes using (a) IL or (b) standard lithography using PMMA resist. (c−e) High magnification AFM of (c) clean chips before the contacting process (RMSSR = 0.25−0.27 nm), (d) after IL (RMSSR = 0.31 nm), and (e) after PMMA lithography (RMSSR = 0.81 nm). All samples on identical Si_3N_4 surfaces. (f) Transmission electron microscopy image of a typical CVD SWCNT suspended across 750-nm-wide slits in a Si_3N_4 membrane that was SEM imaged at room temperature prior to ALD of 11 nm of Al_2O_3. (g) Image of a representative SWCNT after ALD, under identical conditions as in (f) except that it was protected with a 120 nm layer of ice prior to SEM imaging.

induced damage sites do.[10−12] Panels f and g of Figure 3 show an example of how free-standing, unprotected nanotubes imaged by SEM do nucleate Al_2O_3 growth, while those imaged through ice do not. Thus, IL can produce devices that remain free of processing residues and e-beam induced defects.

Electrical measurements under ambient room temperature conditions showed that the SWCNTs contacted by IL contained both semiconducting and metallic tubes at a ratio of 2:1, as commonly observed for CVD grown tubes. Examples of the electrical responses of a metallic and a semiconducting SWCNT FET produced on Si_3N_4 are shown in Figure 4. While sweeping the back-gate bias from −10 to 10 V, the semiconducting tube switches to its ON state at a negative gate bias, indicating hole conduction,[13] while the metallic tube did not show a significant back gate response. The hysteresis commonly observed in ambient conditions for conventionally made SWCNT FETs[14] is noted.

Because it is known that metal films deposited onto cold surfaces tend to be nanoporous,[15] we were concerned that the metal contacts and leads formed on cold device structures by IL would not be of the highest electrical quality. We compared IL fabricated devices with more conventionally
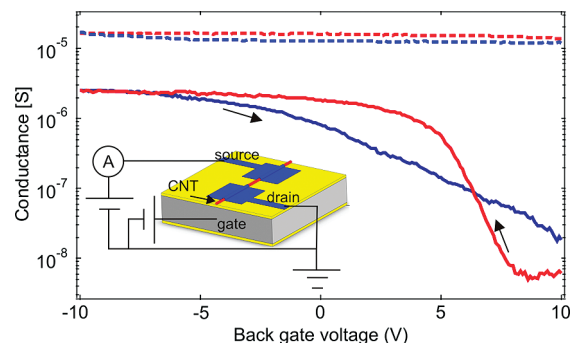

FIGURE 4. Conductance measurement in ambient conditions of two SWCNT FETs made by IL. Si substrates coated with 500 nm of SiO_2 and 60 nm of Si_3N_4. Lower left corner illustrates the measurement setup. Keeping the source−drain voltage over the SWCNT constant at 10 mV, the gate voltage was swept at 5 V/min from −10 to 10 V (blue) and back from 10 to −10 V (red). Arrows indicate sweep direction. Dotted lines show a 60 kΩ metallic tube after annealing at 300 °C. The solid lines show a semiconducting tube after annealing at 600 °C. The ON resistance is 380 kΩ.

fabricated nanotube devices on SiO_2 coated Si. Each 10-nm-thick source and drain Pd electrode covered a 0.8 μm long segment of the SWCNT, with 2 μm between the two electrodes. The IL-made SWCNT FET source−drain resistances (R_{sd}) ranged between 0.33 and 16 MΩ, significantly higher than the R_{sd} of ∼50 kΩ for metallic FETs we fabricated using conventional e-beam lithography with PMMA resist (results not shown). But straightforward annealing of IL samples in an Ar atmosphere at temperatures ranging from 300 to 600 °C reduced the IL FET R_{sd} by more than 10-fold and yielded contacts whose R_{sd} values were comparable to those obtained using standard resist based e-beam lithography: metallic FET devices with R_{sd} between 60 and 90 kΩ, and semiconducting tubes with R_{sd} down to 100 kΩ. We attribute the improved contacts to high-temperature densification of the cold-deposited Pd contacts.

Our results demonstrate a new approach to nanodevice fabrication that solves several problems often faced in designing and producing devices. We foresee that IL could also be used to pattern high-purity metal onto three-dimensional structures. Automation and scaling up are also feasible. We anticipate that IL can be incorporated into more complex cluster tool environments for making graphene nanoribbons and nanopore devices.[16]

Supporting Information Available. Detailed description of sample preparation and IL process. This material is available free of charge via the Internet at http://pubs.acs.org.

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