SPECTRUM DIGITAL INCORPORATED

TMS320DM6437 Evaluation Module

Technical Reference

2007 ***DSP Development Systems***

TMS320DM6437 Evaluation Module Technical Reference

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Contents

About This Manual

This document describes the board level operations of the DM6437 Evaluation Module (EVM). The EVM is based on the Texas Instruments TMS320DM6437 Processor.

The DM6437 Evaluation Module is a table top card that allows engineers and software developers to evaluate certain characteristics of the DM6437 processor to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The DM6437 Evaluation Module will sometimes be referred to as the DM6437 EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents, Application Notes and User Guides

Information regarding this device can be found at the following Texas Instruments website:

http://www.ti.com

Table 1: Manual History

Revision	History
A	Alpha Release
B	Beta Release
C	Gamma Release
D	Production Release

Table 2: Board History

PWB Revision	History
A	Alpha Release
B	Beta Release
C	Gamma Release
D	Production Release - Ethernet Straps, Fuse added

Chapter 1

Introduction to the DM6437 EVM

Chapter One provides a description of the DM6437 EVM along with the key features and a block diagram of the circuit board.

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1.1 Key Features

The DM6437 EVM is a PCI based or standalone development platform that enables users to evaluate and develop applications for the TI DaVinci™ processor family. Schematics, list of materials, and application notes are available to ease hardware development and reduce time to market.

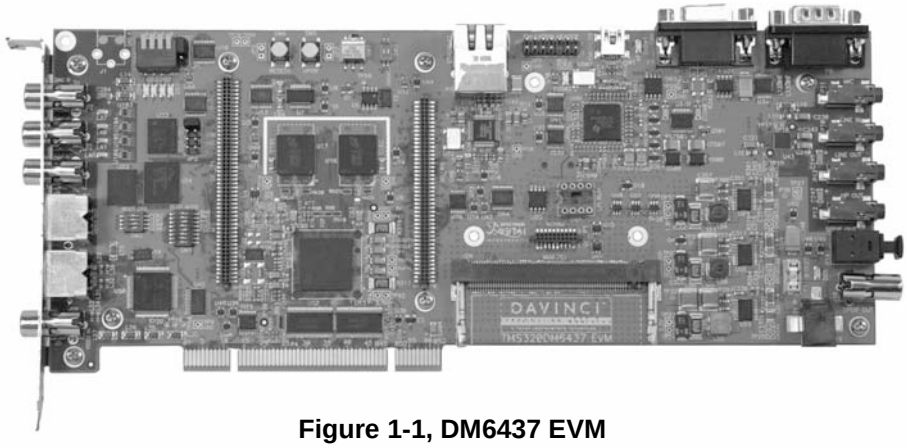

Figure 1-1, DM6437 EVM

The EVM comes with a full complement of on board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments DM6437 processor operating up to 600 Mhz.
- 1 TVP5146M2 video decoder, supports composite or S video
- 4 video DAC outputs - component, RGB, composite (3 populated)
- 128 Mbytes of DDR2 DRAM
- UART, CAN I/O Interfaces
- 16 Mbytes of non-volatile Flash memory, 64 Mbytes NAND Flash, 2 Mbytes SRAM
- AIC33 stereo codec
- I^2C Interface with onboard eeprom and expanders
- 10/100 MBS Ethernet Interface
- Configurable boot load options
- Embedded JTAG emulation interface
- 4 user LEDs and 4 position user switch

- Single voltage power supply (+5V)
- Expansion connectors for daughter card use
- VLYNQ Interface
- S/PDIF Interface, analog, and optical

1.2 Functional Overview of the DM6437 EVM

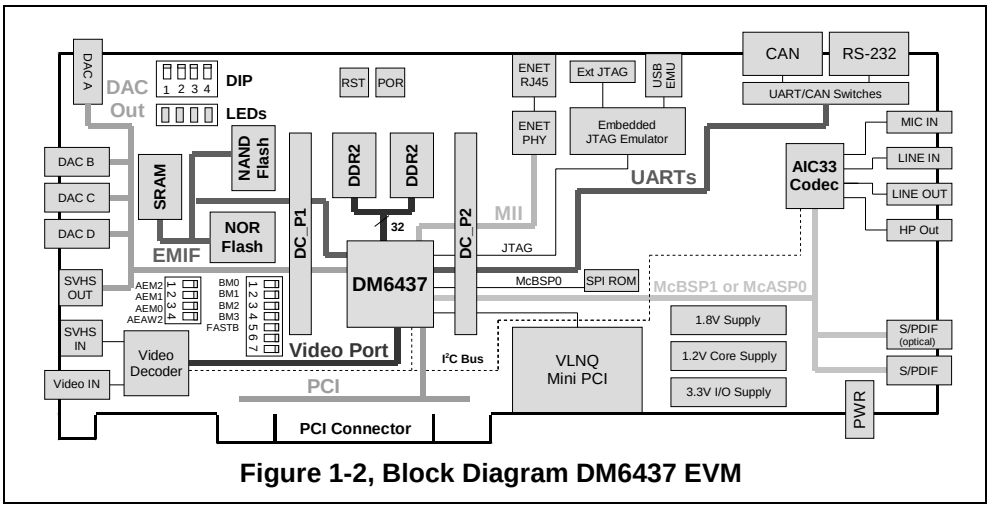

Figure 1-2, Block Diagram DM6437 EVM

The DM6437 on the EVM interfaces to on-board peripherals through integrated device interfaces and a 8-bit wide EMIF bus. The DDR2 memory is connected to its own dedicated 32 bit wide bus. The EMIF bus is jumper selectable to be connected to the Flash, SRAM, NAND, and daughter card expansion connectors which are used for add-on boards.

On board video decoder and on chip encoders interface video streams to the DM6437 processor. One TVP5146M2 decoder and 4 on chip DAC channels are standard on the EVM (only 3 output connectors are populated so that the board can fit in a PCI slot). On screen display functions are implemented in software on the DM6437 processor.

An on-board AIC33 codec allows the DSP to transmit and receive analog audio signals. The I^2C bus is used for the codec control interface, while the McBSP controls the audio stream. Signal interfacing is done through 3.5mm audio jacks that correspond to microphone input, line input, line output, and headphone outputs.

The EVM includes 4 user LEDs, and 4 position user DIP switch which can be used to provide the user with interactive feedback. These interfaces are implemented via I^2C expanders.

VLYNQ, and ethernet MAC interfaces are integrated peripherals on the DM6437 processor exploiting its system on a chip architecture. VLYNQ is available when the PCI is not used.

An included 5V external power supply is used to power the board. On-board switching voltage regulators provide the +1.2V CPU core voltage and +3.3V for peripherals and +1.8V DDR2 memory. The board is held in reset until these supplies are within operating specifications.

Code Composer communicates with the EVM through an embedded emulator or via the 14 pin external JTAG connector.

1.3 Basic Operation

The EVM is designed to work with TI's Code Composer Studio development. Code Composer communicates with the board through the embedded emulator or an external JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

Detailed information about the EVM including examples and reference material is available on the EVM's CD-ROM.

1.4 Memory Map

The DaVinci family of processors have a large byte addressable address space, some limitations to byte addressing are determined by peripheral interconnection to the DM6437 device. Program code and data can be placed anywhere in the unified address space. Addresses are multiple sizes depending on hardware implementation. Refer to the appropriate device data sheets for more details.

The memory map shows the address space of a DM6437 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

The part incorporates a dual EMIF interface. One dedicated EMIF directly interfaces to the DDR2 memory. The Flash, NAND Flash, or SRAM are mapped into CS2 space and selectable via JP2. When CS2 is used for daughter card interfacing JP2 must be set appropriately.

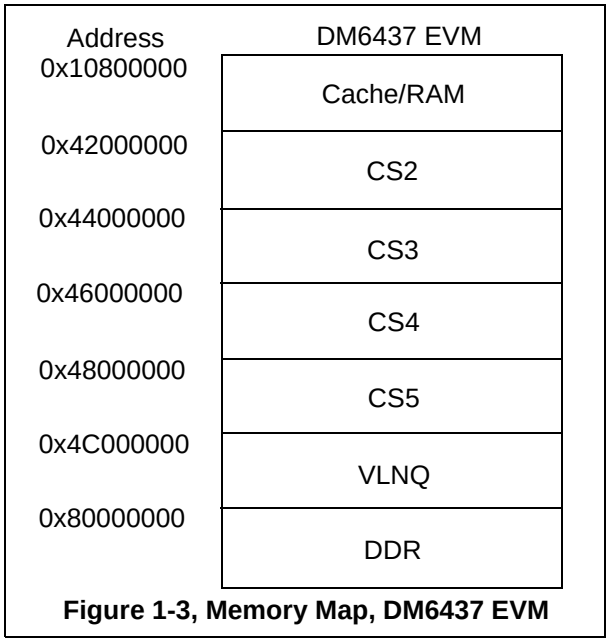

Figure 1-3, Memory Map, DM6437 EVM

1.5 Configuration Switch Settings

The EVM has a two configuration switches that allow users to control the operational state of the processor when it is released from reset. The configuration switches are labeled SW1 and SW2 on the EVM board.

Switch SW1 configures the boot mode that will be used when the DSP starts executing. By default the switches are configured to EMIF boot (out of 8-bit Flash). The DM6437 EVM only supports little endian mode and is not configurable. Refer to section 3.5.1 for the boot load options using switch SW1.

1.6 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J16), a 2.5 MM. barrel-type plug. Internally, the +5V input is converted into +1.2V, +1.8V and +3.3V using Texas Instruments swift voltage regulators. The +1.2V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and other chips on the board. The +1.8 volt supply is used for DM6437 DDR2 interface, and DDR2 memory.

There are three power test points on the EVM; TP23, TP34, and TP38. These test points provide a convenient mechanism to check the EVM's multiple power supplies. The table below shows the voltages for each test point and what the supply is used for.

Table 1: Power Test Points

Test Point	Voltage	Voltage Use
TP23	+1.2 V	DM6437 Core
TP34	+3.3V	DSP I/O and logic
TP38	+1.8 V	DDR2 Memory, DSP I/O, and logic

1.7 Power Measurement

The EVM supports power test points to allow measurement of the various power rails on the DM6437 device. Series resistors are used in the device's power domains thereby measuring the voltage across these resistors. The current can be calculated via V = I * R.

Refer to the test point section in chapter 3 for detailed information on measuring current on the DM6437 device.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the DM6437 EVM.

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2.1 EMIF Interfaces

A separate 8 bit EMIF with multiple chip selects divide up the address space and allow for asynchronous accesses on the EVM. On board the CS2 is used for Flash, NAND Flash, or SRAM.

2.1.1 DDR2 Memory Interface

The DM6437 device incorporates a dedicated 32 bit wide DDR2 memory bus. The EVM uses two 512 megabit 16 bit wide memories on this bus, for a total of 128 megabytes of memory for program, data, and video storage. The internal DDR controller uses a PLL to control the DDR memory timing. The interface supports rates up to 166 Mhz., and is clocked on differential edges for optimal performance. Memory refresh for DDR2 is handled automatically by the DM6437 internal DDR controller.

2.1.2 Flash, NAND Flash, SRAM Memory Interface

The DM6437 has 16 megabytes of NOR Flash, or 64 megabytes of NAND Flash, or 2 megabyte of SRAM memory mapped into the CS2 space. This NOR Flash memory, and NAND Flash memory are used primarily for boot loading. SRAM is used for debugging application code. The CS2 space is configured as 8 bits wide on the DM6437 EVM for NOR Flash, SRAM, or NAND flash usage.

2.2 Peripheral Interfaces

The DM6437 has several peripheral interfaces which allow the user to interface to external devices. These interfaces are outlined in the following sections.

2.2.1 VLYNQ Interface

The DM6437 brings its internal VLYNQ interface out to a mini PCI connector J20 and small 20 pin connector DC_P3. The VLYNQ interface is multiplexed on the PCI/EM bus and this bus must be reconfigured after boot up to support VLYNQ. A multiplexer is used to minimize board layout stubs and allow as direct as possible interface for the VLYNQ signals. VLYNQ is not operational if the board is used in a PCI slot.

2.2.2 UART Interface

The internal UART0 on the DM6437 device is driven to connector P8. The UART's interface is routed to a Texas Instruments MAX3221 RS-232 line driver prior to being brought out to a male DB-9 connector, P8. The on board UART signals can be disabled by pulling the RS232_ENABLEn signal high via the daughter card connectors.

2.2.3 CAN Interface

The internal CAN controller on the DM6437 device is driven to connector P7. The controller is routed to a Texas Instruments SN65HVD235 CAN controller prior to being routed to female DB-9 connector, P7. The on board CAN signals can be disabled by pulling CAN_ENABLEn high via the daughter card connector.

2.3 Video Interfaces

The DM6437 EVM has video input and output ports to support a variety of user applications. These are discussed in the two sections below.

2.3.1 Input Video Port Interfaces

The DM6437 EVM supports video capture via the devices internal video ports. A Texas Instruments TVP5146M2 is used to decode composite video or S-video inputs into the device. P2 is used for the S-video inputs and J5 for the composite inputs on the EVM.

User inputs can be driven via daughter card connector DC_P1 when the on board CBTs are disabled by driving control TVP5146_ENABLEn signal high on DC_P1.

2.3.2 On Chip Video Output DACs

The DM6437 incorporates 4 output DACs to interface to various output standards. The DACs are buffered via opamps and driven to four RCA jacks, J1-J4. The outputs of the DACs are programmable to support composite video, component video, or RGB.

S-video output is available from connector P1. This connector is driven by video DACs B and C from the DM6437. Video DAC B is the chroma and video DAC C is the luma.

2.4 AIC33 Interface

The EVM uses a Texas Instruments TLV320AIC33 stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line output so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I^2C bus is used as the unidirectional control channel. The control channel is generally only used when configuring the codec, it is typically idle when audio data is being transmitted,

The default configuration is to use the McBSP as the bi-directional data channel. However, optionally the McASP can be used to drive the data channel. Data channel selection is controller via an on board I^2C expander. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side.

The codec has a programmable clock from a PLL1705 PLL device. The default system clock is 22.5792 Mhz. The internal sample rate generate subdivides the 22.5792 MHz clock to generate common frequencies. The sample rate is set by a codec register. The figure below shows the codec interface on the DM6437 EVM.

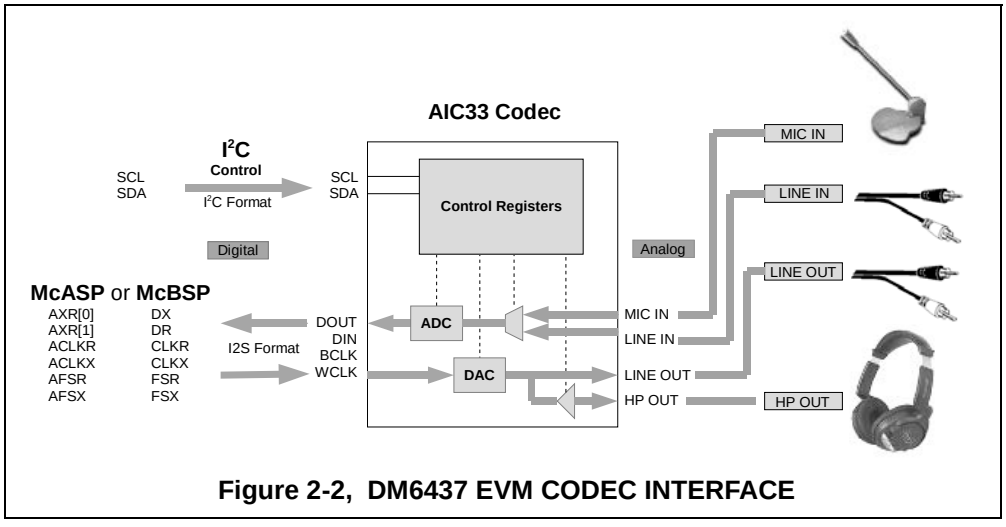

Figure 2-2, DM6437 EVM CODEC INTERFACE

2.4.1 Audio PLL/VCXO Circuit/PLL1705 Clock Generator

The DM6437 EVM implements a multiple PLL clock generator for creating the Audio clocks for the board.

In streaming video applications the audio and video sequences can lose synchronization. The DM6437 uses a VCXO interpolation circuit to incrementally speed up or slow down the STCLK input to allow for this synchronization to remain locked.

The PWM1 and timer inputs on DM6437 are used to control this feature. The PWM0 pin drives a PICX100-27W Voltage Controlled Oscillator which is and fed back into the timer input pin.

The STCLK is also a source clock for the PLL1705 programmable PLL device. This device creates the clocks for the AIC33 Codec, daughter card VIDCLK an AUDIOCLK.

The PLL1705 is programmable via an I^2C and Expander U13. Software sequencing on the I/O expander is required to interface correctly to the PLL1705's programmable inputs.

The diagram below is a simplified diagram of this clocking scheme.

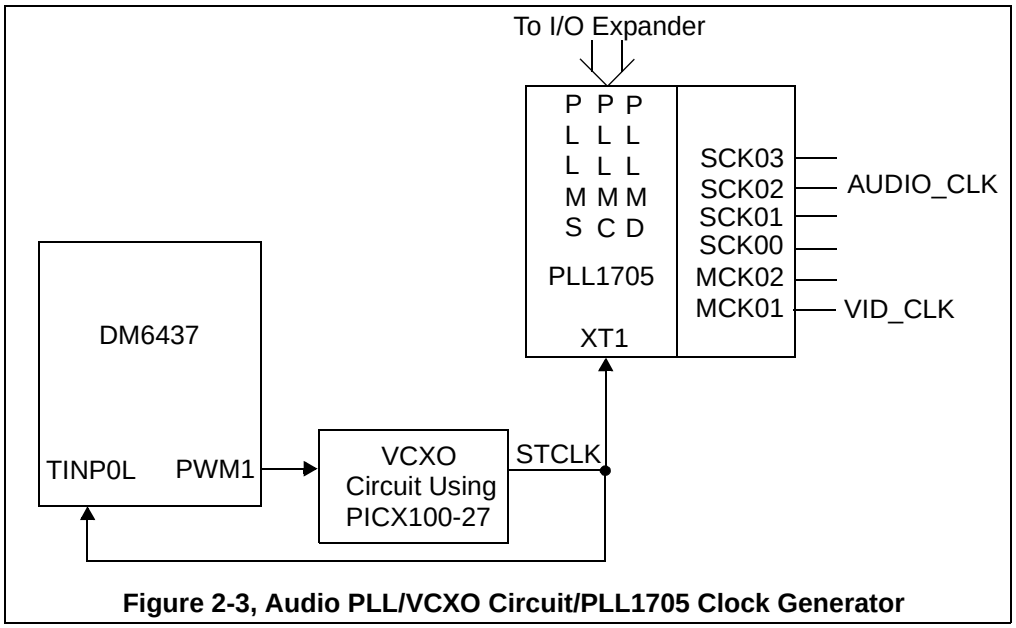

Figure 2-3, Audio PLL/VCXO Circuit/PLL1705 Clock Generator

2.5 Ethernet Interface

The DM6437 integrates an ethernet MAC on chip. This interface is routed to the PHY via CBT switches. The EVM uses an Micrel KS8001L PHY. The 10/100 Mbit interface is isolated and brought out to a RJ-45 standard ethernet connector, P3. The PHY directly interfaces to the DM6437. The ethernet address is stored in the I^2C serial ROM during manufacturing.

The RJ-45 has 2 LEDs integrated into its connector. The LEDs are green and yellow and indicate the status of the ethernet link. The green LED, when on, indicates link and when blinking indicates link activity. The yellow LED, when illuminated, indicates full duplex mode.

2.6 I^2C Interface

The I^2C bus on the DM6437 is ideal for interfacing to the control registers of many devices. On the DM6437 EVM the I^2C bus is used to configure the video decoder, stereo Codec, I/O expanders. An I^2C ROM is also interfaced via the serial bus. The format of the bus is shown in the figure below.

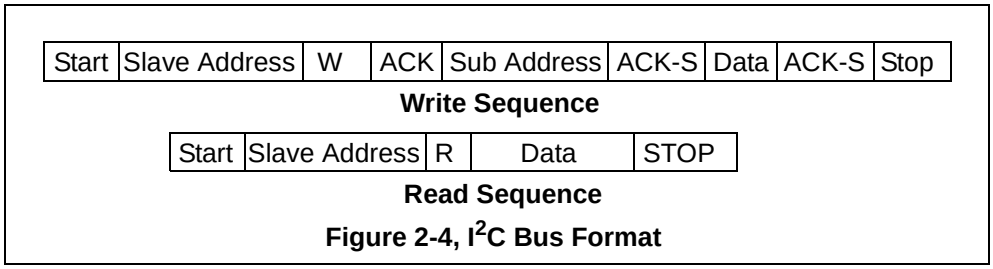

Figure 2-4, I^2C Bus Format

The addresses of the on board peripherals are shown in the table below.

Table 1: I^2C Memory Map

Device	Address	R/W	Device	Function
TVP5146M2	0x5D	R/W	U50	Video Decoder
PCF 8574A	0x38	R/W	U10	User Input
PCF 8574A	0x39	R/W	U11	User LEDs
PCF 8574A	0x3A	R/W	U13	PLL, User I/O
PCF8574A	0x3B	R/W	U64	User I/O
TLV320AIC33	0x1B	R/W	U43	CODEC
24WC256	0x50	R/W	U25	I^2C EEPROM

2.6.1 I/O Expanders

The DM6437 EVM uses four I^2C expanders to handle various bit I/O functions. Each of these is an 8 bit I/O expander, a PCF8574A. At Power Up Reset the expanders are initialized to 0xFF, all ones. The functions for each of the I/O expanders are shown in the tables below.

Table 2: U10 I/O Expander

Pin Number	Function	Description
P0	JP1 NTSC/PAL Select	Read only video mode,1=NTSC,0=PAL
P1	SW7 Slide Switch	Read only slide switch
P2	Reserved	None
P3	Reserved	None
P4	SW4-0	Read only user switch
P5	SW4-1	Read only user switch
P6	SW4-2	Read only user switch
P7	SW4-3	Read only user switch

Table 3: U11 I/O Expander

Pin Number	Function	Description
P0	User LED DS1	0=Turns LED on, 1=Turns LED off
P1	User LED DS2	0=Turns LED on, 1=Turns LED off
P2	User LED DS3	0=Turns LED on, 1=Turns LED off
P3	User LED DS4	0=Turns LED on, 1=Turns LED off
P4	VLYNQ Reset	0=Removes Reset, 1=Applies Reset
P5	Reserved	None
P6	User I/O DC_P2	To daughter card, DC_P2 Pin 81
P7	User I/O DC_P2	To daughter card, DC_P2 Pin 82

Table 4: U13 I/O Expander

Pin Number	Function	Mode	Description
P0	User I/O	RW	Daughter Card, DC_P2 Pin 87
P1	User I/O	RW	Daughter Card, DC_P2 Pin 88
P2	User I/O	RW	Daughter Card, DC_P2 Pin 85
P3	User I/O	RW	Daughter Card, DC_P2 Pin 84
P4	PLL -SR	W	Write PLL1705 SR Pin
P5	PLL - FS2	W	Write PLL1705 FS2 Pin
P6	PLL - FS1	W	Write PLL1705 FS1 Pin
P7	PLL-CSEL	W	Write PLL1705 CSEL Pin

Table 5: U64 I/O Expander

Pin Number	Function	Description
P0	McBSP_Enable to AIC23	***** 1=Enable, 0=Disable
P1	McASP_Enable to AIC23	***** 0=Enable, 1=Disable
P2	SPDIF Enable	***** 0=Enable, 1=Disable
P3	Reserved	None
P4	Reserved	None
P5	Reserved	None
P6	Reserved	None
P7	Core Voltage Select	0 = 1.05 Volt, 1 = 1.2 Volt

***** only one should be enabled at a time

2.6.2 I²C EEPROM

The DM7436 EVM incorporates an I²C eeprom that can be used for booting or general purpose storage.

This eeprom is also used to store the ethernet MAC address and the board's revision. The MAC address is also labeled on the board. Care should be taken not to erase these items when user information is stored in the eeprom. Spectrum Digital uses addresses 0x7F00 to 0x7FFF for manufacturing information. This information is shown in the table below.

Table 6: DM6437 MAC Addresses

Address	Contents
0x7F00	EMAC Address 0 (most significant)
0x7F01	EMAC Address 1
0x7F02	EMAC Address 2
0x7F03	EMAC Address 3
0x7F04	EMAC Address 4
0x7F05	EMAC Address 5
0x7F06	Reserved
0x7F07	Board Revision

2.7 S/PDIF Analog, and Optical Interfaces

The McBSP's FSR pin on the DM6437 can be configured to operate as a S/PDIF transmitter. The DM6437 EVM supports both analog and optical interfaces. The analog S/PDIF output pin is routed to a driver and filter circuit before being output on J10. I²C Expander U64 output P2 is used to enable the S/PDIF interface. When S/PDIF is selected on the expander (P2=0), the McASP enable should be disabled and the McBSP enable should be disabled.Another driver is used to interface the optical transmitter P14. When the S/PDIF interface is enabled the TLV320AIC33 codec is disabled, the WCLK should be disabled prior to enabling the S/PDIF output.

The McBSP interface can be disabled for daughter card use by pulling the AIC_ENABLEn signal high from the daughter card connector.

2.8 Daughter Card Interfaces

The EVM provides expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their EVM platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for all major interfaces including memory, peripherals, and video expansion.

The pin outs for this interface are documented in Section 3.

The connectors provide access to the DSP's EMIF signals to interface with memories and memory mapped devices. The video capture port is brought out to the daughter card interface.

Several signals are used to disable the on board video peripherals so that they can be used by the expansion connector. The table below indicates the operation of these signals.

Table 7: Daughter Card Interface

Signal	Function
AIC33_ENABLEn	Disconnects CPU from on board codec
CI_EMA_ENABLEn	Disables CI0 to CI7 from upper on board EMIF address lines
MEM_EMD7-0_ENABLEn	Disables CPU from on board data bus
VIC_TINPOL_ENABLEn	Disable CPU TINPOL pin from on board use
ENET_ENABLEn	Disconnects CPU from on board ethernet PHY
CAN_ENABLEn	Disconnects CPU from on board CAN
RS232_ENABLEn	Disconnects CPU from on board UART
TVP5146_ENABLEn	Disconnects CPU from on board video decoder

Other than the buffering, most daughter card signals are not modified on the board.

2.9 DM6437 Core CPU Clock

The DM6437 EVM uses a 27 Megahertz crystal to generate the input clock. The DM6437 has an internal PLL which can multiply the input clock to generate the internal clock. The PLL multiplier is set via software on the DM6437 device.

2.10 DM6437 Core Voltage Select

The DM6437 EVM has the ability to adjust the core voltage between 1.2 volts and 1.05 volts. an I/O expander is used to control this I^2C feature.

Chapter 3

Physical Description

This chapter describes the physical layout of the DM6437 EVM and its interfaces.

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3.1 Board Layout

The DM6437 EVM is a 8.75 x 4.5 inch (210 x 115 mm.) ten (10) layer printed circuit board which is powered by an external +5 volt only power supply. Figure 3-1 shows the layout of the DM6437 EVM.

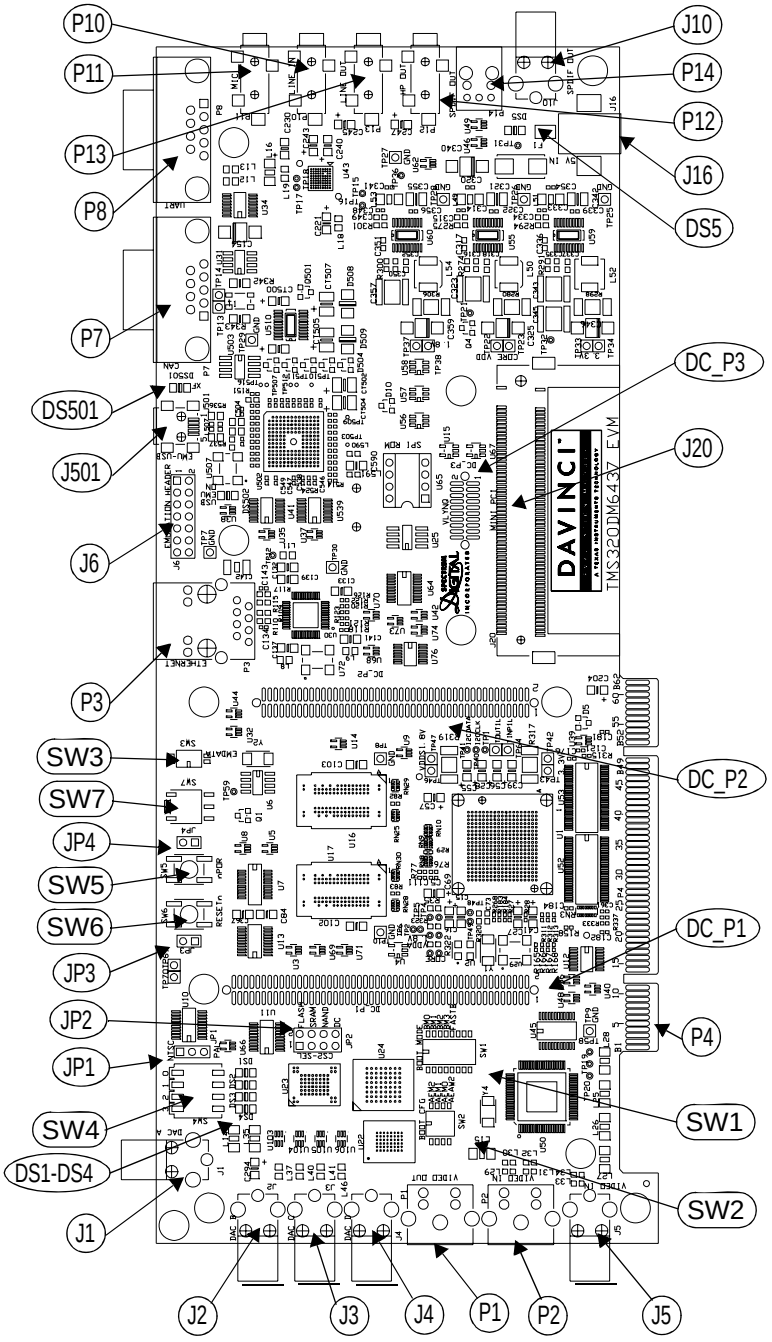

Figure 3-1, DM6437 EVM, Interfaces Top Side

3.2 Connectors

The EVM has twenty three (23) connectors providing interfaces to various peripherals. These connectors are described in the following sections.

Table 1: Connectors

Connector	Size	Function
J1	RCA	DAC A *
J2	RCA	DAC B
J3	RCA	DAC C
J4	RCA	DAC D
J5	RCA	Video In
J6	14	External Emulation Header
J10	RCA	S/PDIF Out
J16	2.5 mm	+5V In
J20	2 x 62	Mini PCI Interface
J501	Mini USB	Embedded USB Emulation Interface
P1	4 Pin DIN	S-Video Out
P2	4 Pin DIN	S-Video In
P3	RJ-45	Ethernet
P4	PCI	PCI
P7	9 Pin D-sub	CAN
P8	9 Pin D-sub	RS-232 UART
P10	3.5 mm	Stereo Line In
P11	3.5 mm	Microphone In
P12	3.5 mm	Headphone Out
P13	3.5 mm	Stereo Line Out
P14	Optical	S/PDIF Out
DC_P1	2x50	Expansion
DC_P2	2x45	Expansion
DC_P3	2x10	Expansion

***** Not populated

3.2.1 J1, DAC A Video Out

J1 is an RCA jack used to interface to DAC A of the DM6437 to a video device. This connector is driven directly by the VPSS back end via an opamp. This connector is not installed for clearance reasons when using the PCI bus. The pinout of this connector is shown below.

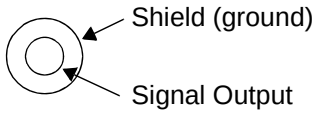

Figure 3-2, J1, RCA Jack

3.2.2 J2, DAC B Video Out

J2 is an RCA jack used to interface to DAC B of the DM6437 to a video device. This connector is driven directly by the VPSS back end via an opamp. This connector is not installed for clearance reasons when using the PCI bus. The pinout of this connector is shown below.

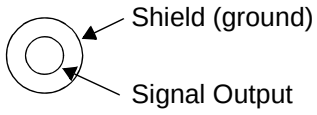

Figure 3-3, J2, RCA Jack

3.2.3 J3, DAC C Video Out

J3 is an RCA jack used to interface to DAC C of the DM6437 to a video device. This connector is driven directly by the VPSS back end via an opamp. This connector is not installed for clearance reasons when using the PCI bus. The pinout of this connector is shown below.

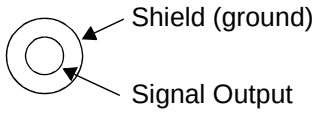

Figure 3-4, J3, RCA Jack

3.2.4 J4, DAC D Video Out

J1 is an RCA jack used to interface to DAC D of the DM6437 to a video device. This connector is driven directly by the VPSS back end via an opamp. This connector is not installed for clearance reasons when using the PCI bus. The pinout of this connector is shown below.

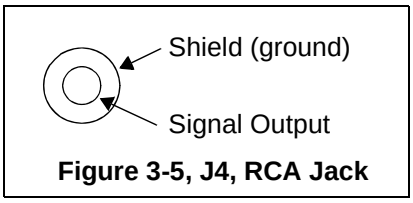

Figure 3-5, J4, RCA Jack

3.2.5 J5, Video In

J5 is an RCA jack used as a video input to the TVP5146M2 video decoder. This connector brings in a video signal to the TVP5146M2. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

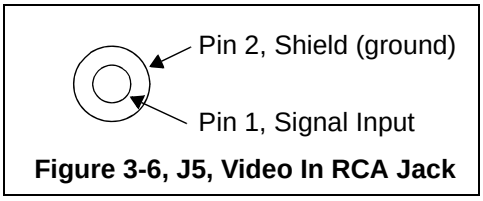

Figure 3-6, J5, Video In RCA Jack

Table 2: J5, Video In, RCA Jack

Pin #	Signal Name
1	Pin 8, TVP5146M2
2	GND

3.2.6 J10, S/PDIF Out

J10 is an RCA jack used as an analog output from the McBSP FSR signal on the DSP. This connector brings out the SPDIF signal. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

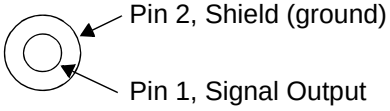

Figure 3-7, J10, S/PDIF Out, RCA Jack

Table 3: J10, S/PDIF, RCA Jack

Pin #	Signal Name
1	S/PDIF Analog output
2	GND

3.2.7 J16, +5V Input

Connector J16 is the input power connector. This connector bring in +5 volts to the EVM. This is a 2.5 mm. jack. The figure below shows this connector as viewed from the card edge.

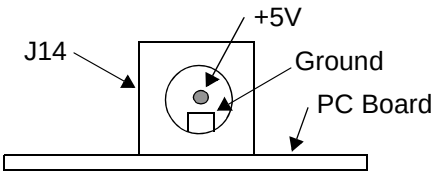

Figure 3-8, J16, +5 Volt Input Connector

3.2.8 J20, Mini PCI Interface

Connector J20 provides a mini-PCI on the DM6437 EVM. Do **NOT** plug into this connector with the power on. The table below shows the signals on this connector.

Table 4: J16, VLYNQ Card Interface

Pin #	Signal
2,3,4,5,6,7,8,10,11, 12,13,15,17,18,29, 30,38,39,47,49,51, 53,55,57,71,73,75, 77,80,82,84,86,93, 98,100,104,105, 106,107,108,109, 113,115,116,117, 118,120,122,123, 124	NC
9,14,20,23,25,27 32,33,34,35,37,41, 42,44,45,46,48,50, 52,54,56,58,60,62, 64,66,68,69,72,74, 76,78,79,81,83,85, 87,90,91,92,94,95, 96,99,101,102, 110,114,119	GND
111	VCC_1.8V
1,19,28,31,40,63, 70,88,89	VCC_3.3V
97,103	VCC_5V
16	VLYNQ_CLK
21	VLYNQ_RXD0
22	VLYNQ_RXD1
24	VLYNQ_SCRUN
26	VLYNQ_RESET
59	VLYNQ_RXD2
61	VLYNQ_RXD3
36	VLYNQ_TXD0
65	VLYNQ_TXD2
67	VLYNQ_TXD3
43	VLYNQ_TXD1

3.2.9 J501, Embedded Mini USB Emulation Interface

This connector allows the user to run software development tools and emulation without an external emulator. The signals on this connector are shown in the table below.

Table 5: J501, Embedded Mini USB Emulation Interface

Pin #	Signal Name
1	VBUS
2	D-
3	D+
4	ID (not used)
5	Ground

3.2.10 P1, Video Out

Connector P1 is a four pin mini din connector which interfaces to an S-video output display device. This connector brings out the DAC B and DAC C. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

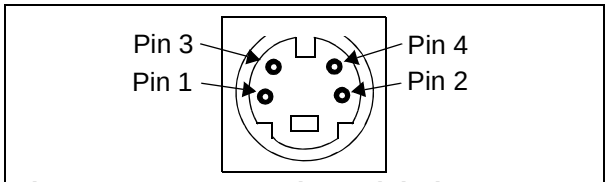

Figure 3-9, P1, Front View, Mini Din Connector

Table 6: P1, Video Out, Mini Din Connector

Pin #	Signal Name
1	Ground
2	Ground
3	DAC_IOUTB, Luma
4	DAC_IOUTC, Chroma

3.2.11 P2, Video In

Connector P2 is a four pin mini din S-video connector which interfaces to the TVP5146M2 encoder. This connector brings in a video signal (LUMA) to pin 9 on the TVP5146M2. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

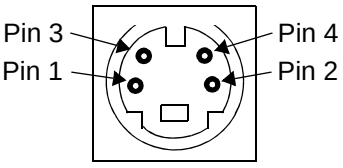

Figure 3-10, P2,Front View, Mini Din Connector

Table 7: J11, Video In, Mini Din Connector

Pin #	Signal Name
1	GND
2	GND
3	LUMA
4	Chroma

3.2.12 P3, Ethernet Interface

The P3 connector is used to provide an 10/100 Mbps Ethernet interface. This is a standard RJ-45 connector. The pinout for the P3 connector is shown in the table below.

Table 8: P3, Ethernet Interface

Pin #	Signal	Pin #	Signal
1	LXT_TDP	2	LXT_TDM
3	LXT_RDP	4	LXT_TDCT
5	NC	6	LXT_RDM
7	NC	8	GND

Two LEDs are embedded into the connector to report link status.

Table 9: Ethernet LEDs

LED #	Color
LED1	Green
LED2	Yellow

3.2.13 P4, PCI Connector

The P4 connector is a card edge PCI interface. This connector has an “A” and “B” side. Because of the card seating notches the pin numbers are not contiguous. The “B” side is the top component side. The I/O direction field is referenced from the PCI slot.

Table 10: P4, PCI Connector, “A” Side

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	TRST-		Not Used	2	+12 Volts		Not Used
3	TMS		Not Used	4	TDI	I/O	Tied to TDO
5	+5 Volts		+5 Volts Power	6	INTA-	O	Interrupt Out
7	INTC-	O	Interrupt Out	8	+5 Volts		+5 Volts Power
9	Rsvd.0		Not Used	10	+V I/O		Not Used
11	Rsvd.1		Not Used	12	Key.1		Key
13	Key.2		Key	14	+3.3 Vaux		Not Used
15	RST-	I	PCI_Resetn	16	+V I/O	O	Not Used
17	GNT-	O	Grant-	18	GND		Ground
19	PME-			20	AD30	I/O/Z	Address/Data 30
21	+3.3 Volts		Not Used	22	AD28	I/O/Z	Address/Data 28
23	AD26	I/O/Z	Address/Data 26	24	GND		
25	AD24	I/O/Z	Address/Data 24	26	IDSEL	I	Initialization Device Select
27	+3.3 Volts		Not Used	28	AD22	I/O/Z	Address/Data 22
29	AD20	I/O/Z	Address/Data 20	30	GND		Ground
31	AD18	I/O/Z	Address/Data 18	32	AD16	I/O/Z	Address/Data 16
33	+3.3 Volts		Not Used	34	FRAME-	I	Frame
35	GND		Ground	36	TRDY-	I/O/Z	Target Ready
37	GND		Ground	38	STOP-	I/O/Z	Stop Direction
39	+3.3 Volts		Not Used	40	SDONE	O	Done
41	SBO-			42	GND		Ground
43	PAR	I/O/Z	Parity	44	AD15	I/O/Z	Address/Data 15
45	+3.3 Volts		Not Used	46	AD13	I/O/Z	Address/Data 13
47	AD11	I/O/Z	Address/Data 11	48	GND		Ground
49	AD9	I/O/Z	Address/Data 9	50	Key.3		Key
51	Key.4		Key	52	C/BE0		Command/Byte Enable0
53	+3.3 Volts		Not Used	54	AD6	I/O/Z	Address/Data 6
55	AD4	I/O/Z	Address/Data 4	56	GND		Ground
57	AD2	I/O/Z	Address/Data 2	58	AD0	I/O/Z	Address/Data 0
59	+V I/O		Not Used	60	REQ64-		Not Used
61	+5 Volts		+5 Volts Power	62	+5 Volts		+5 Volts Power

The signals on the “B” side of the connector are shown in the table below.

Table 11: P4, PCI Connector, “B” Side

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	-12 Volts		Not Used	2	TCK	I	Not Used
3	GND		Ground	4	TDO	I	Tied to TDO
5	+5 Volts		+5 Volt Power	6	+5 Volts	I	+5 Volt Power
7	INTB-		Interrupt OUT	8	INTD-		Interrupt Out
9	PRSNT1-	O	Power Requirement	10	Rsvd.2		
11	PRSNT2-	O	Power Requirement	12	Key.5		Key
13	Key.6		Key	14	Rsvd.3		
15	GND		Ground	16	CLK		System Clock
17	GND		Ground	18	REQ-		
19	+V I/O		Not Used	20	AD31	I/O/Z	Address/Data 31
21	AD29	I/O/Z	Address/Data 29	22	GND		Ground
23	AD27	I/O/Z	Address/Data 27	24	AD25	I/O/Z	Address/Data 25
25	+3.3 Volts		Not Used	26	C/BE3	I/O/Z	Command/Byte Enable 3
27	AD23	I/O/Z	Address/Data 23	28	GND		Ground
29	AD21	I/O/Z	Address/Data 21	30	AD19	I/O/Z	Address/Data 19
31	+3.3 Volts		Not Used	32	AD17	I/O/Z	Address/Data 17
33	C/BE2-	I/O/Z	Command/Byte Enable 2	34	GND		Ground
35	IRDY-	I	Initiator Ready	36	+3.3 Volts		Not Used
37	DEVSEL-	I/O/Z	Device Select	38	GND		Ground
39	LOCK-	I	Resource Locked	40	PERR-	I/O/Z	Parity Error
41	+3.3 Volts		Not Used	42	SERR-	O	System Error
43	+3.3 Volts		Not Used	44	C/BE1-	I/O/Z	Command/Byte Enable 1
45	AD14	I/O/Z	Address/Data 14	46	GND		Ground
47	AD12	I/O/Z	Address/Data 12	48	AD10	I/O/Z	Address/Data 10
49	M66EN	O	66 Mhz Enable	50	Key.7		Key
51	Key.8		Key	52	AD8	I/O/Z	Address/Data 8
53	AD7	I/O/Z	Address/Data 7	54	+3.3 Volts		Not Used
55	AD5	I/O/Z	Address/Data 5	56	AD3	I/O/Z	Address/Data 3
57	GND		Ground	58	AD1	I/O/Z	Address/Data 1
59	+V I/O		Not Used	60	ACK64-		Not Used
61	+5 Volts		+5 Volt Power	62	+5 Volts		+5 Volt Power

3.2.14 P7, CAN Connector

The DM6437 EVM has a 9 Pin female D-connector which brings out the CAN transmit and receive signals. This CAN interface uses the SN65HVD235 CAN driver. The pin positions for the P7 connector as viewed from the edge of the printed circuit board are shown below.

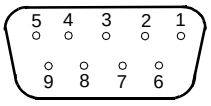

Figure 3-11, P7, DB9 Female Connector

The pin numbers and their corresponding signals are shown in the table below.

Table 12: P7, CANA Pinout

Pin #	Signal Name
1	No Connect
2	CANL
3	GND
4	No Connect
5	No Connect
6	No Connect
7	CANH
8	No Connect
9	No Connect

3.2.15 P8, RS-232 UART Connector

The DM6437 EVM has an RS-232 connector which brings out the SCI transmit and receive signals to be used as UART. This UART uses the MAX3221 RS-232 line driver and is routed to a male 9 pin D-connector, P8. The pin positions for the P8 connector as viewed from the edge of the printed circuit board are shown below.

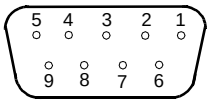

Figure 3-12, P8, DB9 Male Connector

The pin numbers and their corresponding signals are shown in the table below. This corresponds to a standard dual row to DB-9 connector interface used on personal computers.

Table 13: P8, RS-232 UART Pinout

Pin #	Signal Name
1	No Connect
2	RXD
3	TXD
4	No Connect
5	GND
6	No Connect
7	No Connect
8	No Connect
9	No Connect

3.2.16 P10, Audio Line In Connector

The audio line in is a stereo input. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

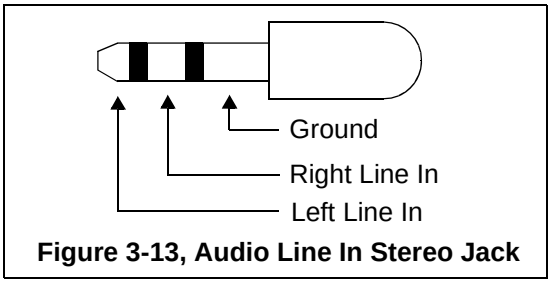

Figure 3-13, Audio Line In Stereo Jack

3.2.17 P11, Microphone Connector

The input is a 3.5 mm. stereo jack. Both inputs are connected to the microphone so it is monaural. The signals on the plug are shown in the figure below.

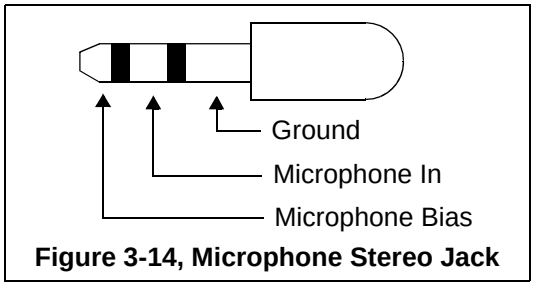

Figure 3-14, Microphone Stereo Jack

3.2.18 P12, Headphone Connector

Connector P12 is a headphone/speaker jack. It can drive standard headphones or a high impedance speaker directly. The standard 3.5 mm jack is shown in the figure below.

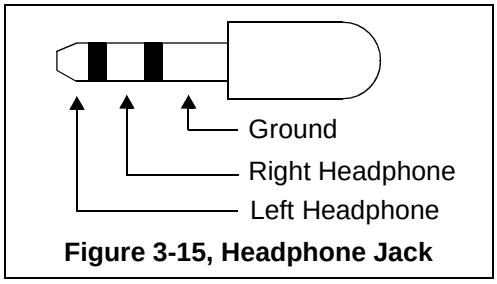

Figure 3-15, Headphone Jack

3.2.19 P12, Audio Line Out Connector

The audio line out is a stereo output. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

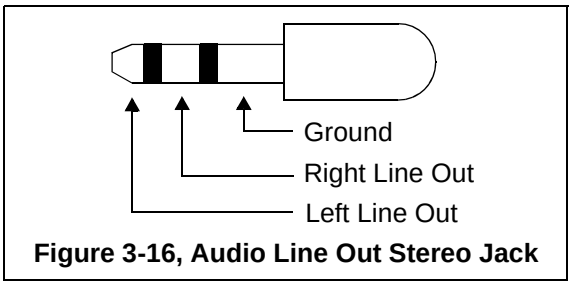

Figure 3-16, Audio Line Out Stereo Jack

3.2.20 P14, S/PDIF Out (Optical)

P14 is an optical transmitter connector used as an output from the McBSP FSR signal on the DM6437 DSP. This connector brings out an optical S/PDIF signal. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

3.2.21 DC_P1, Memory/Video Expansion-

Table 14: DC_P1, Memory/Video Expansion

Pin	Signal	Conn	Pin	Signal	Conn
1	GROUND		2	GROUND	
3	PCLK_GP[54]		4	Y1_EMD_ENABLEn	
5	TVP5146_ENABLEn		6	GROUND	
7	YI3_(CCD3)_GP39]		8	YI4_(CCD4)_GP40]	
9	YI2_(CCD2)_GP[38]		10	YI5_(CCD5)_GP[41]	
11	TI1_(CCD1)_GP[37]		12	TI6_(CCD6_GP[42]	
13	YI0_(CCD0_GP[36]		14	YI7_(CCD7)_GP[43]	
15	GROUND		16	GROUND	
17	C_WE_RNW_GP[35]		18	C_FIELD_EM_A[21]_GP[34]	
19	VD_GP[53]		20	HD_GP[52]	
21	CI3_(CDD11)_EM_A[17]_EM_D[04]_GP[47]		22	CI4_(CDD12)_EM_A[16]_EM_D[03]_GP[48]	
23	CI2_(CDD10)_EM_A[18]_EM_D[05]_GP[46]		24	CI5_(CDD13)_EM_A[15]_EM_D[02]_GP[49]	
25	CI1_(CDD9)_EM_A[19]_EM_D[06]_GP[45]		26	CI6_(CDD14)_EM_A[14]_EM_D[01]_GP[50]	
27	CI0_(CDD8)_EM_A[20]_EM_D[07]_GP[44]		28	CI7_(CDD15)_EM_A[13]_EM_D[00]_GP[51]	
29	GROUND		30	GROUND	
31	VCLK_GP[31]		32	VSYNC_EM_CS4n_GP[32]	
33	GROUND		34	GROUND	
35	VPBECLK_GP[30]		36	HSYNC_EM_CS5n_GP[33]	
37	GROUND		38	GROUND	
39	YOUT3_GP[25]_BOOTMODE3		40	YOUT4_GP[26]_FASTBOOT	
41	YOUT2_GP[24]_BOOTMODE2		42	YOUT5_GP[27]	
43	YOUT1_GP[23]_BOOTMODE1		44	YOUT6_GP[28]	
45	YOUT0_GP[22]_BOOTMODE0		46	YOUT7_GP[29]	
47	GROUND		48	GROUND	
49	COUT3_EM_D[3]_GP[17]		50	COUT4_EM_D[4]_GP[18]	
51	COUT2_EM_D[2]_GP[16]		52	COUT5_EM_D[5]_GP[19]	
53	COUT1_EM_D[1]_GP[15]		54	COUT6_EM_D[6]_GP[20]	
55	COUT0_EM_D[0]_GP[14]		56	COUT7_EM_D[7]_GP[21]	
57	GROUND		58	GROUND	
59	B0_LCD_FIELD_EM_A[3]_GP[11]		60	R0_EM_A[4]_GP[10]_(AEAW2)	
61	G1_EM_A[1]_(ALE)_GP[9]_(AEAW1)		62	B1_EMA[2]_(CLE)_GP[8]_(AEAW0)	
63	R2_EM_BA[0]_GP[6]_(AEM1)		64	R1_EM_A[0]_GP[7]_(AEM2)	
65	B2_EM_BA[1]_GP[6]_(AEM0)		66	G0_EM_CS2n__GP[12]	
67	EM_WAIT_(RDY/BSTn)		68	LCD_OE_EM_CS3n_GP[13]	
69	GROUND		70	GROUND	
71	EM_A[5]_GP[96]		72	EM_A[9]_GP[92]	
73	EM_A[6]_GP[95]		74	EM_A[10]_GP[91]	
75	EM_A[7]_GP[94]		76	EM_A[11]_GP[90]	
77	EM_A[8]_GP[93]		78	EM_A[12]_GP[89]	
79	EM_WEn		80	EM_OEn	
81	GROUND		82	GROUND	
83	MEM_EMD7-7_ENABLEn		84	CLK_OUT_PWM2_GP[84]	
85	CI_EMA_ENABLEn		86	GROUND	
87	RESETn		88	GP[4]_PWM1	
89	SYS_RESETn		90	I2C_INT_ENABLEn	
91	VCC_1V8		92	VCC_1V8	
93	GROUND		94	GROUND	
95	VCC_3V3		96	VCC_3V3	
97	GROUND		98	GROUND	
99	VCC_5V		100	VCC_5V	

3.2.22 DC_P2, Peripheral Expansion

Table 15: DC_P2, Peripheral Expansion

Pin	Signal	Conn	Pin	Signal	Conn
1	GROUND		2	GROUND	
3	VCC_5V		4	VCC_5V	
5	VCC_3V3		6	VCC_3V3	
7	VIC_TINPOL_ENABLEn		8	GROUND	
9	CLKS1_TINPOL_GP[98]		10	CLKS0_TINPOL_GP[97]	
11	GP[00]		12	GP[01]	
13	GP[02]		14	GP[03]	
15	RS232_ENABLEn		16	GROUND	
17	URXD0_GP[85]		18	URTS0_PWM0_GP[88]	
19	UTXD0_GP[86]		20	UCTS0_GP[87]	
21	GROUND		22	GROUND	
23	HECC_RX_TINP1L_URXD1_GP[56]		24	HECC_tX_TOUT1L_UTXD1_GP[55]	
25	GROUND		26	CAN_ENABLEn	
27	AUDIO_CLK		28	GROUND	
29	AXR0[3]_FSR0_GP[102]		30	AXR0[2]_FSX0_GP[103]	
31	AFSR0_DR0_GP[100]		32	AXR0[1]_DX0_GP[104]	
33	AHCLKR0_CLKR0_GP[101]		34	ACLKR0_CLKX0_GP[99]	
35	GROUND		36	GROUND	
37	I2C_CLK		38	I2C_DATA	
39	AIC33_ENABLEn		40	GROUND	
41	AXR0_FSR1_GP[105]		42	AMUTEIN0_FSX1_GP[109]	
43	AMUTE0_DR1_GP[110]		44	ACHLKX0_CLKR1_GP[108]	
45	ACLKX0_CLKX1_GP[106]		46	AFSX0_DX1_GP[107]	
47	GROUND		48	GROUND	
49	RESET_OUTn		50	SPARE	
51	SPARE		52	HCNTL0_MRXER_GP[76]	
53	HDS1n_RXD1_GP[79]		54	HDS2n_RXD0_GP[78]	
55	HINTn_RXD3_GP[82]		56	HRDYn_RXD2_GP[80]	
57	GROUND		58	HD09_COL_GP[67]	
59	HHWIL_RXDV_GP[74]		60	GROUND	
61	HD10_CRS_GP[68]		62	HRNW_RXCLK_GP[77]	
63	GROUND		64	GROUND	
65	HCSnMDC_GP[81]		66	HASn_MDIO_GP[83]	
67	GROUND		68	GROUND	
69	HD11_TXD3_GP[69]		70	HD12_TXD2_GP[70]	
71	HD13_TXD1_GP[71]		72	HD14_TXD0_GP[72]	
73	HCNTL1_TXEN_GP[75]		74	ENET_ENABLEn	
75	GROUND		76	GROUND	
77	SPARE		78	HD15_TXCLK_GP[73]	
79	GROUND		80	GROUND	
81	USER_I2C_IO.A0P6		82	USER_I2C_IO.A0P7	
83	SPARE		84	SPARE	
85	USER_I2C_IO.A1P2		86	USER_I2C_IO.A1P3	
87	USER_I2C_IO.A1P0		88	USER_I2C_IO.A1P1	
89	GROUND		90	GROUND	

3.2.23 DC_P3, VLYNQ Connector

The DC_P3 connector allows the user to connect the VLYNQ interface to other logic. The pinout for the DC_P3 connector is shown in the table below.

Table 16: DC_P3, VLYNQ Header

Pin #	Signal	Conn	Pin #	Signal	Conn
1	HD00_VLYNQ_SCRUN_GP[58]		2	VLYNQ_CLOCK_GP[57]	
3	GROUND		4	GROUND	
5	HD01_VLYNQ_RXD0_GP[59]		6	HD05_VLYNQ_TXD0_GP[63]	
7	HD02_VLYNQ_RXD1_GP[60]		8	HD06_VLYNQ_TXD1_GP[64]	
9	GROUND		10	GROUND	
11	VCC_3V3		12	DC_P3_VLYNQ_RESETn	
13	HD03_VLYNQ_RXD2_GP[61]		14	HD07_VLYNQ_TXD2_GP[65]	
15	HD04_VLYNQ_RXD3_GP[62]		16	HD08_VLYNQ_TXD3_GP[66]	
17	GROUND		18	GROUND	
19	VCC_5V		20	VCC_5V	

3.3 Jumpers

The DM6437 EVM has four (4) jumpers which are used to make certain logic or feature determinations on the board. The function of each jumper is described in the table below.

Table 17: Jumpers

Jumper #	Function	Size
JP1	NTSC/PAL Select	1x3
JP2	CS2 Select	2x4
JP3 *	Reset	1x2
JP4 *	Power Up Reset	1x2

* Not populated

3.3.1 JP1 Jumper

Jumper JP1 is used to select the display output format, NTSC or PAL. This jumper **must** be populated in one of the two configurations. When the center to NTSC is selected the display output will be NTSC format. When the center to PAL is selected the display output will be in PAL format. These positions are shown in the figure below.

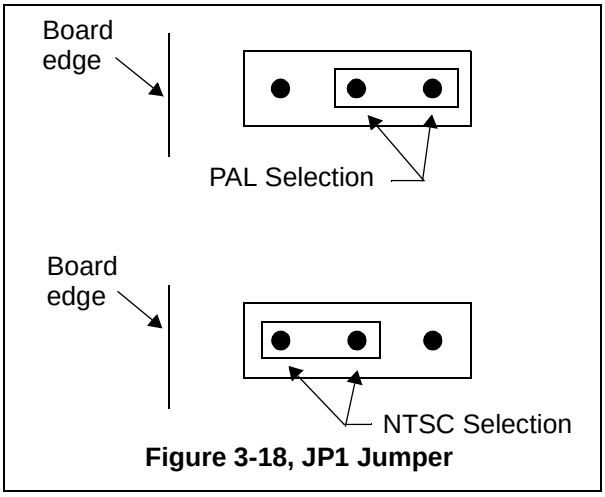

Figure 3-18, JP1 Jumper

3.3.2 JP2 Jumper

Jumper JP2 is a jumper bank used to select the routing of the CS2 signal. It can be routed to Flash ROM, SRAM, NAND Flash, and daughter card connector. Only one of these 1-2 selections should be made. The positions are shown in the figure below.

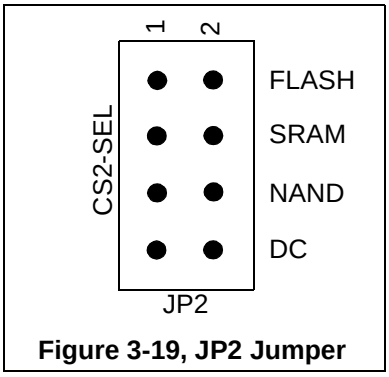

Figure 3-19, JP2 Jumper

3.3.3 JP3 Jumper

Jumper JP3 is a jumper used to allow external switches to interface to the DM6437 power up reset signal.

3.3.4 JP4 Jumper

Jumper JP4 is a jumper used to allow external switches to interface to the DM6437 reset signal.

3.4 LEDs

The DM6437 EVM has eight (8) LEDs. Four of these LEDs (DS1-4) are under user control and addressed over the I^2C bus. LED DS5 indicates the presence of +5 volts on the board. The remaining LEDs, DS501 and DS502 indicate embedded USB status. DS502 is on when embedded USB emulation is selected and off when the external JTAG emulator is plugged into connector J6. DS501 blinks as packets are sent to and from the embedded USB emulator. The LED functions are summarized in the table below.

Table 18: LEDs

LED #	Use	Color
DS1	User Defined	Green
DS2	User Defined	Green
DS3	User Defined	Green
DS4	User Defined	Green
DS5	+5V present	Red
DS501	Embedded Emulation Status	Green
DS502	Embedded/external EMU	Green

3.5 Switches

The DM6437 EVM has seven (7) switches. These switches are used to create certain actions on the board or to select certain functions on the board. The switch functions are summarized in the table below.

Table 19: Switches

SW #	Function
SW1	Bootload Mode Select
SW2	DM6437 Muxing Configuration
SW3	EMIF Data Select
SW4	4 position user readable
SW5	Power On Reset
SW6	Reset
SW7	Slide Switch

3.5.1 SW1, Bootload Mode Select

Switch SW1 is an 8 position switch used to select the source of the bootload. Five (5) of the eight (8) positions are used. The selections are shown in the table below.

Table 20: SW1, Bootload Mode Select

SW1[4:1]	SW1[5]	Auto Detected	Boot Description	Notes	DSPBOOTADDR default
0000	x	x	Emulation Boot In this mode, FASTBOOT setting is don't care (not used by bootloader code)	DM6437 is master	0x0010 0000
0001	1*	0	HPI Boot	DM6437 is slave	0x0010 0000
0001	1*	1	PCI Boot without auto-initialization	DM6437 is slave	0x0010 0000
0010	1*	0	PCI Boot with auto-initialization	DM6437 is slave	0x0010 0000
0010	1*	1	HPI Boot	DM6437 is slave	0x0010 0000
0100	0	x	EMIFA ROM Direct Boot	DM6437 is master	0x4200 0000
0100	1	x	EMIFA ROM Fast Boot	DM6437 is master	0x0010 0000
0101	x	x	I2C Boot	DM6437 is master	0x0010 0000
0110	1*	x	SPI Boot (McBSP peripheral)	DM6437 is master	0x0010 0000
0111	1*	x	NAND Flash	DM6437 is master	0x0010 0000
1000	x	x	UART	DM6437 is master	0x0010 0000
1011	x	x	EMAC Boot through secondary bootloader	DM6437 is slave	0x0010 0000

x = don't care, * these boot modes must be accompanied with FASTBOOT = 1.

The figure below shows the as shipped boot configuration for SW1, booting from Flash ROM.

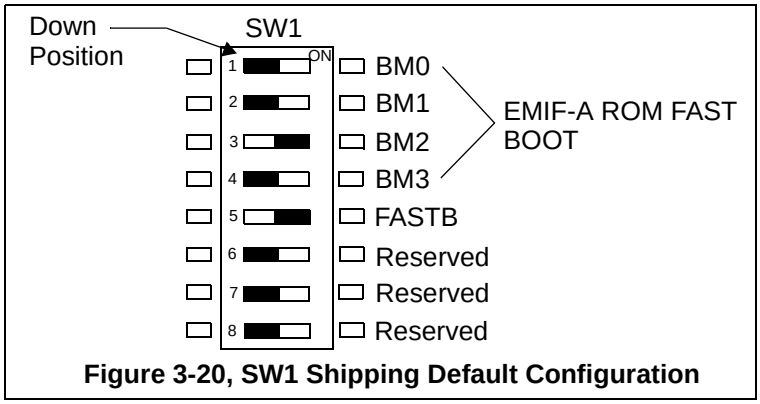

Figure 3-20, SW1 Shipping Default Configuration

3.5.2 SW2, Bootload Configuration Select

Switch SW2 is an 4 position switch used to select the DM6437 multiplexing options at reset. The selection are shown in the table below.

Table 21: SW2, Bootload Configuration Select

Position	Function	Description
1	AEM2	Specifies EMIF mode at reset
2	AEM1	Specifies EMIF mode at reset
3	AEM0	Specifies EMIF mode at reset
4	AEAW2	Specifies EMIF mode at reset

The figure below shows the as shipped boot configuration for SW2.

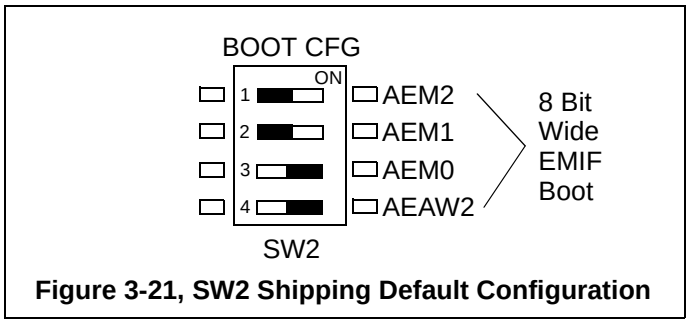

Figure 3-21, SW2 Shipping Default Configuration

3.5.3 SW3, EMIF Data Select

Switch SW3 is used to select between data bus pins for the asynchronous EMIF controller. The functions of this switch are shown in the table below.

Table 22: SW3, EMDATA Select

Position	Function	Description
1	Not used	Not Used
2	MEM_EMD7-0_SELECT	0=Selects CI0-7 as EMIF data bus D0:D7 pins 1=Selects COUT0-7 data bus D0:D7 pins

The figure below shows the as shipped boot configuration for SW3.

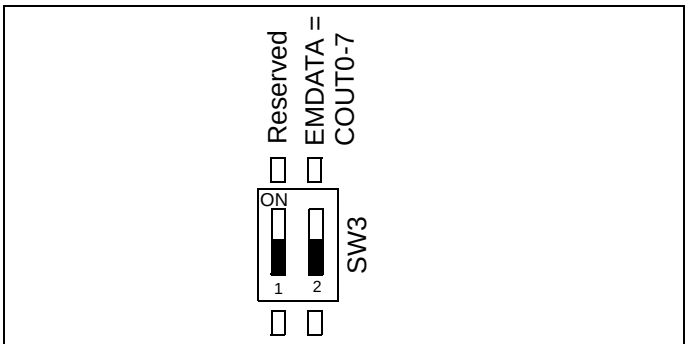

Figure 3-22, SW3 Shipping Default Configuration

3.5.4 SW4, 4 Position User Readable

Switch SW4 is a 4 position bank of user readable switches via the I^2C expander. The individual switches can be placed in any position and read by the user software from the expander. See the section on I^2C expanders for more information.

3.5.5 SW5, Power On Reset Switch

Switch SW5 is a momentary switch that asserts power on reset to the DM6437 device.

3.5.6 SW6, Reset Switch

Switch SW6 is a momentary switch that asserts a reset to the DM6437 processor.

3.5.7 SW7, Slide Switch

Switch SW7 is a 2 position slide switch used by demonstration software. The switch is read via a I^2C expander. Refer to the I^2C section for more information.

3.6 Test Points

The EVM has 51 test points. All test points appear on the top of the board. The following figure identifies the position of each test point. the next table list each test point and the signal appearing on that test point.

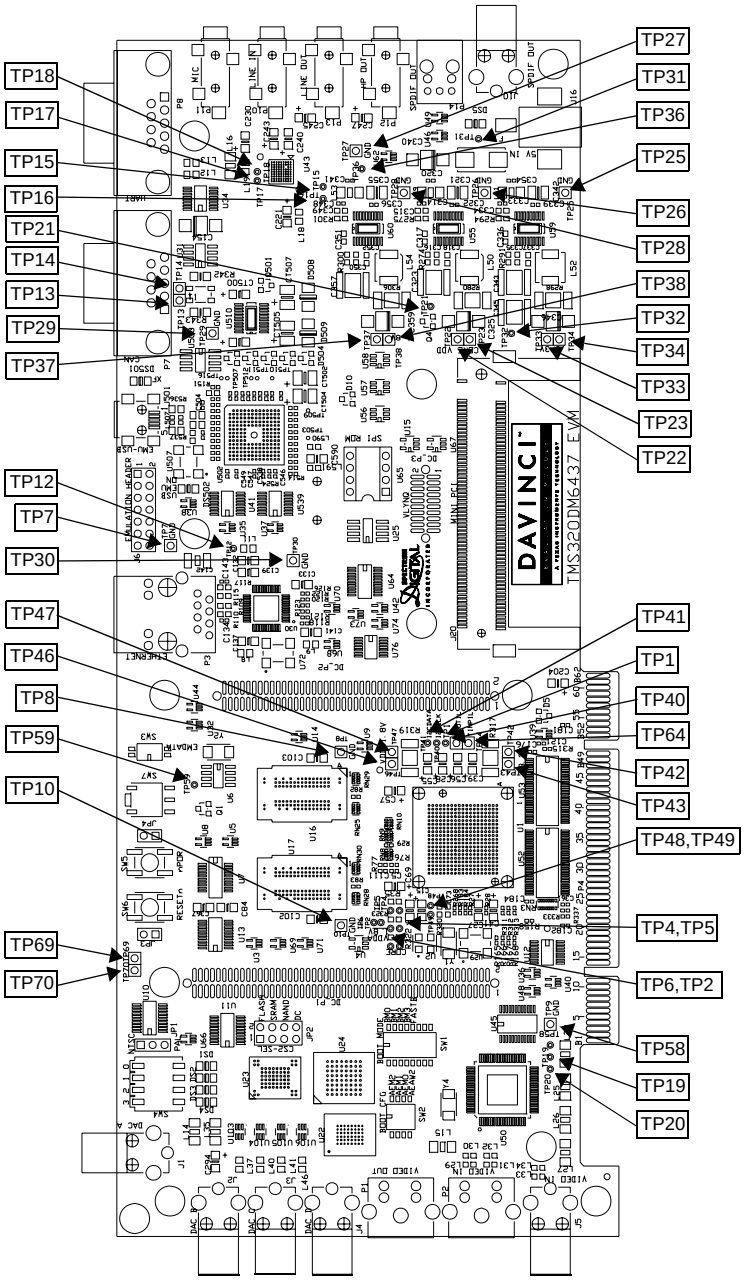

Figure 3-20, DM6437 EVM, Test Points

Table 23: DM6437 EVM Test Points

Test Point #	Signal	Test Point #	Signal
TP1	RESETOUTn	TP27	GND
TP2	RSV4	TP28	GND
TP6	RSV5	TP29	GND
TP7	GND	TP30	GND
TP8	GND	TP31	VCC_5V
TP10	GND	TP32	3V3_PWR_OK
TP12	Ethernet PHY Interrupt Pin	TP36	1V8_PWR_OK
TP13	CAN Driver Output B_CANH	TP40	DM6437 I2CCLK
TP14	CAN Driver Output B_CANL	TP41	DM6437 I2CDATA
TP15	Codec MFP2 Pin	TP52	VDD_1P1V
TP16	Codec MPF3 Pin	TP53	VDD_1P1V
TP17	Codec GPIO1 Pin	TP58	VIDEO DECODER GLCO/I2C Pin
TP18	Codec GPIO2 Pin	TP59	VIC INPUT CLOCK
TP19	VIDEO DECODER AVID/GPIO Pin	TP61	DM6437 HECC_RX
TP20	VIDEO DECODER INTREQ Pin	TP64	DM6437 HECC_TX
TP21	CORE_PWR_OK	TP69	DM6437 PWM1
TP25	GND	TP70	DM6437CLK_OUT
TP26	GND		

Table 24: Power Pair Test Points

Power Pairs		Power Domain	Resistance Between Inputs
Input1	Input2		
TP4	TP5	DDR_VDDL	0.1 ohms
TP22	TP23	DSP_CORE_VDD	0.025 ohms
TP33	TP34	VCC_3V3	0.025 ohms
TP37	TP38	VCC_1V8	0.025 ohms
TP42	TP43	DVD_3V3	0.025 ohms
TP47	TP46	DVDD_1V8	0.025 ohms
TP48	TP49	PLLPWR18	0.1 ohms
TP52	TP53	VDDA_1P1V	0.1 ohms
TP54	TP55	VDDA_1P8V	0.1 ohms

Appendix A

Schematics

This appendix contains the schematics for the DM6437 EVM.

SCHEMATIC CONTENTS

I2C Address Table

ADDRESS HEX	ADDRESS BINARY	DEVICE	FUNCTION
0x38	00111000B	PCF8574	USER INPUT Expander - 0111(A2)(A1)(A0)
0x39	00111001B	PCF8574	LED Expander - 0111(A2)(A1)(A0)
0x3A	00111010B	PCF8574	VIC PLL Expander - 0111(A2)(A1)(A0)
0x3B	00111011B	PCF8574	VLYNQ IO Expander - 0111(A2)(A1)(A0)
0x50	01010000B	CAT24C256	EEPROM - 1010(A2)(A1)(A0)
0x1B	00011011B	AIC33	AUDIO CODEC - 00110(MFP1)(MFP0)
0x5D	01011101B	TVP5146	VIDEO DECODER - 101110(I2CA)

SPECTRUM DIGITAL INCORPORATED

Title: TMS320DM6437 Evaluation Module

Page Contents: TITLE SHEET

Size:B | DWG NO 509102-0001 | Revision: D

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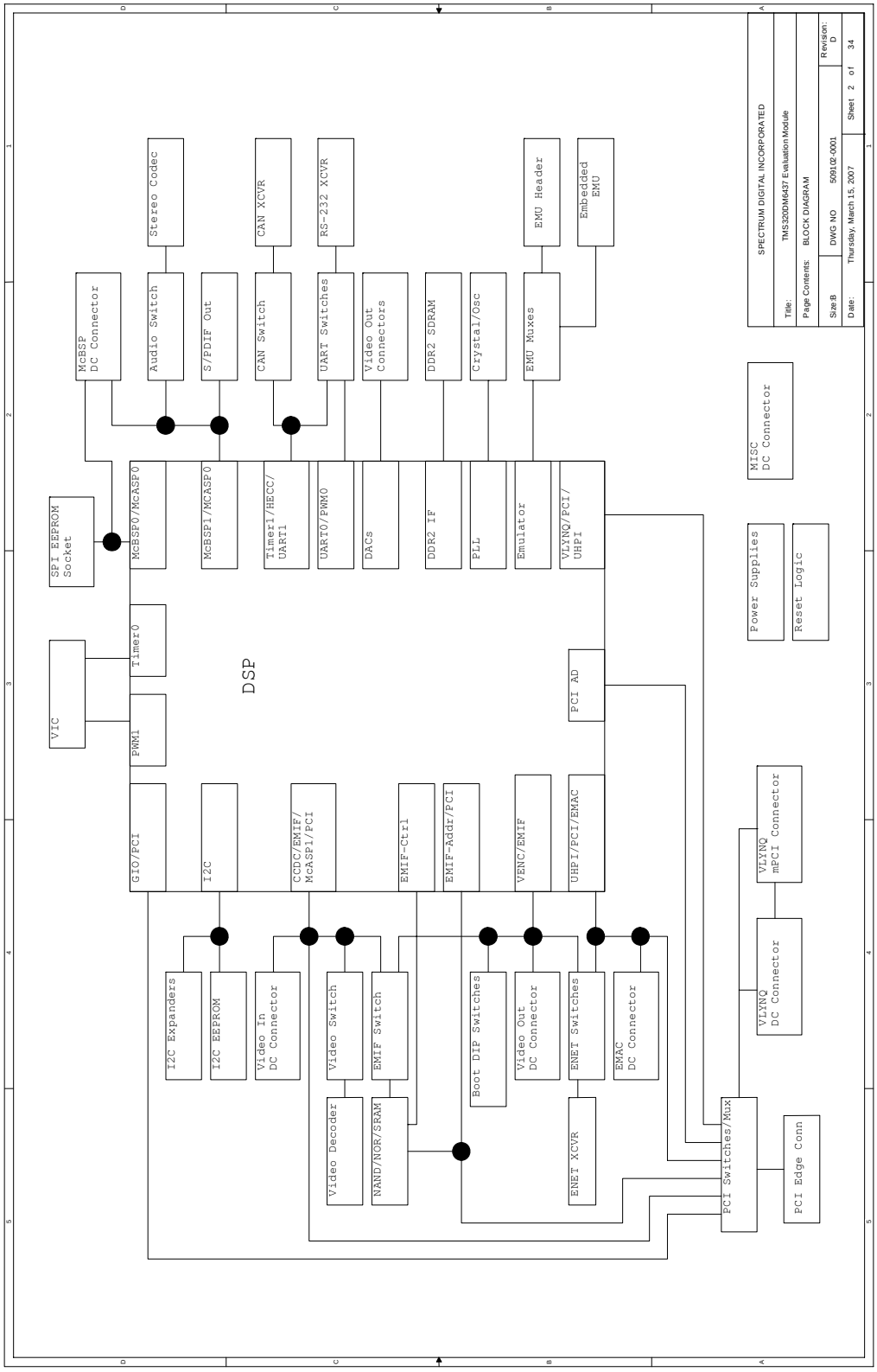
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Title: TMS320DM6437 Evaluation Module
Page Contents: BLOCK DIAGRAM
Size:B
DWG NO 509102-0001
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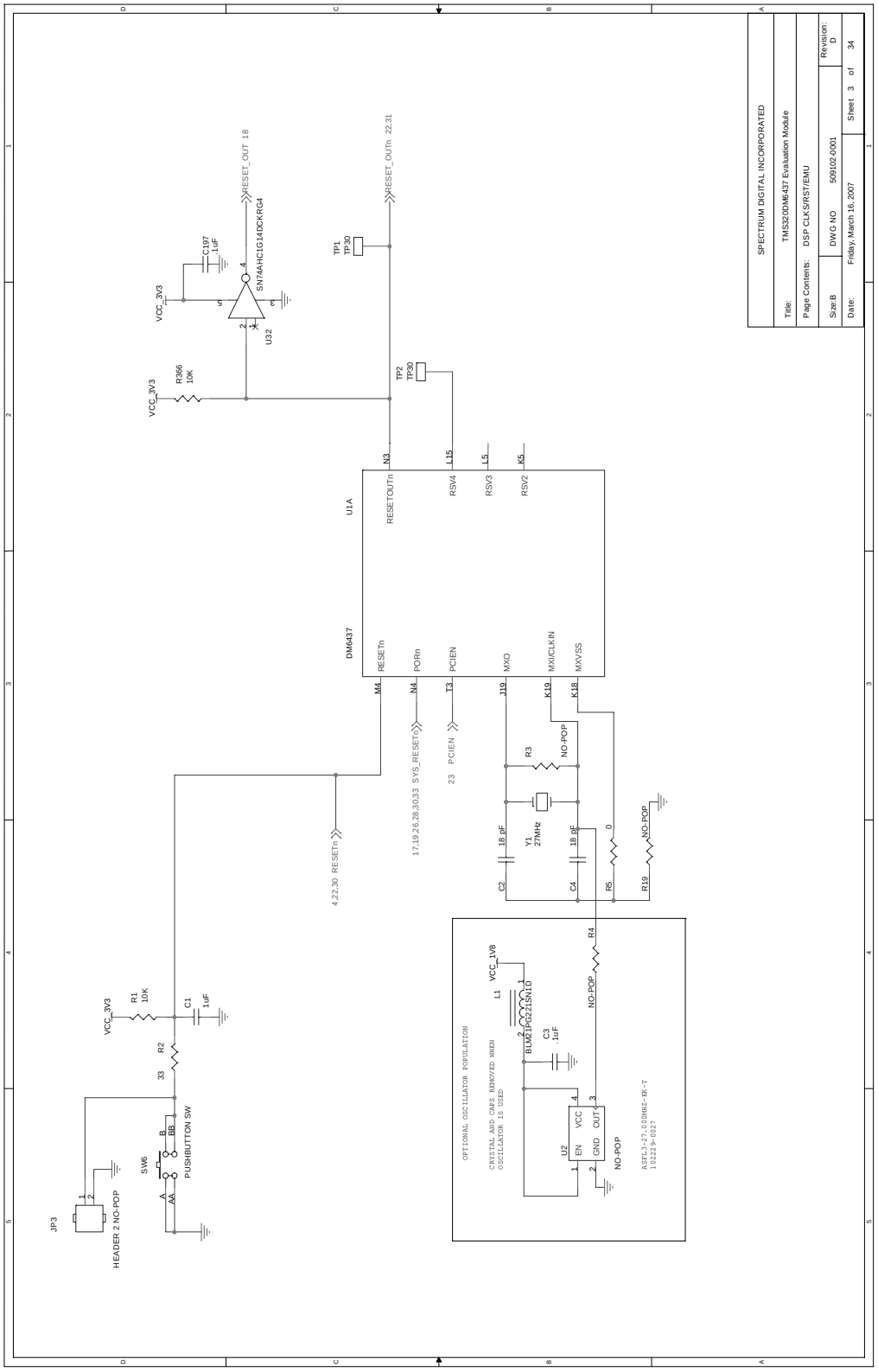
Date: Thursday, March 15, 2007
Sheet 2 of 34
DSP
Stereo Codec
CAN XCVR
RS-232 XCVR
EMU Header
Embedded EMU
McBSP DC Connector
Audio Switch
S/PDIF Out
CAN Switch
UART Switches
Video Out Connectors
DDR2 SDRAM
Crystal/Osc
EMU Muxes
MISC DC Connector
SPI EEPROM Socket
McBSP0/McASP0
McBSP1/MCASP0
Timer1/HECC/ UART1
UART0/PWM0
DACs
DDR2 IF
PLL
Emulator
VLYNQ/PCI/ UHPI
Power Supplies
Reset Logic
VIC
Timer0
PWM1
PCI AD
GIO/PCI
I2C
CCDC/EMIF/ McASP1/PCI
EMIF-Ctrl
EMIF-Addr/PCI
VENC/EMIF
UHPI/PCI/EMAC
VLYNQ mPCI Connector
VLYNQ DC Connector
I2C Expanders
I2C EEPROM
Video In DC Connector
Video Switch
EMIF Switch
Boot DIP Switches
Video Out DC Connector
ENET Switches
EMAC DC Connector
Video Decoder
NAND/NOR/SRAM
ENET XCVR
PCI Switches/Mux
PCI Edge Conn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Page Contents: DSP CLKS/RST/EMU
Size:B
DWG NO 509102-0001
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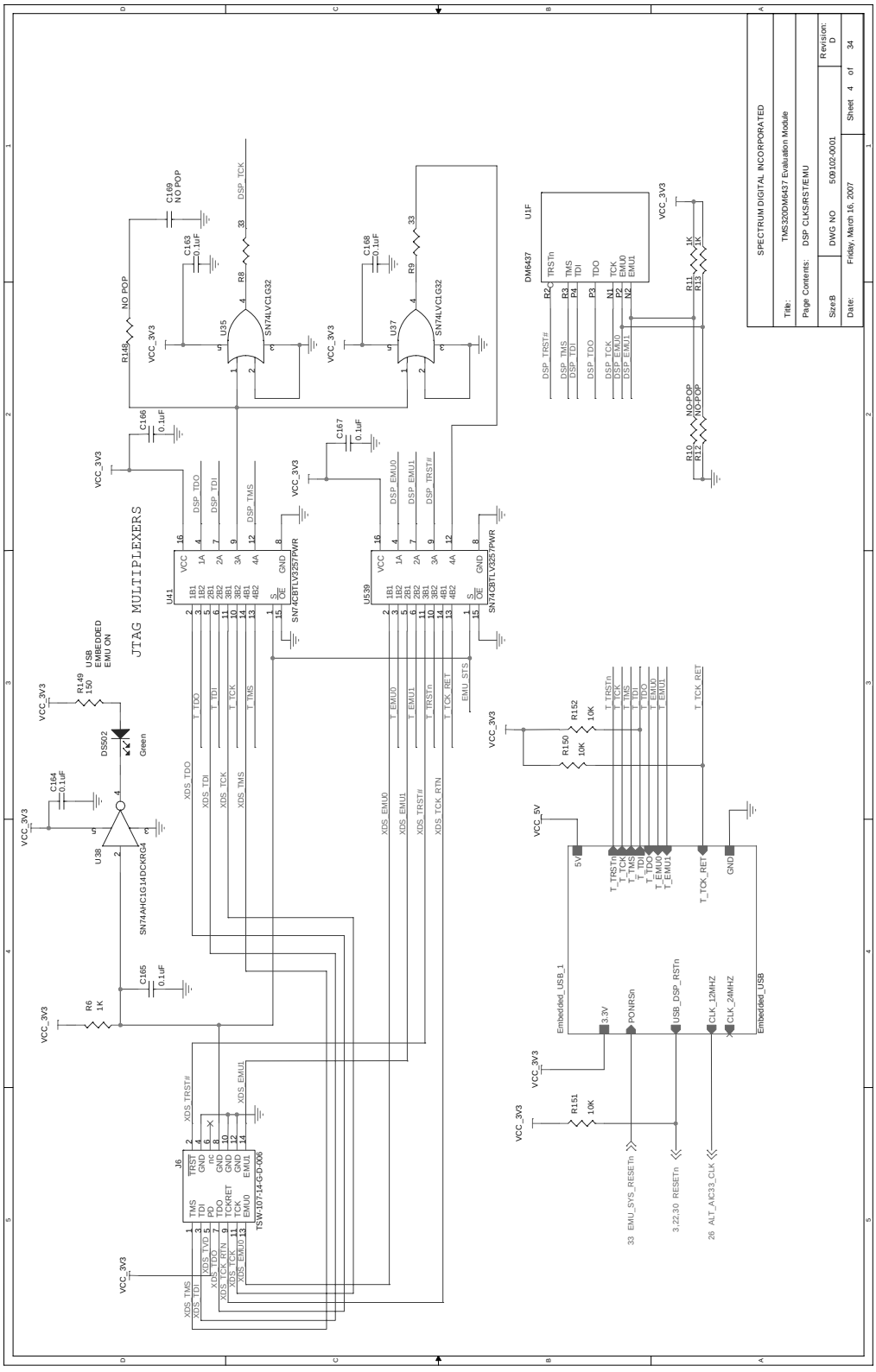
DM6437
U1A
RESETOUTn
RESETn
PORn
PCIEN
MXO
MXI/CLKIN
MXVSS
RSV4
RSV3
RSV2
RESET_OUT 18
RESET_OUTn 22,31
SN74AHC1G14DCKRG4
U32
C197 .1uF
VCC_3V3
R366 10K
TP1 TP30
TP2 TP30
SYS_RESETn
PCIEN
17,19,26,28,30,33
4,22,30 RESETn
R3 NO-POP
Y1 27MHz
18 pF
C2
C4
R5 0
R19 NO-POP
R4 NO-POP
L1 BLM21PG221SN1D
C3 1uF
VCC_1V8
U2
EN
VCC
GND
OUT
NO-POP
OPTIONAL OSCILLATOR POPULATION
CRYSTAL AND CAPS REMOVED WHEN OSCILLATOR IS USED
R1 10K
C1 1uF
R2 33
SW6
PUSHBUTTON SW
JP3
HEADER 2 NO-POP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DWG NO 5IB102-0001
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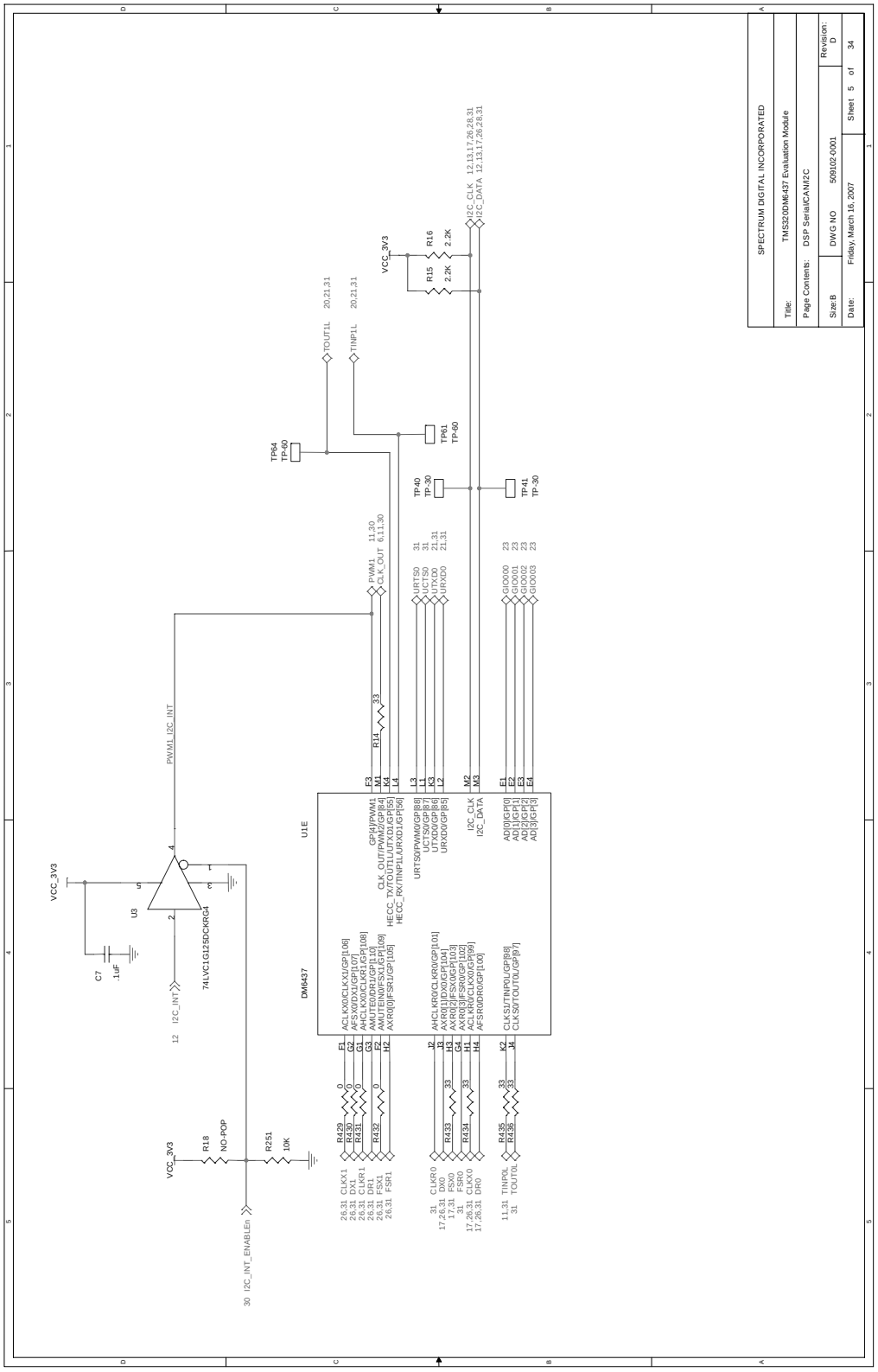
JTAG MULTIPLEXERS
USB EMBEDDED EMU ON
DS502
Green
R149 150
C164 0.1uF
C165 0.1uF
R6 1K
U38
SN74AHC1G14DCKRG4
J6
TSW-107-14-G-D-006
C166 0.1uF
C167 0.1uF
C168 0.1uF
C169 NO POP
C163 0.1uF
R148 NO POP
R8 33
R9 33
U35
U37
SN74LVC1G32
U41
U539
SN74CBTLV3257PWR
DM6437 U1F
R2 TRSTn
R3 TMS
R4 TDI
P3 TDO
N1 TCK
P2 EMU0
N2 EMU1
R11 1K
R13 1K
R10 NO POP
R12 NO POP
R150 10K
R152 10K
R151 10K
Embedded_USB_1
Embeded_USB
XDS_TDO
XDS_TDI
XDS_TCK
XDS_TMS
XDS_EMU0
XDS_EMU1
XDS_TRST#
XDS_TCK_RTN
T_TDO
T_TDI
T_TCK
T_TMS
T_TRSTn
T_EMU0
T_EMU1
T_TCK_RET
EMU_STS
DSP_TDO
DSP_TDI
DSP_TMS
DSP_TCK
DSP_TRST#
DSP_EMU0
DSP_EMU1
PONRSn
USB_DSP_RSTn
CLK_12MHZ
CLK_24MHZ
RESETn
EMU_SYS_RESETn
ALT_AIC33_CLK
VCC_3V3
VCC_5V
GND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Page Contents: DSP Serial/CAN/I2C
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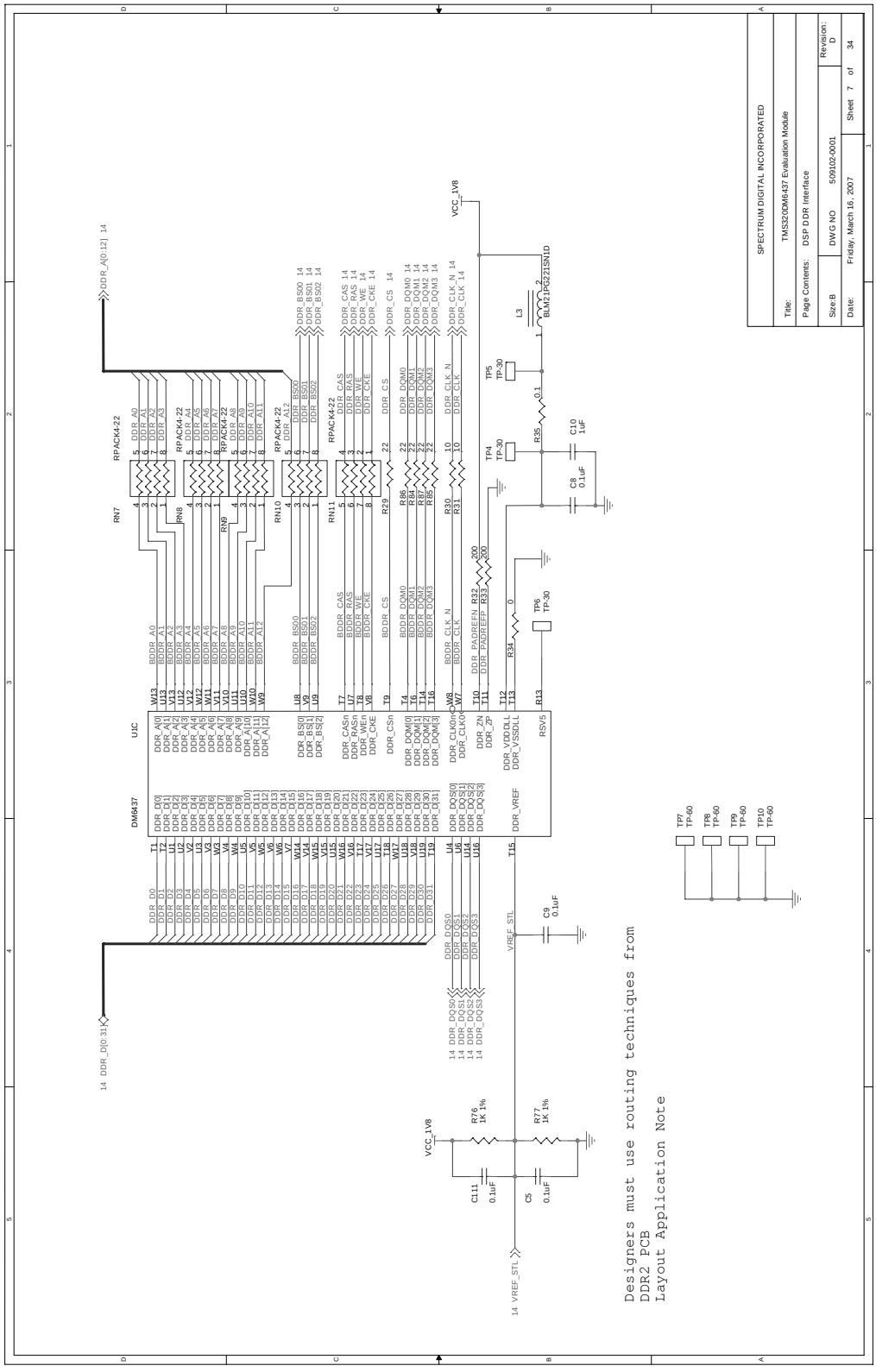
DWG NO 509102-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 5 of 34
DM6437
U1E
U3
74LVC1G125DCKRG4
VCC_3V3
R18 NO-POP
R251 10K
C7 .1uF
I2C_INT
I2C_INT_ENABLEn
PWM1 I2C_INT
TOUT1L
TINP1L
TP64 TP-60
TP61 TP-60
TP40 TP-30
TP41 TP-30
R15 2.2K
R16 2.2K
I2C_CLK
I2C_DATA
R14 33
R429 0
R430 0
R431 0
R432 0
R433 33
R434 33
R435 33
R436 33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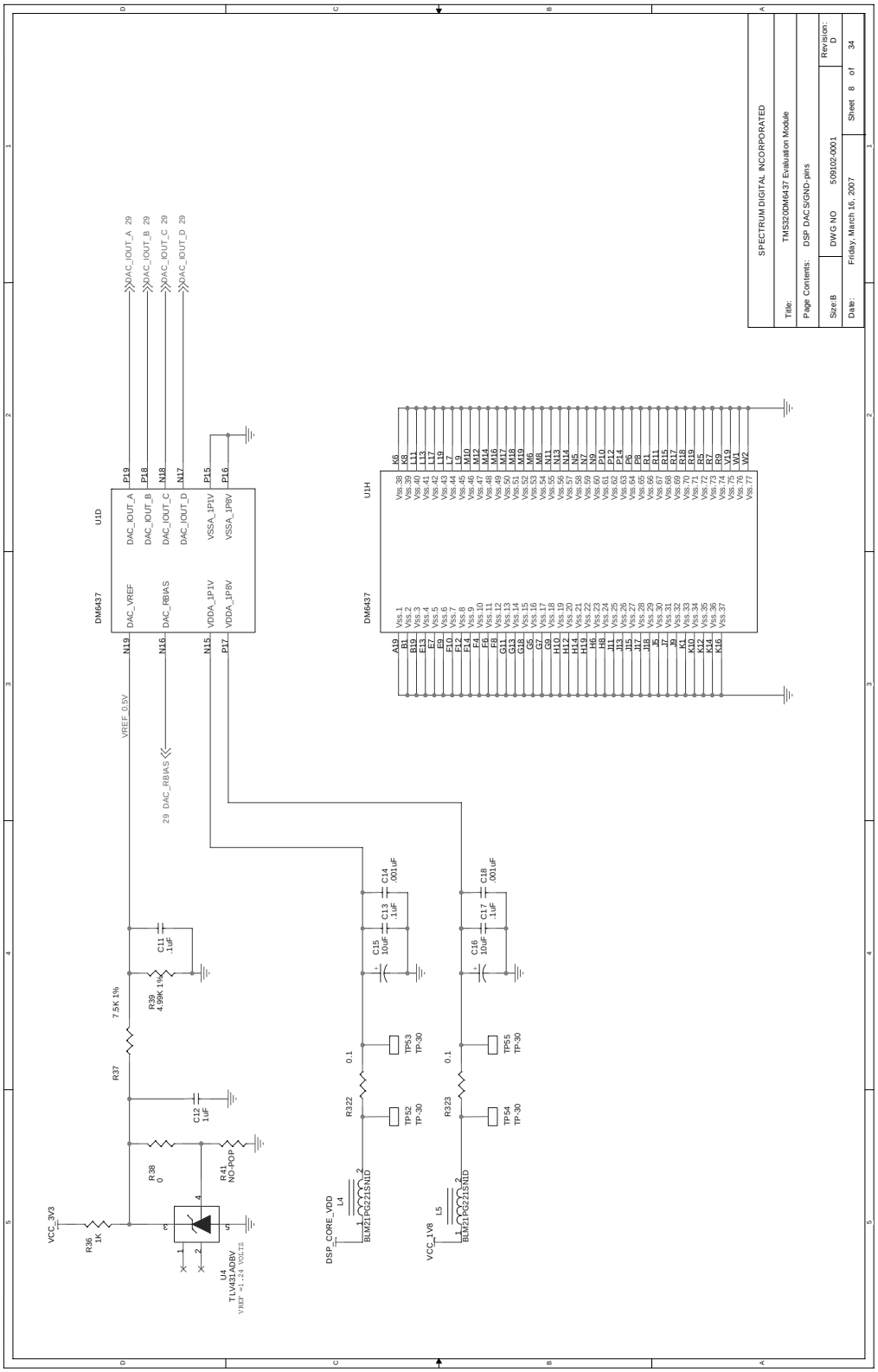
Page Contents: DSP DDR Interface
Size:B
DWG NO 5091020001
Revision: D
Date: Friday, March 16, 2007
Sheet 7 of 34
Designers must use routing techniques from
DDR2 PCB
Layout Application Note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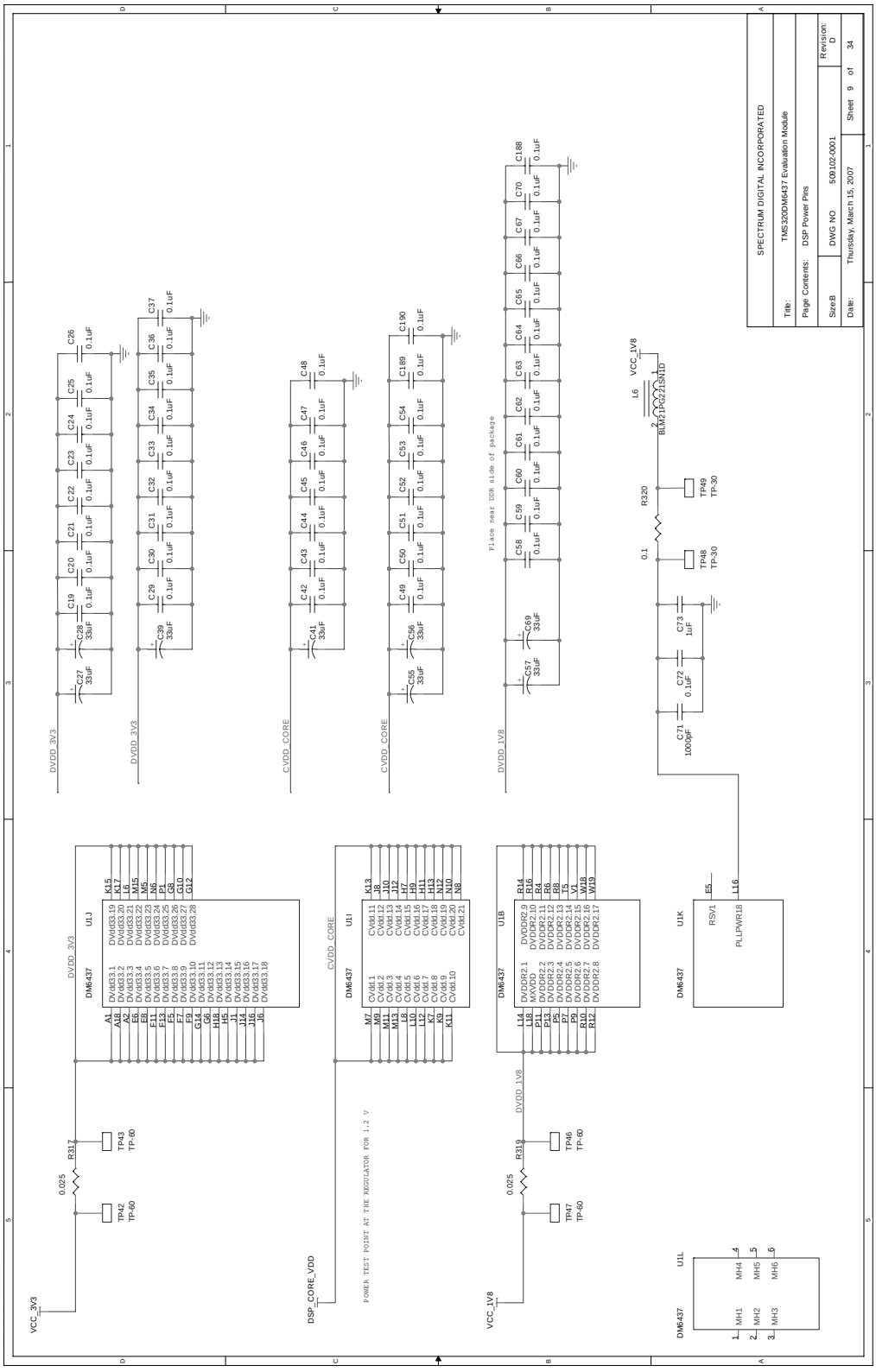
Title: TMS320DM6437 Evaluation Module
Page Contents: DSP DAC'SGND pins
Size:B
DWG NO 509102-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 8 of 34
U1D
DM6437
DAC_IOUT_A
DAC_IOUT_B
DAC_IOUT_C
DAC_IOUT_D
DAC_VREF
DAC_RBIAS
VSSA_1P1V
VSSA_1P8V
VDDA_1P1V
VDDA_1P8V
U1H
VREF 0.5V
29 DAC_RBIAS
R36 1K
R37 7.5K 1%
R38 0
R39 4.99K 1%
R41 NO-POP
C11 .1uF
C12 1uF
U4 TLV431ADBV VREF =1.24 VOLTS
DSP_CORE_VDD
VCC_1V8
L4 BLM21PG221SN1D
L5 BLM21PG221SN1D
R322 0.1
R323 0.1
C13 .1uF
C14 .001uF
C15 10uF
C16 10uF
C17 .1uF
C18 .001uF
TP52 TP-30
TP53 TP-30
TP54 TP-30
TP55 TP-30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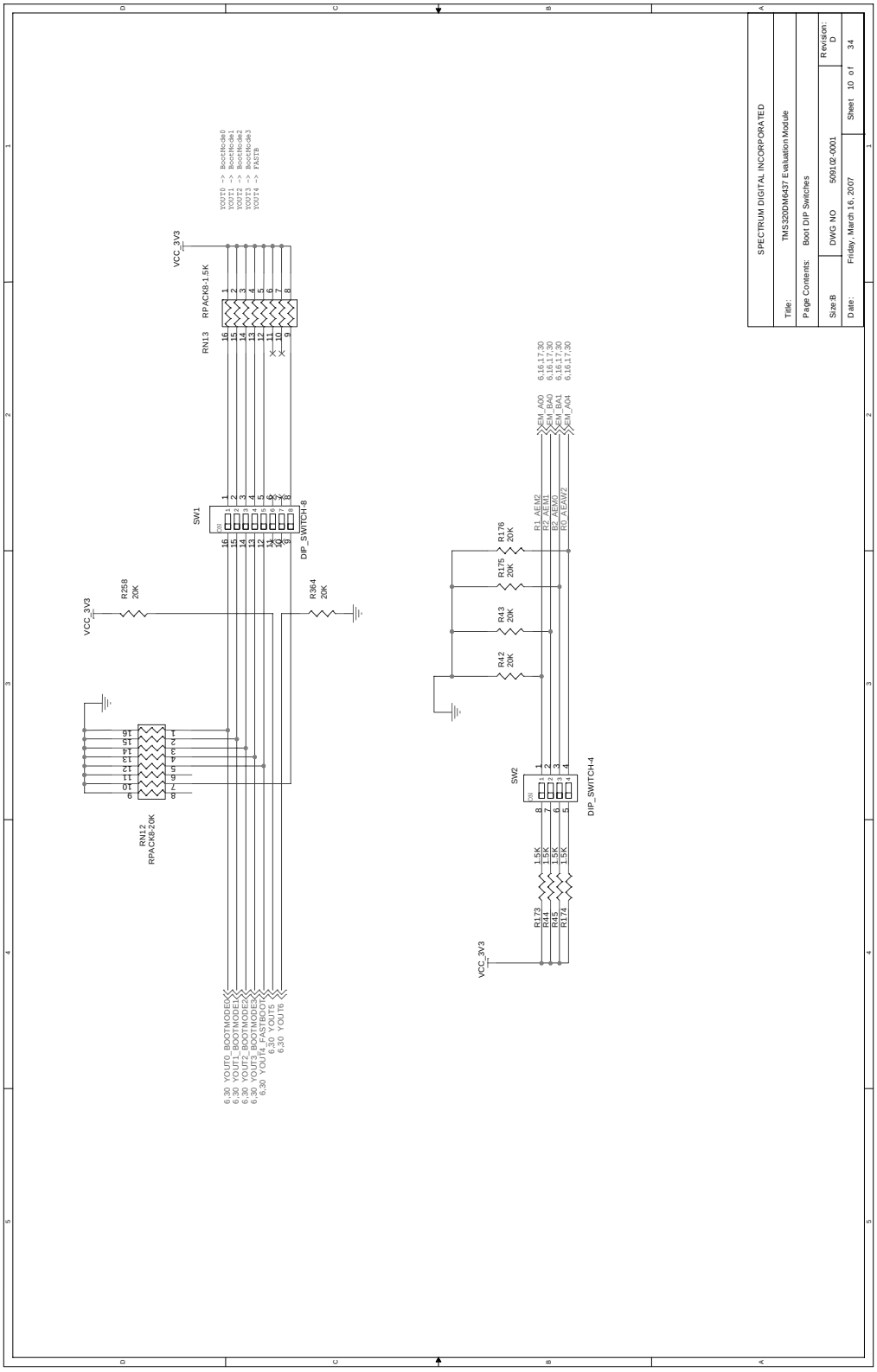
Page Contents: DSP Power Pins
Size:B DWG NO 509102-0001 Revision: D
Date: Thursday, March 15, 2007 Sheet 9 of 34
DVDD_3V3
CVDD_CORE
DVDD_1V8
VCC_1V8
place near DSP side of package
POWER TEST POINT AT THE REGULATOR FOR 1.2 V
DSP_CORE_VDD
VCC_3V3
DM6437
U1J
U1I
U1B
U1K
U1L
R317
R319
R320
L6
L16
C71
C72
C73
TP42
TP43
TP46
TP47
TP48
TP49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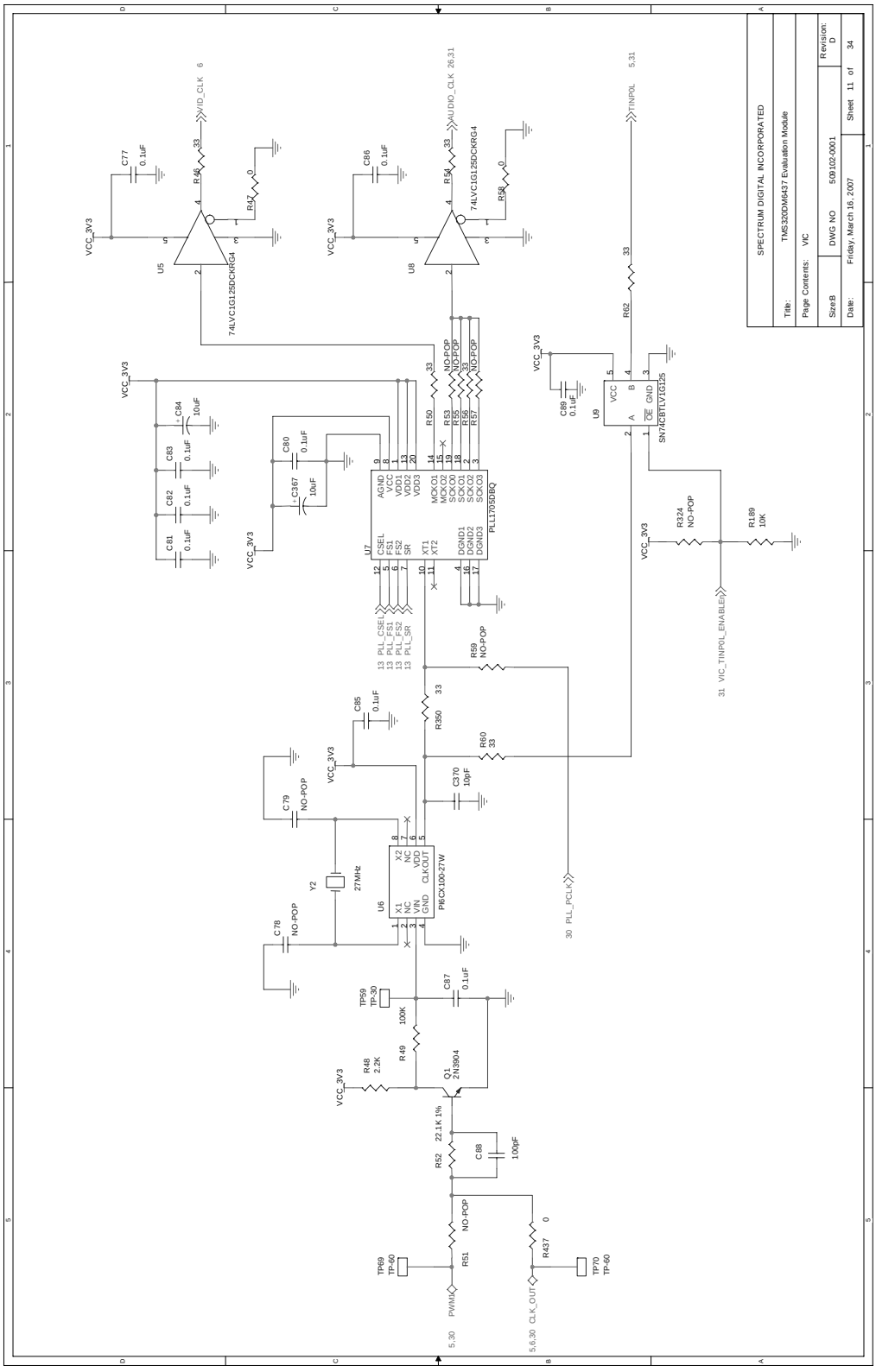
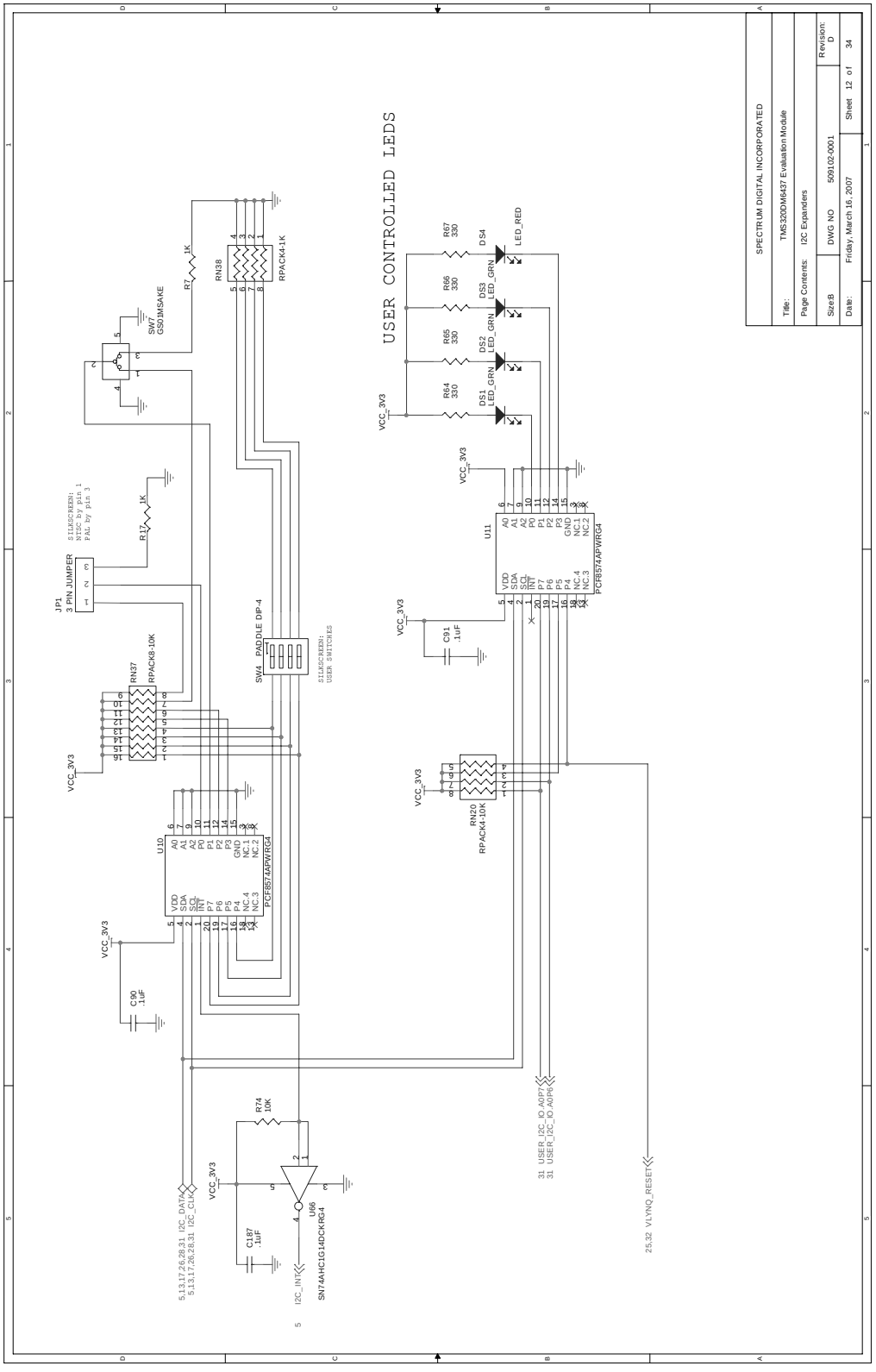
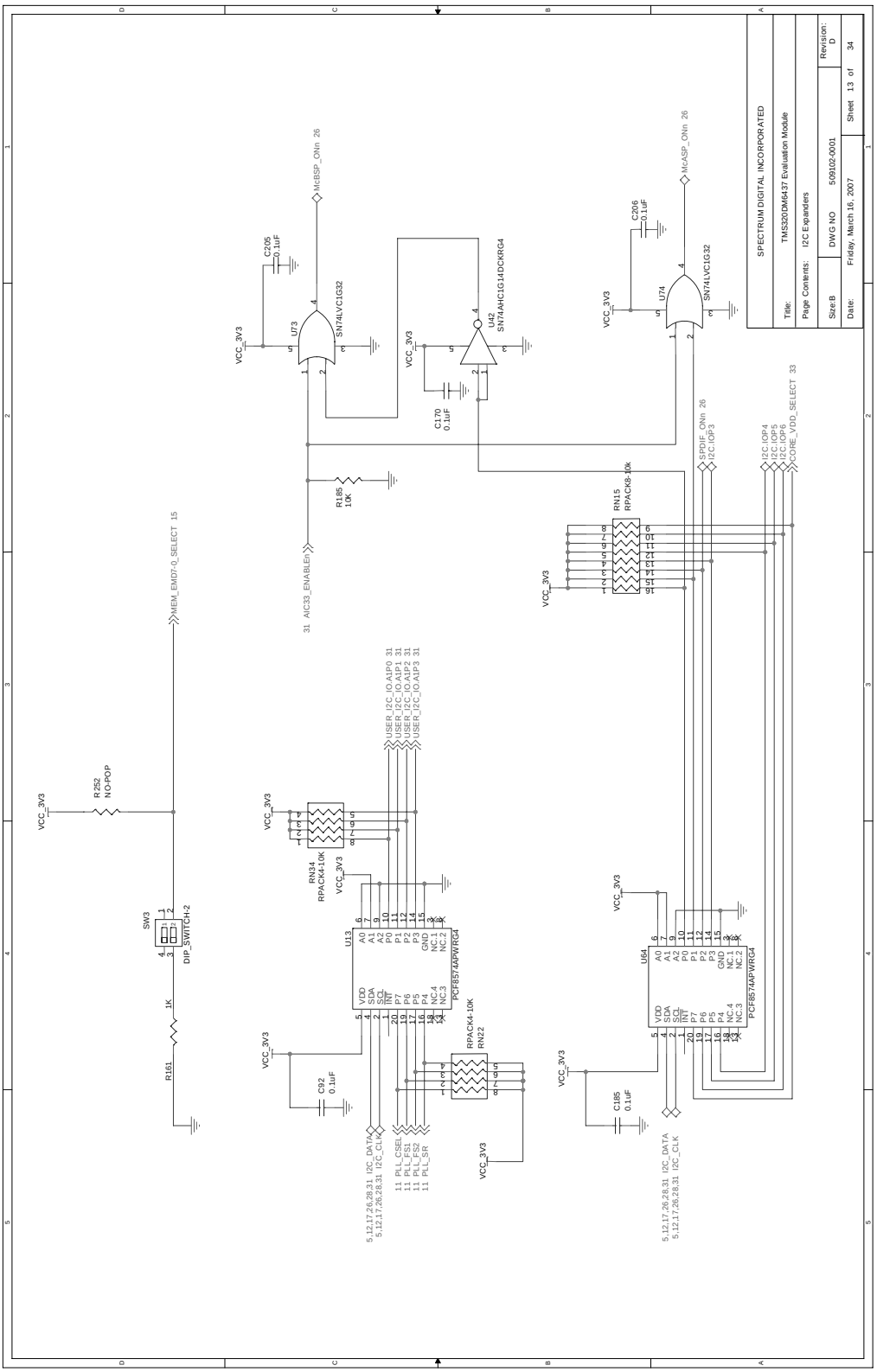
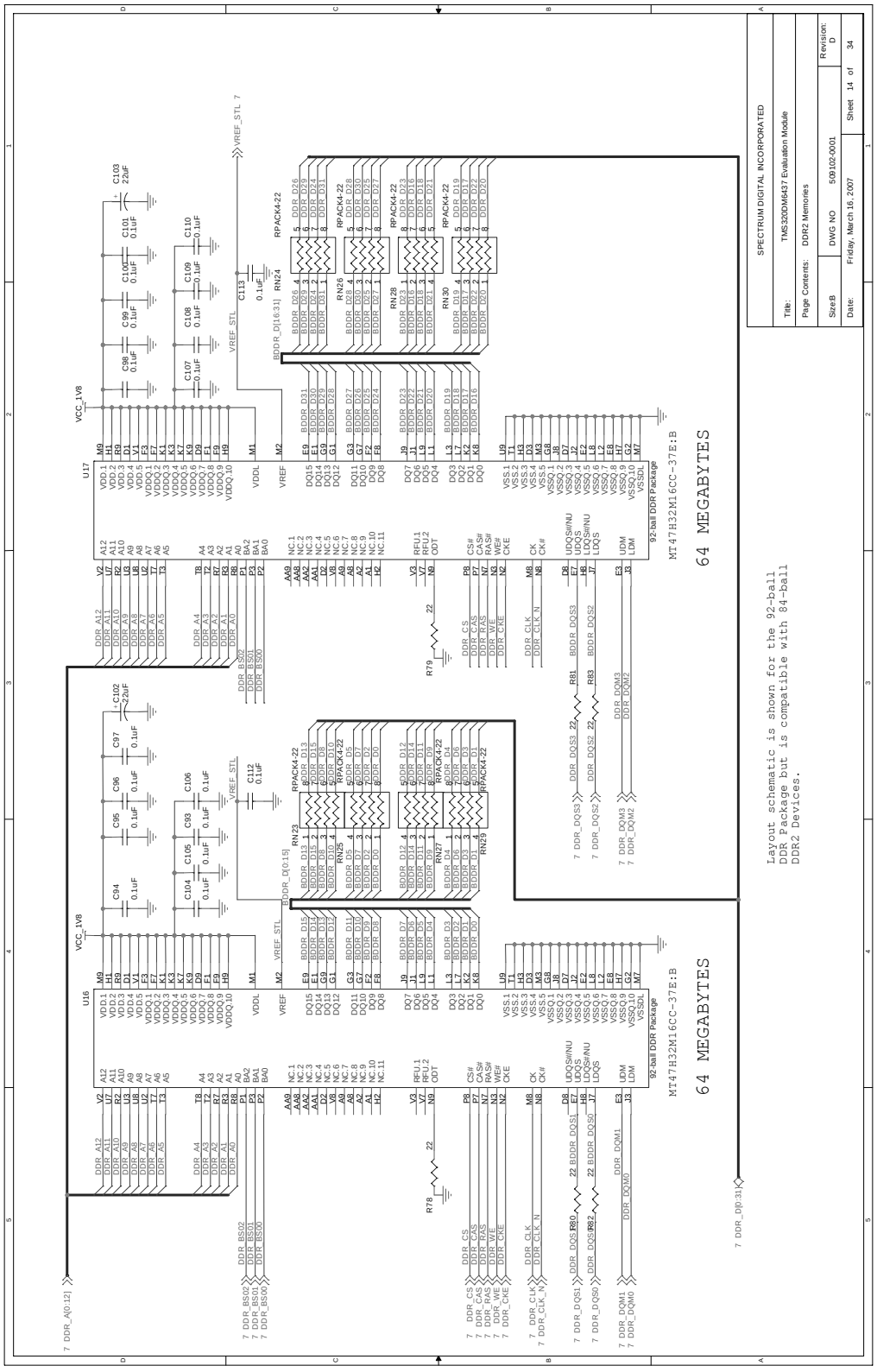
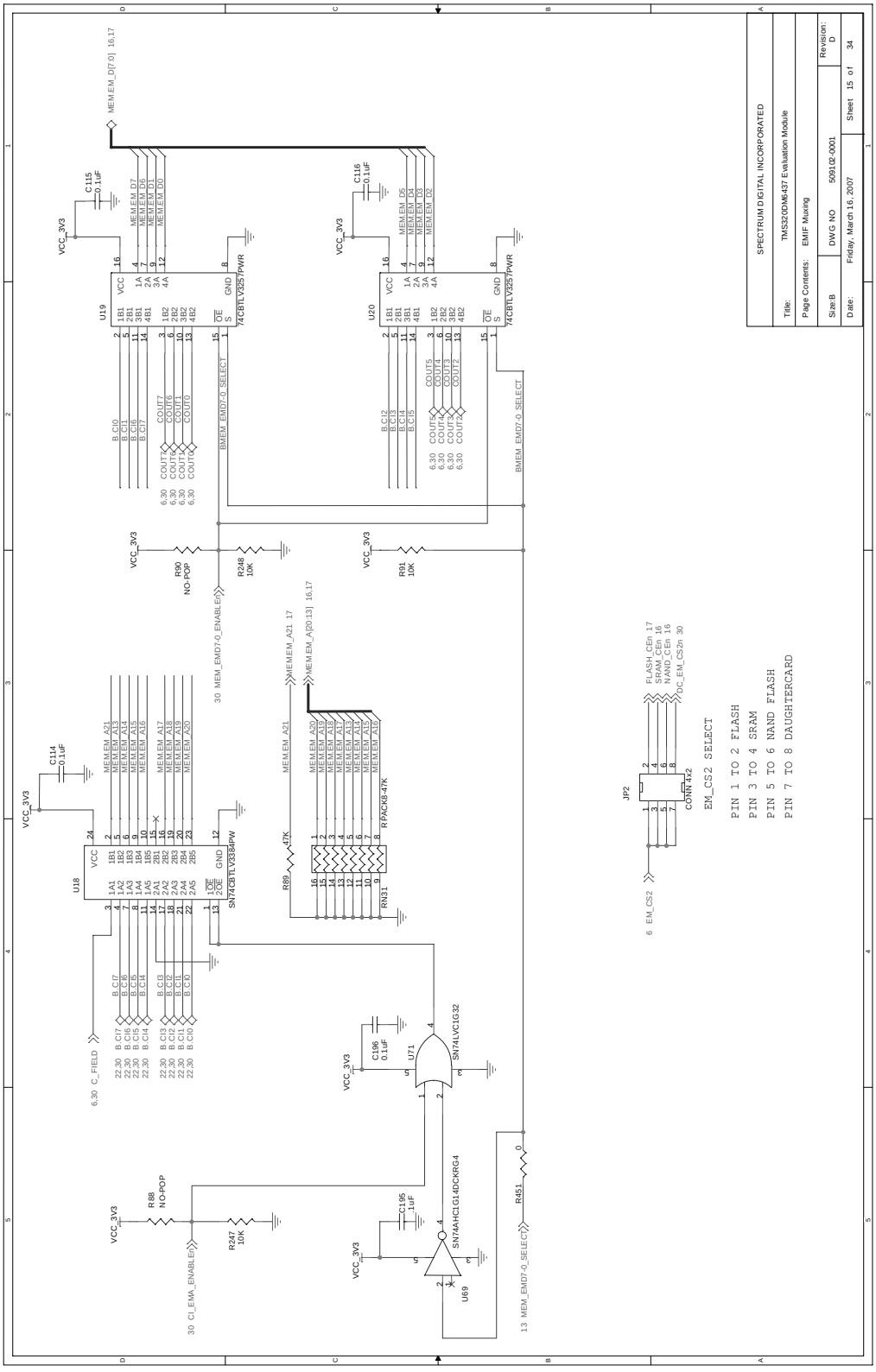
Size:B
DWG NO 5091I2-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 10 of 34
VCC_3V3
RPACK8-1.5K
RN13
SW1
DIP_SWITCH-8
R258 20K
R364 20K
RN12 RPACK8-20K
R176 20K
R175 20K
R43 20K
R42 20K
SW2
DIP_SWITCH-4
R173 1.5K
R44 1.5K
R45 1.5K
R174 1.5K
R1_AEM2
R2_AEM1
R3_AEM0
R4_AEM10
AEM_A00
AEM_BA0
AEM_BA1
AEM_A04
6,16,17,30
6,30 YOUT0_BOOTMODE0
6,30 YOUT1_BOOTMODE1
6,30 YOUT2_BOOTMODE2
6,30 YOUT3_BOOTMODE3
6,30 YOUT4_FASTBOOT
6,30 YOUT5
6,30 YOUT6

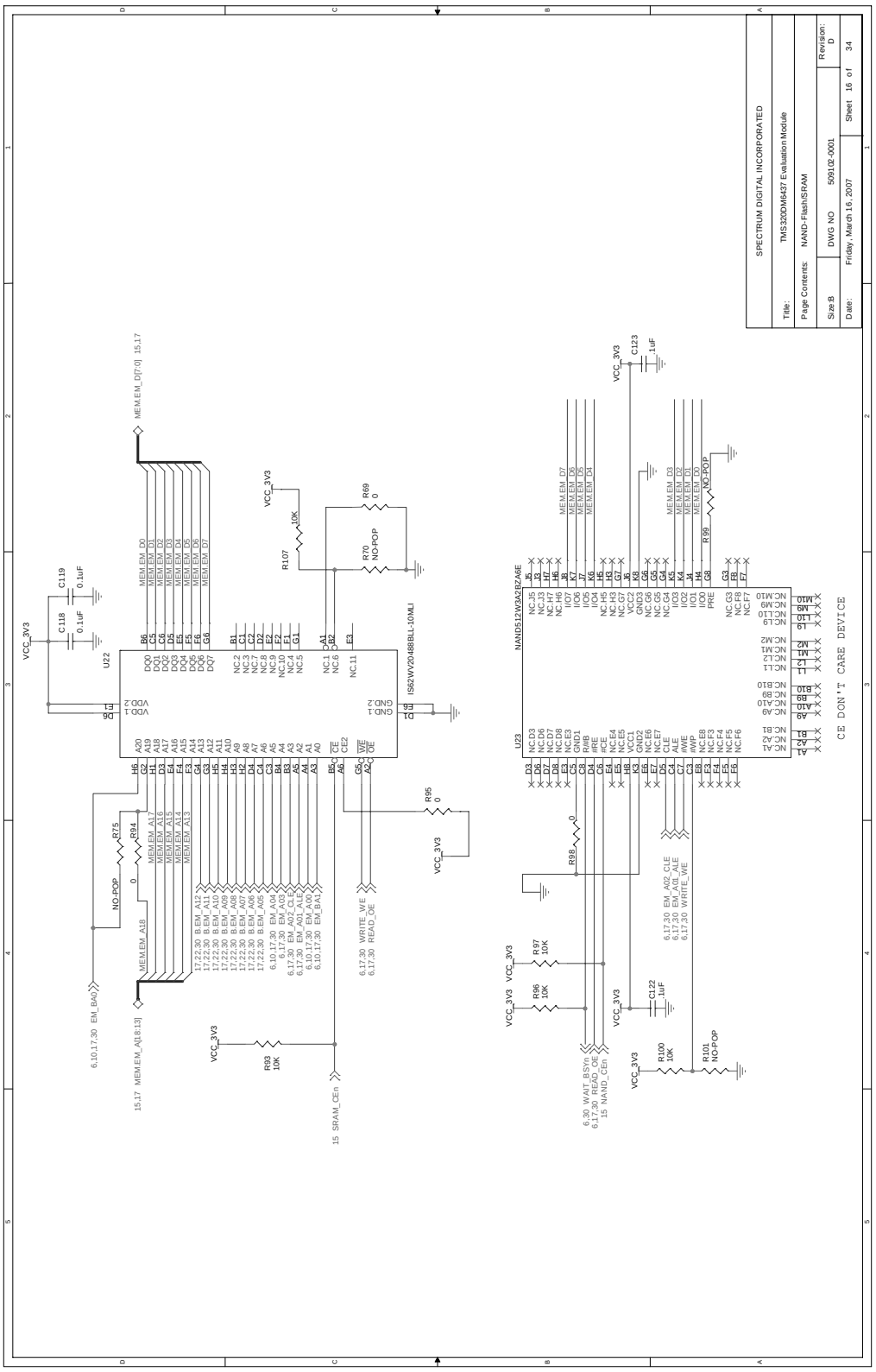

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: VIC
Size:B DWG NO 509102-0001 Revision: D
Date: Friday, March 16, 2007 Sheet 11 of 34
VCC_3V3
74LVC1G125DCKRG4
74LVC1G125DCKRG4
SN74CBTLV1G125
PLL1705IDBQ
P8CX100-27W
2N3904
27MHz
VID_CLK
AUDIO_CLK
TINPOL
PLL_CSEL
PLL_FS1
PLL_FS2
PLL_SR
PLL_PCLK
VIC_TINPOL_ENABLE
PWMIN
CLK_OUT
NO-POP

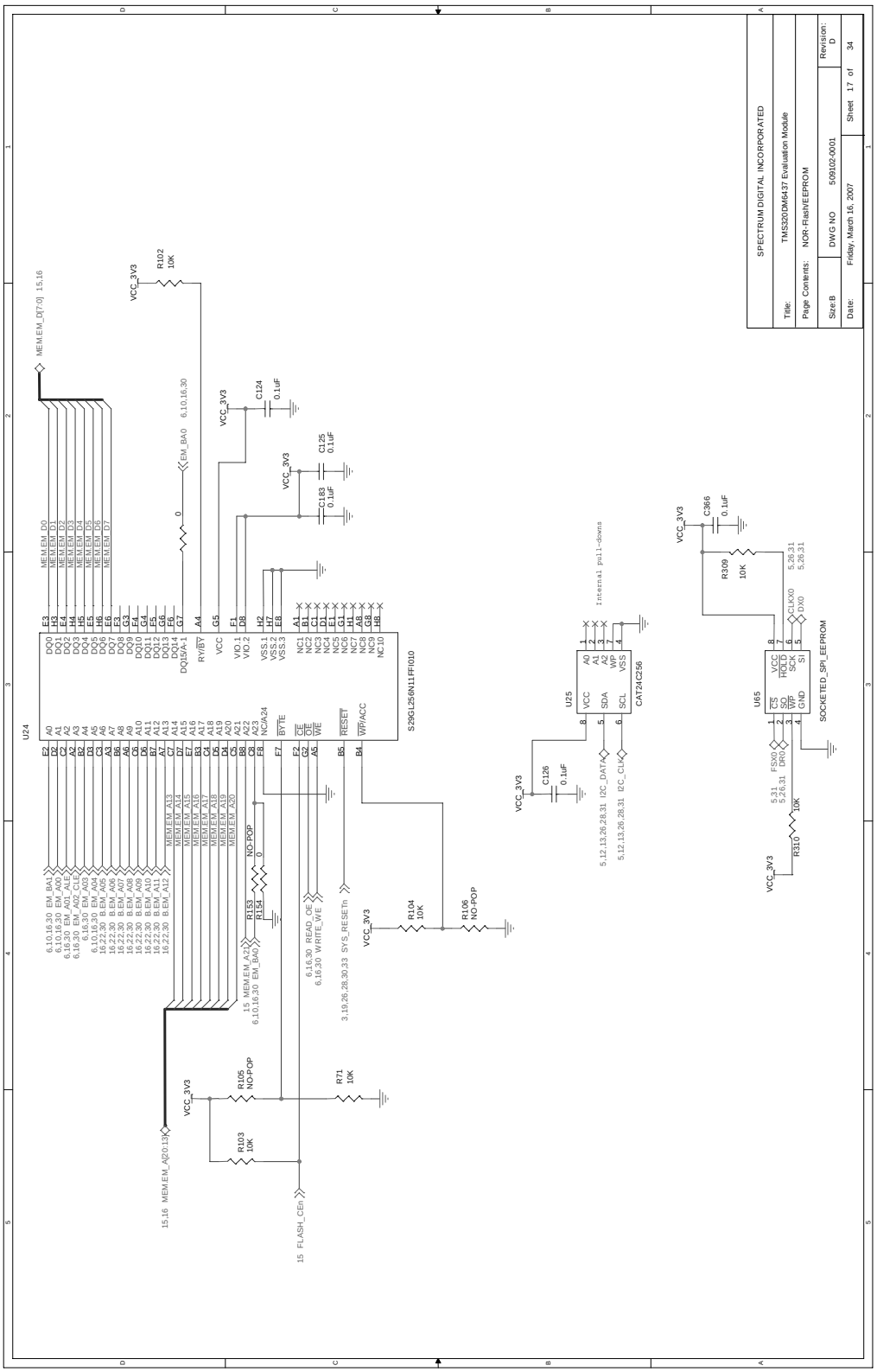

USER CONTROLLED LEDS
SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: I2C Expanders
Size: B
DWG NO 509102-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 12 of 34
VCC_3V3
R64 330
R65 330
R66 330
R67 330
DS1 LED_GRN
DS2 LED_GRN
DS3 LED_GRN
DS4 LED_RED
U11
PCF8574APWRG4
C91 .1uF
RN20 RPACK4-10K
31 USER_I2C_IO_ADP7
31 USER_I2C_IO_ADP6
R7 1K
RN38 RPACK4-1K
SW7 GSOJMSAKE
R17 1K
JP1 3 PIN JUMPER
SILKSCREEN: NTSC by pin 1 PAL by pin 3
RN37 RPACK8-10K
SW4 PADDLE DIP-4
SILKSCREEN: USER SWITCHES
U10
PCF8574APWRG4
C90 .1uF
R74 10K
C187 .1uF
U66
SN74AHC1G14DCKRG4
5,13,17,26,28,31 I2C_DATA
5,13,17,26,28,31 I2C_CLK
I2C_INT
25,32 VLYNQ_RESET

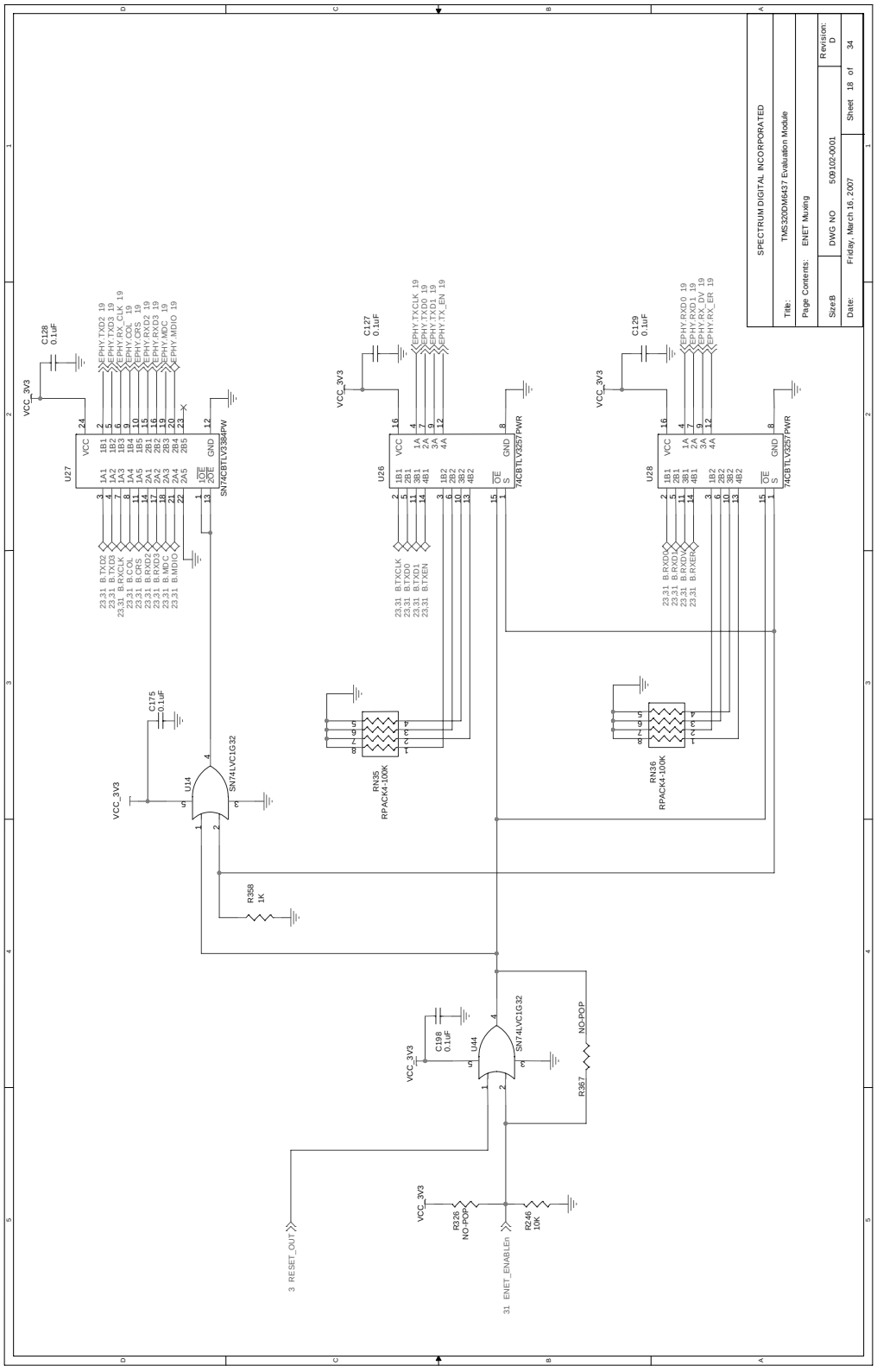

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: I2C Expanders
Size:B
DWG NO 509102-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 13 of 34
VCC_3V3
MCBSP_ONn 26
MCASP_ONn 26
SPDIF_ONn 26
I2C.IOP3
I2C.IOP4
I2C.IOP5
I2C.IOP6
CORE_VDD_SELECT 33
MEM_EMD7-0_SELECT 15
AIC33_ENABLEn 31
USER_I2C_IO.A1P0 31
USER_I2C_IO.A1P1 31
USER_I2C_IO.A1P2 31
USER_I2C_IO.A1P3 31
I2C_DATA 5,12,17,26,28,31
I2C_CLK 5,12,17,26,28,31
PLL_CSEL 11
PLL_FSEL 11
PLL_FS2 11
PLL_SR 11
U73 SN74LVC1G32
U42 SN74AHC1G14DCKRG4
U74 SN74LVC1G32
U13 PCF8574APWRG4
U64 PCF8574APWRG4
RN34 RPACK4-10K
RN15 RPACK8-10K
RN22 RPACK4-10K
SW3 DIP_SWITCH-2
R252 NO-POP
R161 1K
R185 10K
C205 0.1uF
C206 0.1uF
C170 0.1uF
C92 0.1uF
C185 0.1uF

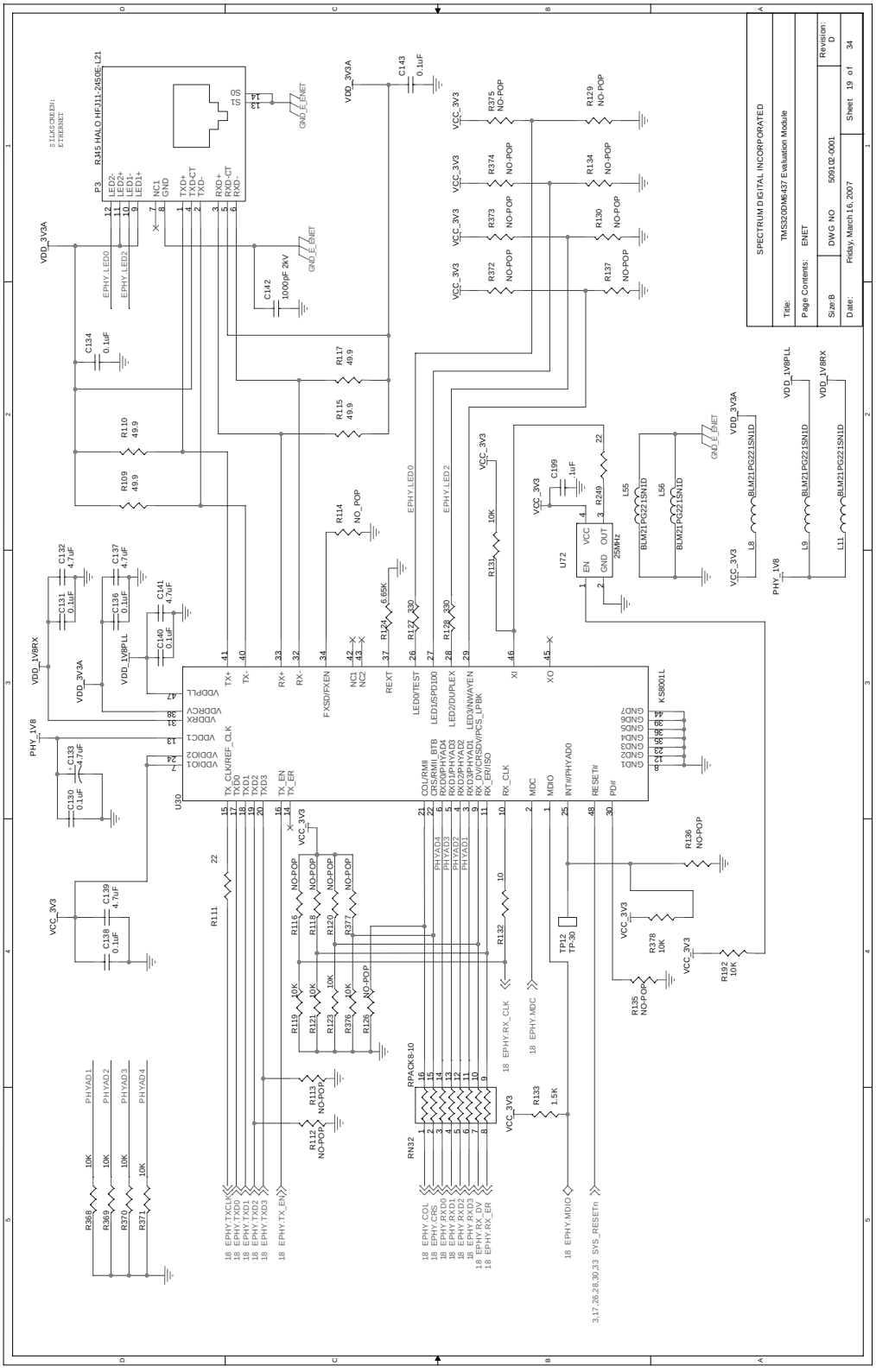

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: DDR2 Memories
Size:B
DWG NO 509102-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 14 of 34
Layout schematic is shown for the 92-ball
DDR Package but is compatible with 84-ball
DDR2 Devices.
64 MEGABYTES
MT47H32M16CC-37E:B
92-ball DDR Package
U16
U17
VCC_1V8
VREF_STL
VREF_STL_7
7 DDR_A[0:12]
7 DDR_D[0:31]
7 DDR_BS02
7 DDR_BS01
7 DDR_BS00
7 DDR_CAS
7 DDR_RAS
7 DDR_WE
7 DDR_CKE
7 DDR_CLK
7 DDR_CLK_N
7 DDR_DQS3
7 DDR_DQS2
7 DDR_DQM3
7 DDR_DQM2
7 DDR_DQS1
7 DDR_DQS0
7 DDR_DQM1
7 DDR_DQM0
R78
R79
R80
R81
R82
R83
RN23
RN24
RN25
RN26
RN27
RN28
RN29
RN30
RPACK4-22

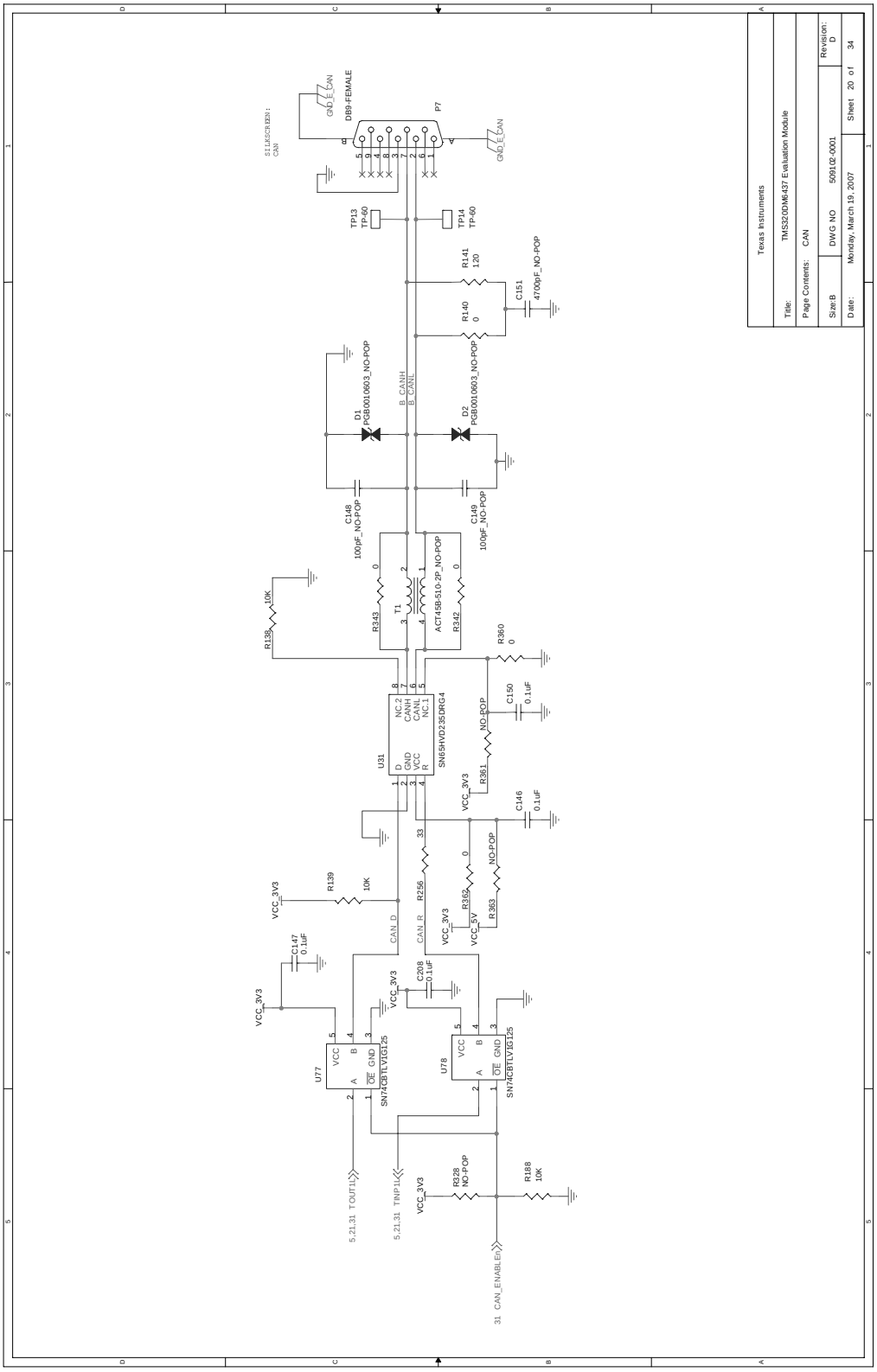

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: EMIF Muxing
Size:B DWG NO 5091l02-0001 Revision: D
Date: Friday, March 16, 2007 Sheet 15 of 34
EM_CS2 SELECT
PIN 1 TO 2 FLASH
PIN 3 TO 4 SRAM
PIN 5 TO 6 NAND FLASH
PIN 7 TO 8 DAUGHTERCARD
U19
U20
U18
U71
U69
JP2
R90 NO-POP
R248 10K
R91 10K
R89 47K
R88 NO-POP
R247 10K
R451 0
C114 0.1uF
C115 0.1uF
C116 0.1uF
C196 0.1uF
C195 1uF
RN31 RPACK8-47K
VCC_3V3
BMEM_EMD7-0_SELECT
MEM.EM_D[7:0] 16,17
MEM.EM_A[20:13] 16,17
MEM.EM_A21 17
30 MEM_EMD7-0_ENABLE
13 MEM_EMD7-0_SELECT
30 CI_EMA_ENABLE
6,30 C_FIELD
6 EM_CS2
FLASH_CEn 17
SRAM_CEn 16
NAND_CEn 16
DC_EM_CS2n 30
74CBTLV3257PWR
SN74CBTLV3384PW
SN74LVC1G32
SN74AHC1G14DCKRG4
CONN 4x2

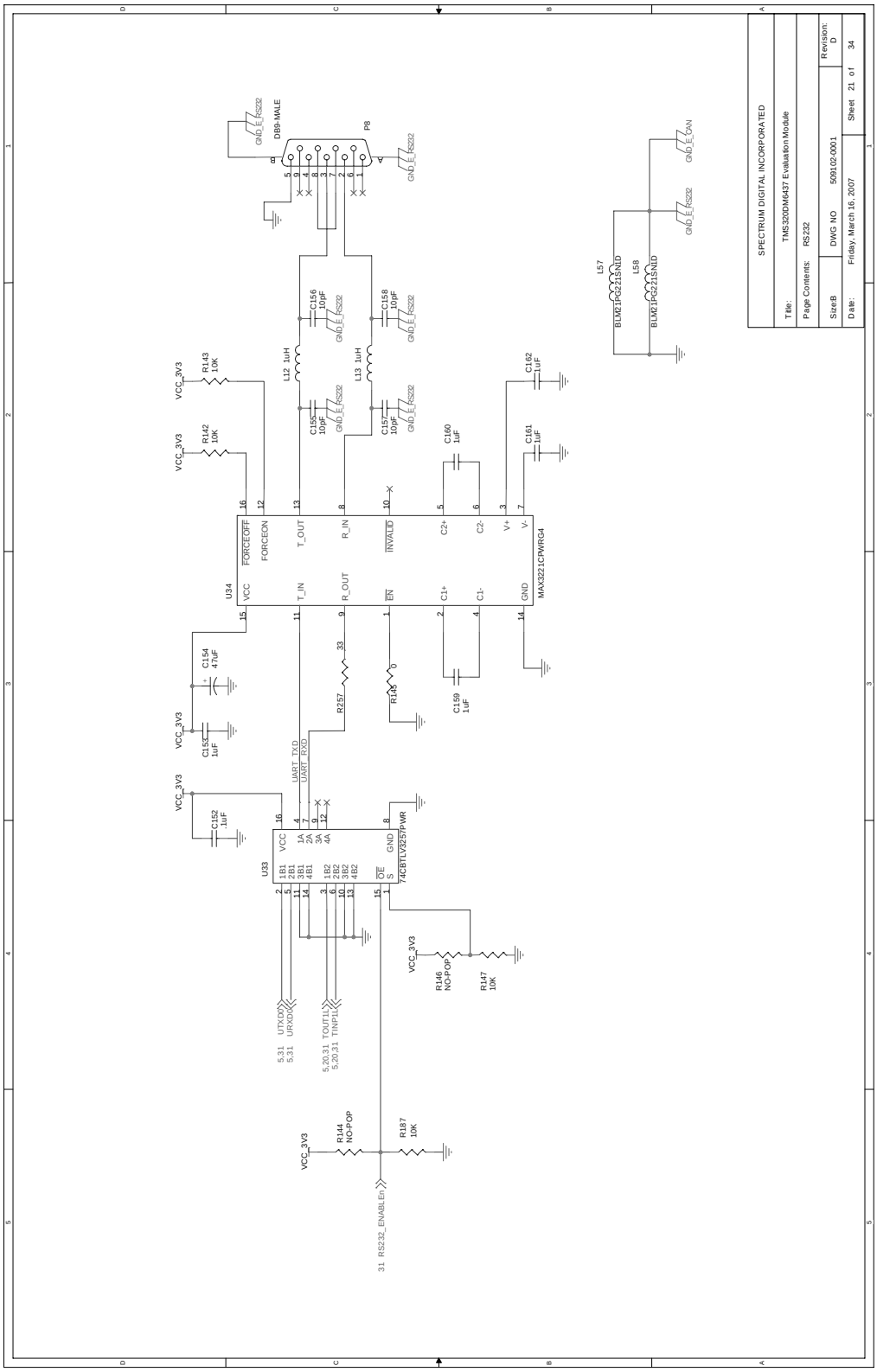

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: NAND-Flash/SRAM
Size:B
DWG NO 509102-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 16 of 34
CE DON'T CARE DEVICE
U2
U23
NAND512W3A2BZA6E
IS62WV20488BLL-10MLI
MEM.EM_D[7:0] 15,17
MEM.EM_A[0:13]
VCC_3V3
NO-POP
SRAM_CEn
WRITE_WE
READ_OE
WAIT_BSYn
NAND_CEn
EM_BA0
EM_BA1
EM_A02_CLE
EM_A01_ALE

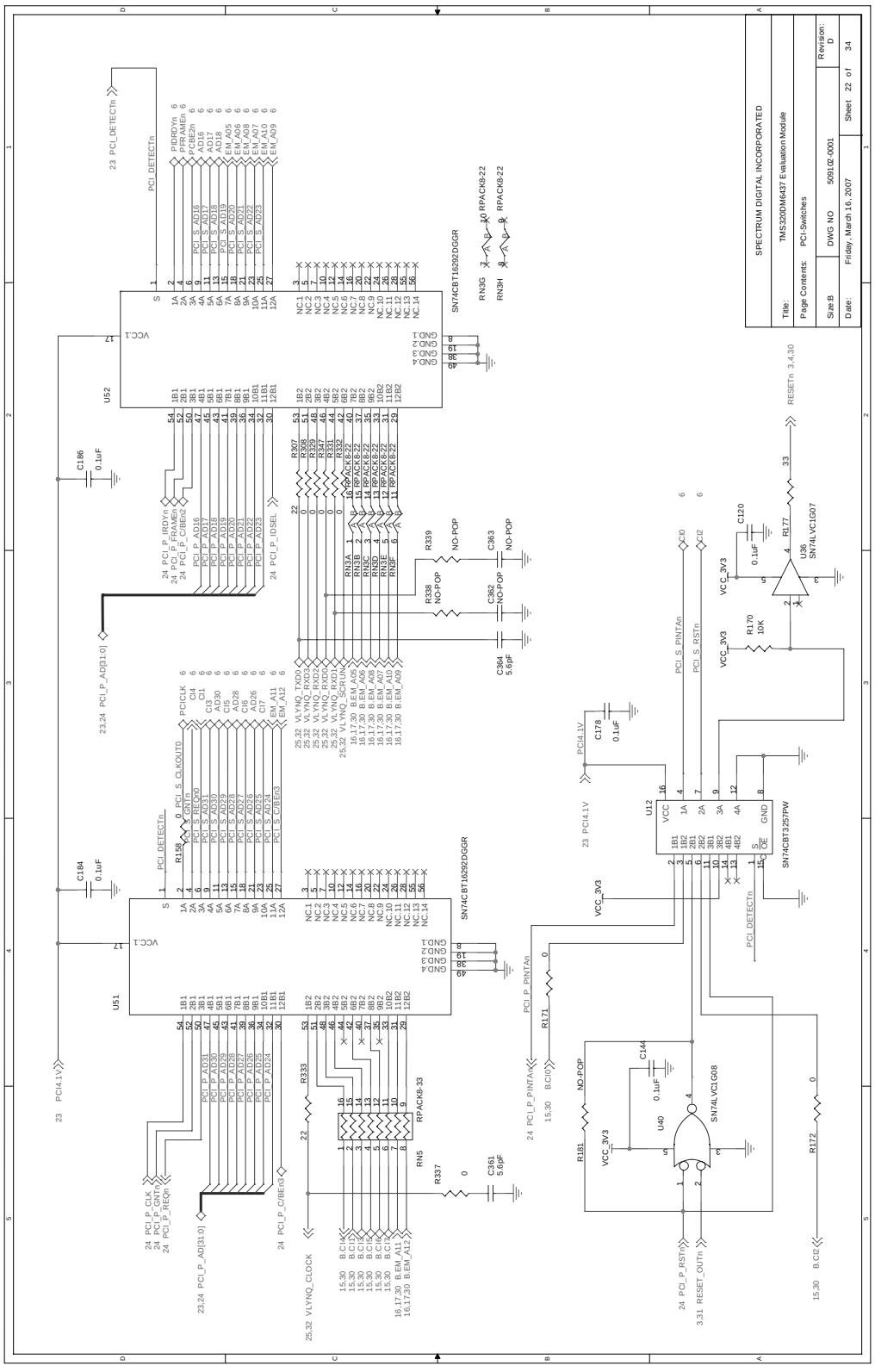

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: NOR-Flash/EEPROM
Size:B
DWG NO 509102-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 17 of 34
U24
S29GL256N11FFI010
U25
CAT24C256
U65
SOCKETED_SPI_EEPROM
MEM.EM_D[7:0] 15,16
VCC_3V3
R102 10K
C124 0.1uF
C125 0.1uF
C183 0.1uF
C126 0.1uF
C366 0.1uF
R309 10K
R310 10K
R71 10K
R103 10K
R104 10K
R105 NO-POP
R106 NO-POP
R153 0
R154 0
NO-POP
EM_BA0 6,10,16,30
MEM.EM_A[20:13]
15 FLASH_CE0
READ_CE
WRITE_WE
SYS_RESETn
I2C_DATA
I2C_CLK
CLKX0
DX0
FSX0
DR0
Internal pull-downs

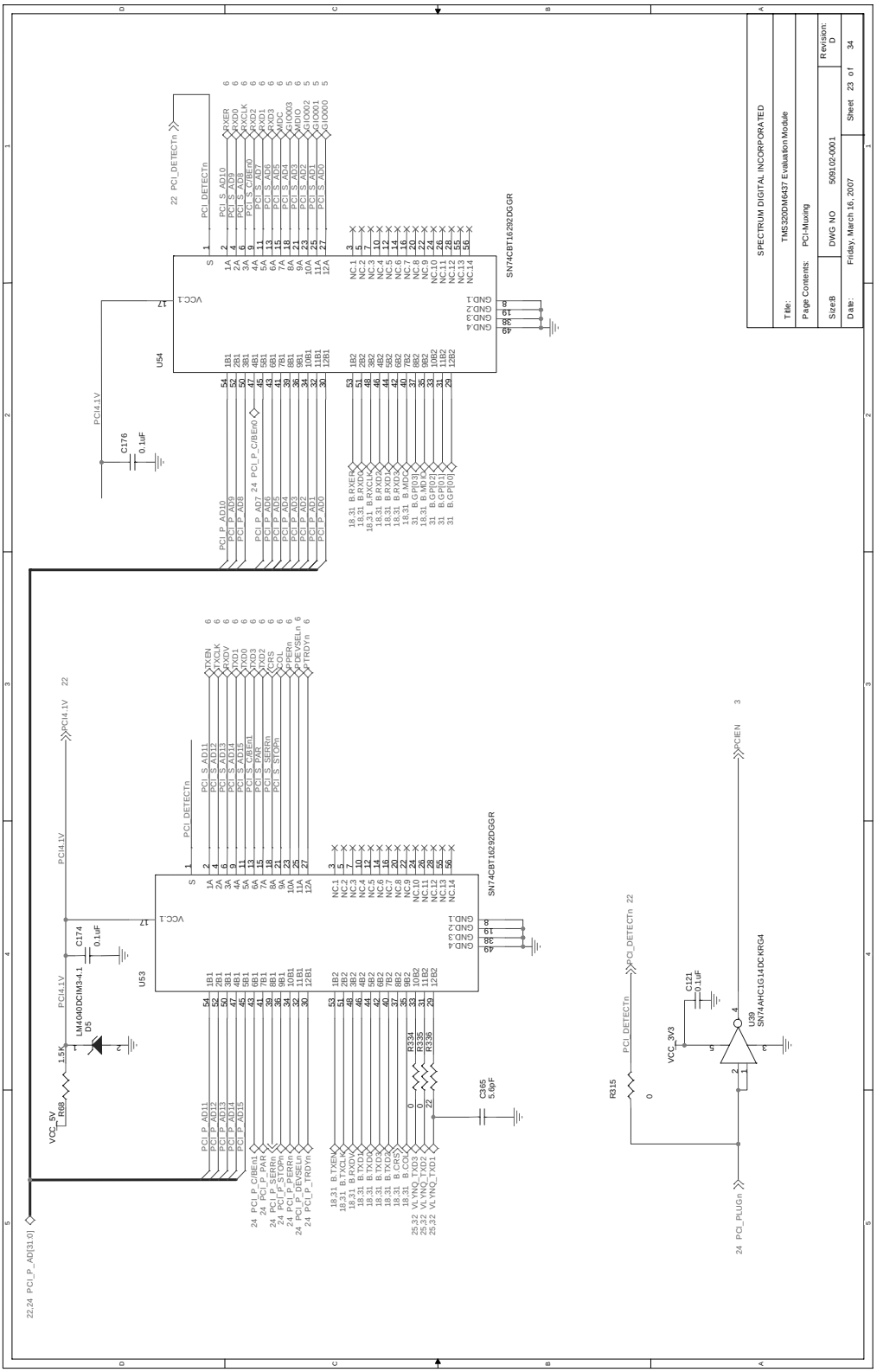

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: ENET Muxing
Size:B
DWG NO 509102-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 18 of 34
VCC_3V3
C128 0.1uF
C127 0.1uF
C129 0.1uF
C175 0.1uF
C198 0.1uF
U27 SN74CBTLV3384PW
U26 74CBTLV3257PWR
U28 74CBTLV3257PWR
U14 SN74LVC1G32
U44 SN74LVC1G32
RN35 RPACK4-100K
RN36 RPACK4-100K
R358 1K
R367 NO-POP
R328 NO-POP
R248 10K
EPHY.TXD2 19
EPHY.TXD3 19
EPHY.RX_CLK 19
EPHY.COL 19
EPHY.CRS 19
EPHY.RXD2 19
EPHY.RXD3 19
EPHY.MDC 19
EPHY.MDIO 19
EPHY.TXCLK 19
EPHY.TXD0 19
EPHY.TXD1 19
EPHY.TX_EN 19
EPHY.RXD0 19
EPHY.RXD1 19
EPHY.RX_DV 19
EPHY.RX_ER 19
23.31 B.TXD2
23.31 B.TXD3
23.31 B.RXCLK
23.31 B.COL
23.31 B.CRS
23.31 B.RXD2
23.31 B.RXD3
23.31 B.MDC
23.31 B.MDIO
23.31 B.TXCLK
23.31 B.TXD0
23.31 B.TXD1
23.31 B.TXEN
23.31 B.RXD0
23.31 B.RXD1
23.31 B.RXD2
23.31 B.RXER
3 RESET_OUT
31 ENET_ENABLEn

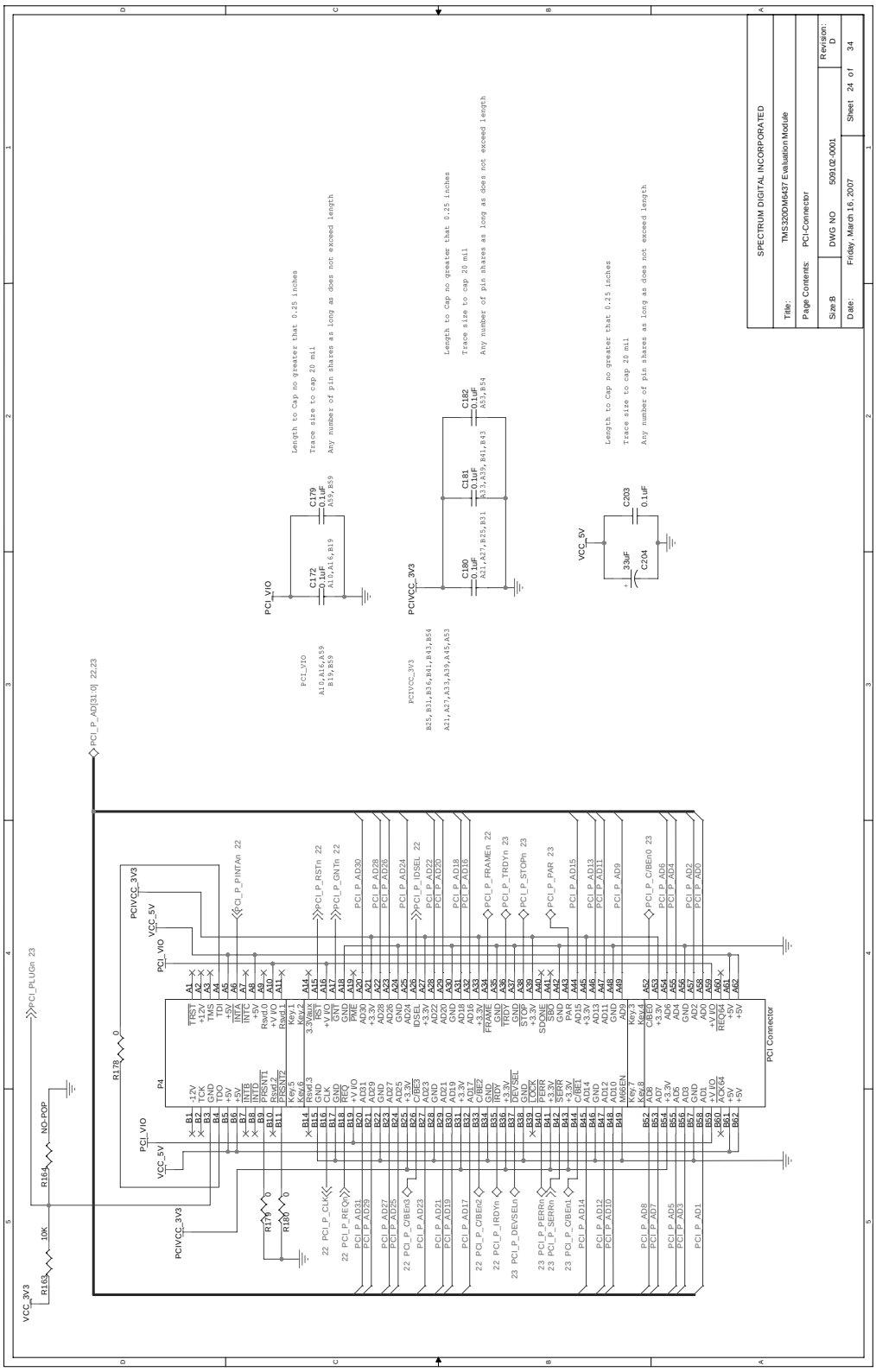

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: ENET
Size:B DWG NO 5091Z0-0001 Revision: D
Date: Friday, March 16, 2007 Sheet 19 of 34
P3 RJ45 HALO HFJ11-2450E-L21
U50
U72
RN32
VDD_3V3A
VCC_3V3
PHY_1V8
VDD_1V8PLL
VDD_1V8RX
GND_E_ENET
EPHY.LED0
EPHY.LED2
EPHY.RX_CLK
EPHY.MDC
EPHY.MDIO
SYS_RESETn

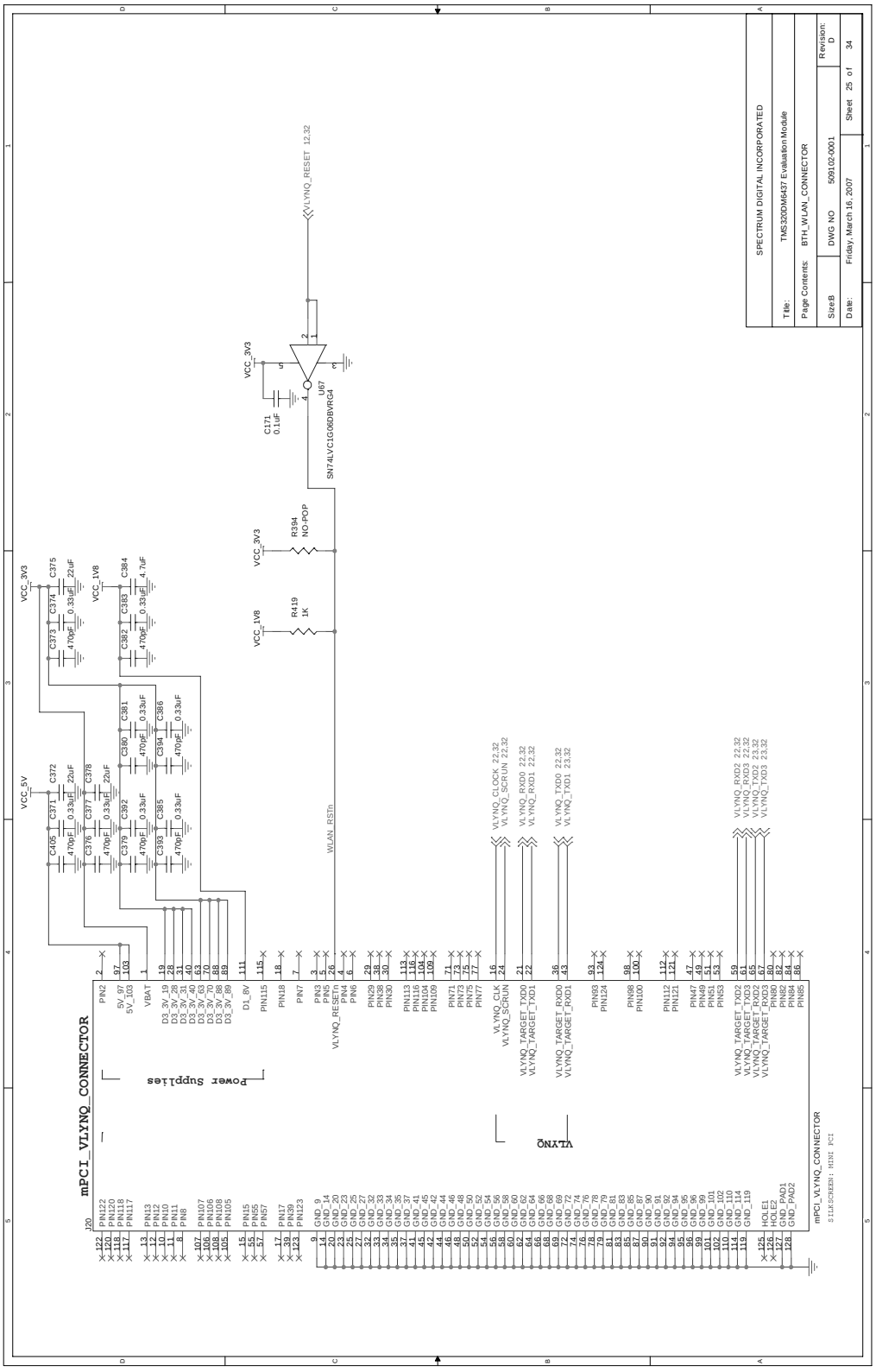

Texas Instruments
Title: TMS320DM6437 Evaluation Module
Page Contents: CAN
Size:B
DWG NO 509102-0001
Revision: D
Date: Monday, March 19, 2007
Sheet 20 of 34
DB9-FEMALE
P7
TP13 TP-60
TP14 TP-60
R141 120
R140 0
C151 4700pF_NO-POP
D1 PGB0010603_NO-POP
D2 PGB0010603_NO-POP
B_CANH
B_CANL
C148 100pF_NO-POP
C149 100pF_NO-POP
T1 ACT45B-510-2P_NO-POP
R343
R342
R138 10K
R360 0
C150 0.1uF
R361 NO-POP
U31 SN65HVD235DRG4
C146 0.1uF
R139 10K
R256 33
R362 0
R363 NO-POP
CAN_D
CAN_R
C147 0.1uF
C208 0.1uF
U77 SN74CBTLV1G125
U78 SN74CBTLV1G125
R328 NO-POP
R188 10K
5,21,31 TOUT1
5,21,31 TINP1
31 CAN_ENABLE

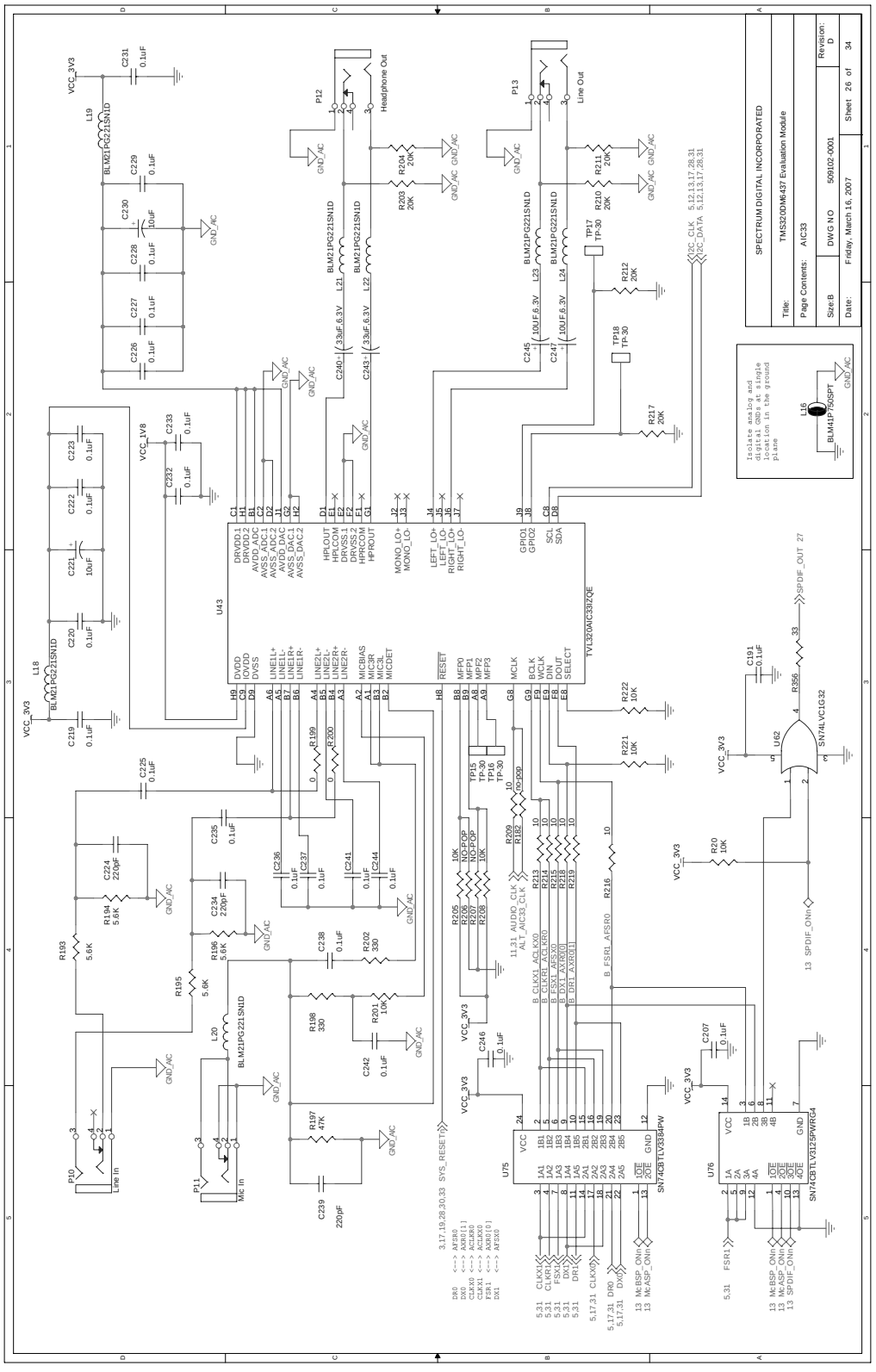

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: RS232
Size:B DWG NO 5091102-0001 Revision: D
Date: Friday, March 16, 2007 Sheet 21 of 34
DB9-MALE
P8
U34
MAX3221CPWRG4
U33
74CBTLV3257PWR
VCC_3V3
GND_E_RS232
GND_E_CAN
UART_TXD
UART_RXD
T_OUT
R_IN
R_OUT
T_IN
INVALID
FORCEON
FORCEOFF
C2+
C2-
V+
V-
C1+
C1-
EN
VCC
GND
R143 10K
R142 10K
R257 33
R145 0
R146 NO-POP
R147 10K
R144 NO-POP
R187 10K
L12 1uH
L13 1uH
L57 BLM21PG221SN1D
L58 BLM21PG221SN1D
C152 .1uF
C153 1uF
C154 47uF
C155 10pF
C156 10pF
C157 10pF
C158 10pF
C159 1uF
C160 1uF
C161 1uF
C162 1uF
5,31 UTXD[0]
5,31 URXD[0]
5,20,31 TOUT1L
5,20,31 TINP1L
31 RS232_ENABLEn

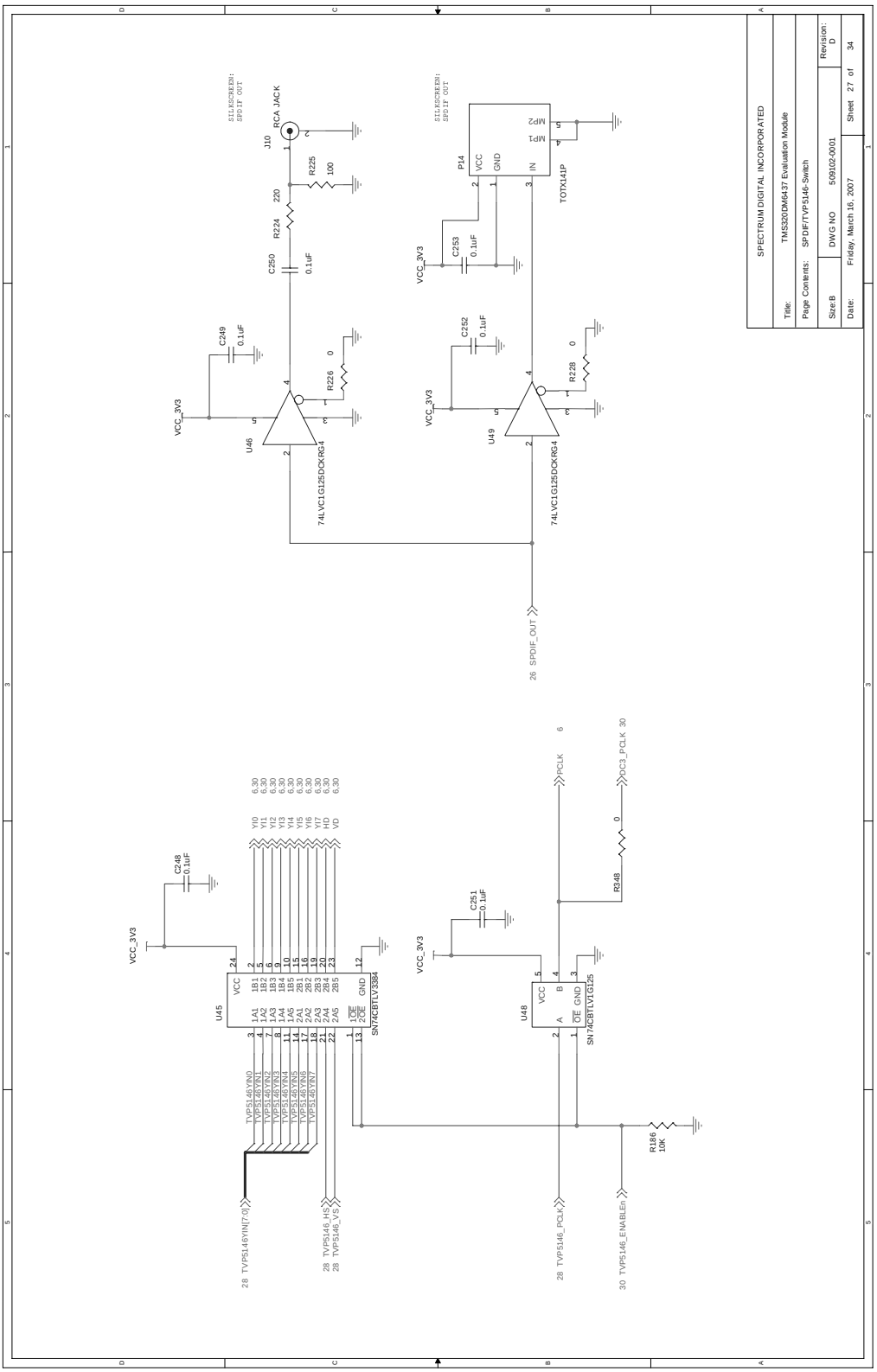

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: PCI-Switches
Size:B
DWG NO 5091l2-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 22 of 34
U51
U52
U12
U40
U39
SN74CBT16292DGGR
SN74CBT3257PW
SN74LVC1G08
SN74LVC1G07
PCI_DETECTn
PCI_P_PINTAn
PCI_S_PINTAn
PCI_S_RSTn
VCC_3V3
PCI4.1V
RESETn 3,4,30
PCI_P_RSTn
RESET_OUTn
VLYNQ_CLOCK
PCI_P_CLK
PCI_P_GNTn
PCI_P_REQn
PCI_P_AD[31:0]
PCI_P_C/BEn[3:0]
PCI_P_IRDYn
PCI_P_FRAMEn
PCI_P_C/BE#2
PCI_P_IDSEL
PCI_P_AD[31:0]
PCI_S_CLKOUT0
PCI_S_REQn0
PCI_S_C/BEn3
PCI_S_AD[31:0]
PCI_S_IRDYn
PCI_S_FRAMEn
PCI_S_C/BE#2
PCI_S_IDSEL
PCI_S_AD[31:0]
RPACK8-33
RPACK8-22
NO-POP
C184
C186
C178
C120
C144
C361
C362
C363
C364
R158
R307
R308
R309
R317
R331
R332
R333
R337
R338
R339
R170
R171
R172
R177
R181
RN5
RN3A
RN3B
RN3C
RN3D
RN3E
RN3F
RN3G
RN3H

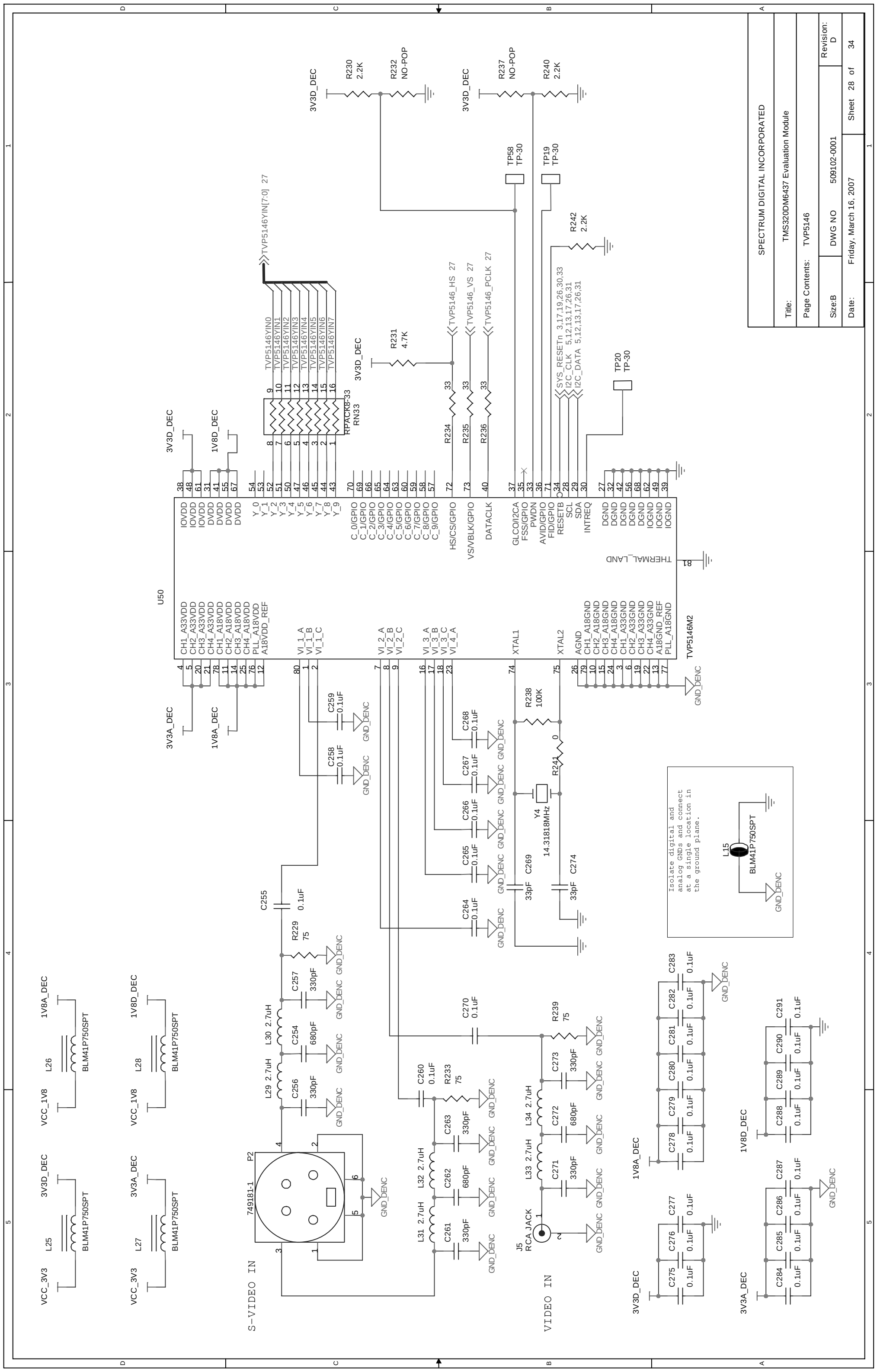

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: PCI-Muxing
Size:B
DWG NO 509102-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 23 of 34
U54
SN74CBT16292DGGR
U53
SN74CBT16232DGGR
U39
SN74AHC1G14DCKRG4
LM4040DCIM3-4.1
D5
R68
1.5K
C174
0.1uF
C176
0.1uF
C121
0.1uF
C356
5.6pF
R315
R334
R335
R336
VCC_5V
VCC_3V3
PCI4.1V
PCI_DETECTn
PCIEN
PCI_PLUGn
PCI_P_AD[31:0]

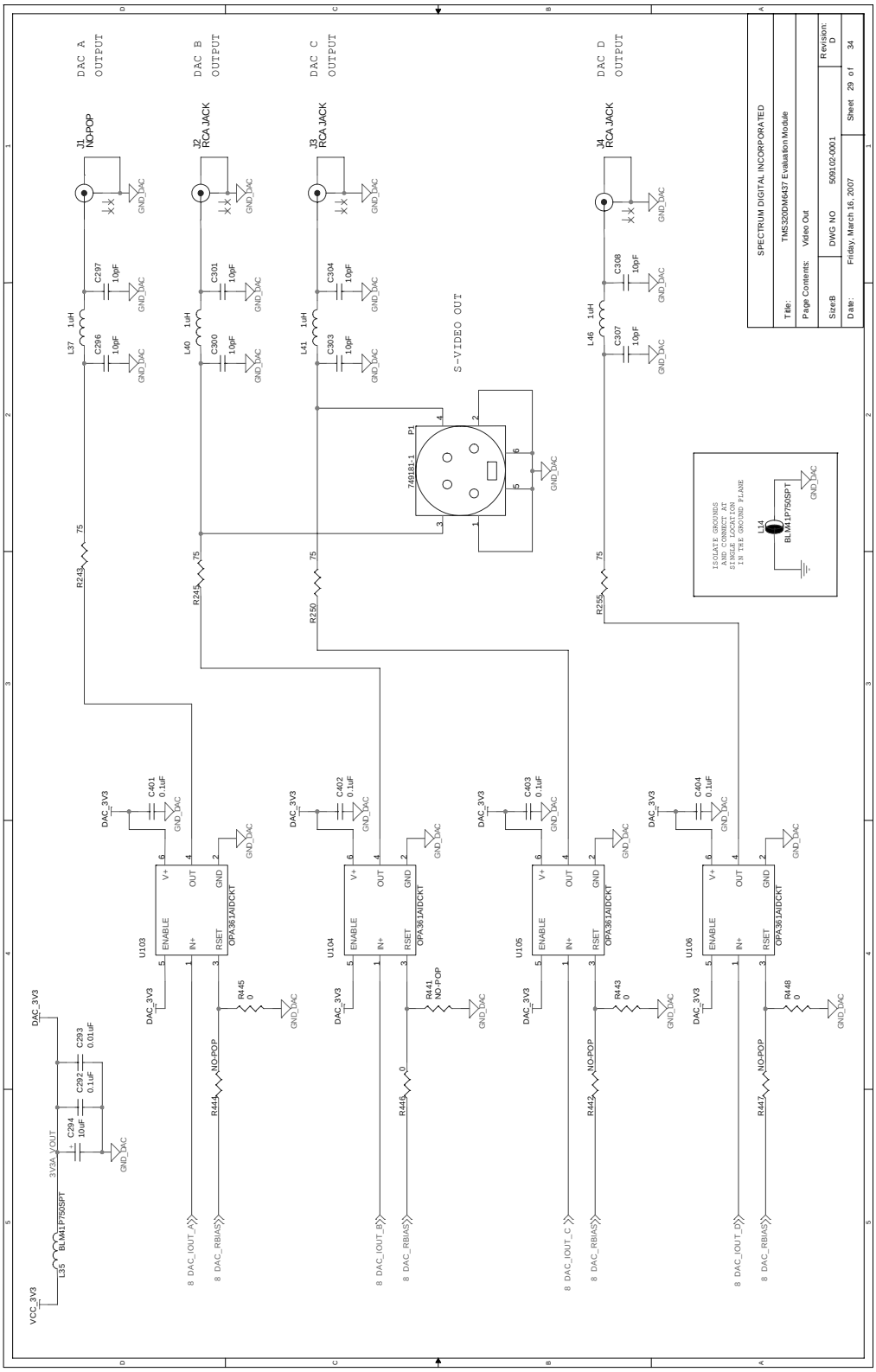

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: PCI-Connector
Size:B
DWG NO 509102-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 24 of 34
PCI Connector
P4
R178 0
R164 NO-POP
R163 10K
R174 0
R180 0
C172 0.1uF
C179 0.1uF
C180 0.1uF
C181 0.1uF
C182 0.1uF
C203 0.1uF
C204 .33uF
PCI_P_AD[31:0] 22,23
PCI_PLUGn 23
PCI_VIO
PCIVCC_3V3
VCC_5V
VCC_3V3
VCC_6V
Length to Cap no greater that 0.25 inches
Trace size to cap 20 mil
Any number of pin shares as long as does not exceed length

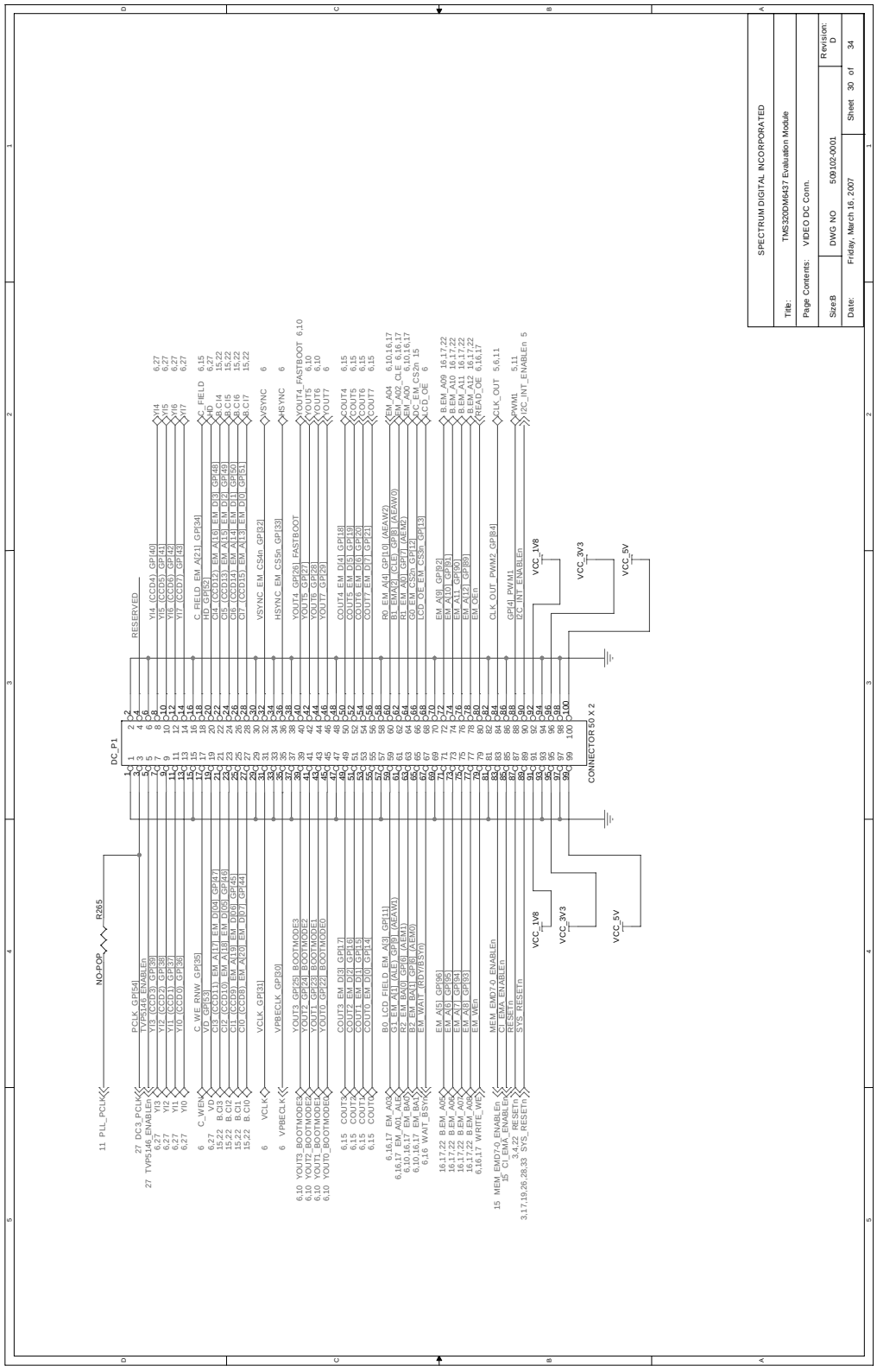

mPCI_VLYNQ_CONNECTOR
Power Supplies
VLYNQ
SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: BTH_WLAN_CONNECTOR
Size:B DWG NO 509102-0001 Revision: D
Date: Friday, March 16, 2007 Sheet 25 of 34
mPCI_VLYNQ_CONNECTOR
SILKSCREEN: MINI PCI
SN74LVC1G06DBVRG4
VLYNQ_RESET 12,32
WLAN_RSTn
VLYNQ_CLOCK 22,32
VLYNQ_SCRUN 22,32
VLYNQ_RXD0 23,32
VLYNQ_RXD1 23,32
VLYNQ_TXD0 23,32
VLYNQ_TXD1 23,32
VLYNQ_RXD2 22,32
VLYNQ_RXD3 22,32
VLYNQ_TXD2 23,32
VLYNQ_TXD3 23,32

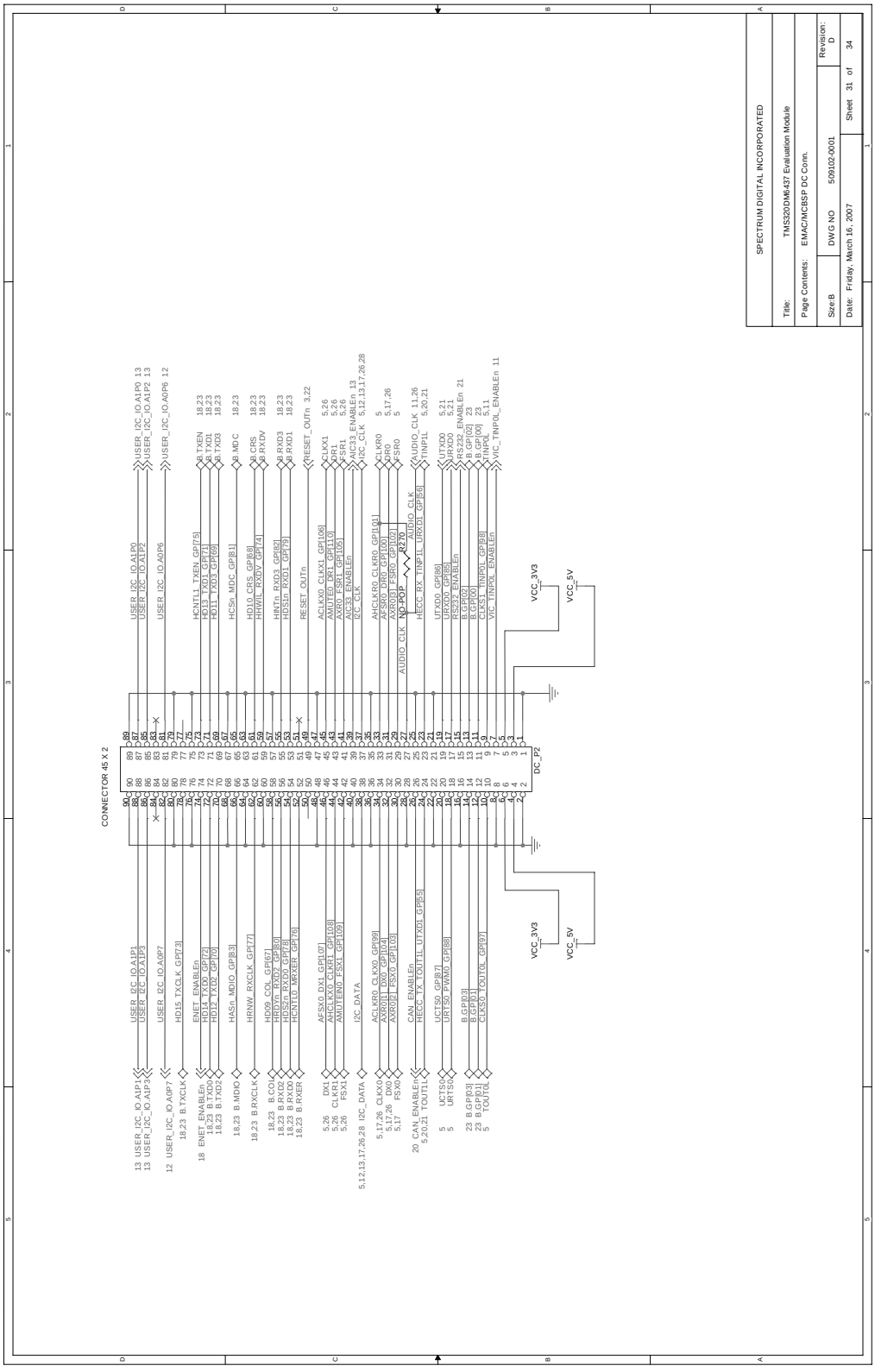

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: AIC33
Size:B
DWG NO 509102-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 26 of 34
U43
TVL320AIC33IZQE
U75
SN74CBTLV3384PW
U76
SN74CBTLV3125PWRG4
U62
SN74LVC1G32
Line In
Mic In
Headphone Out
Line Out
Isolate analog and digital GNDs at single location in the ground plane

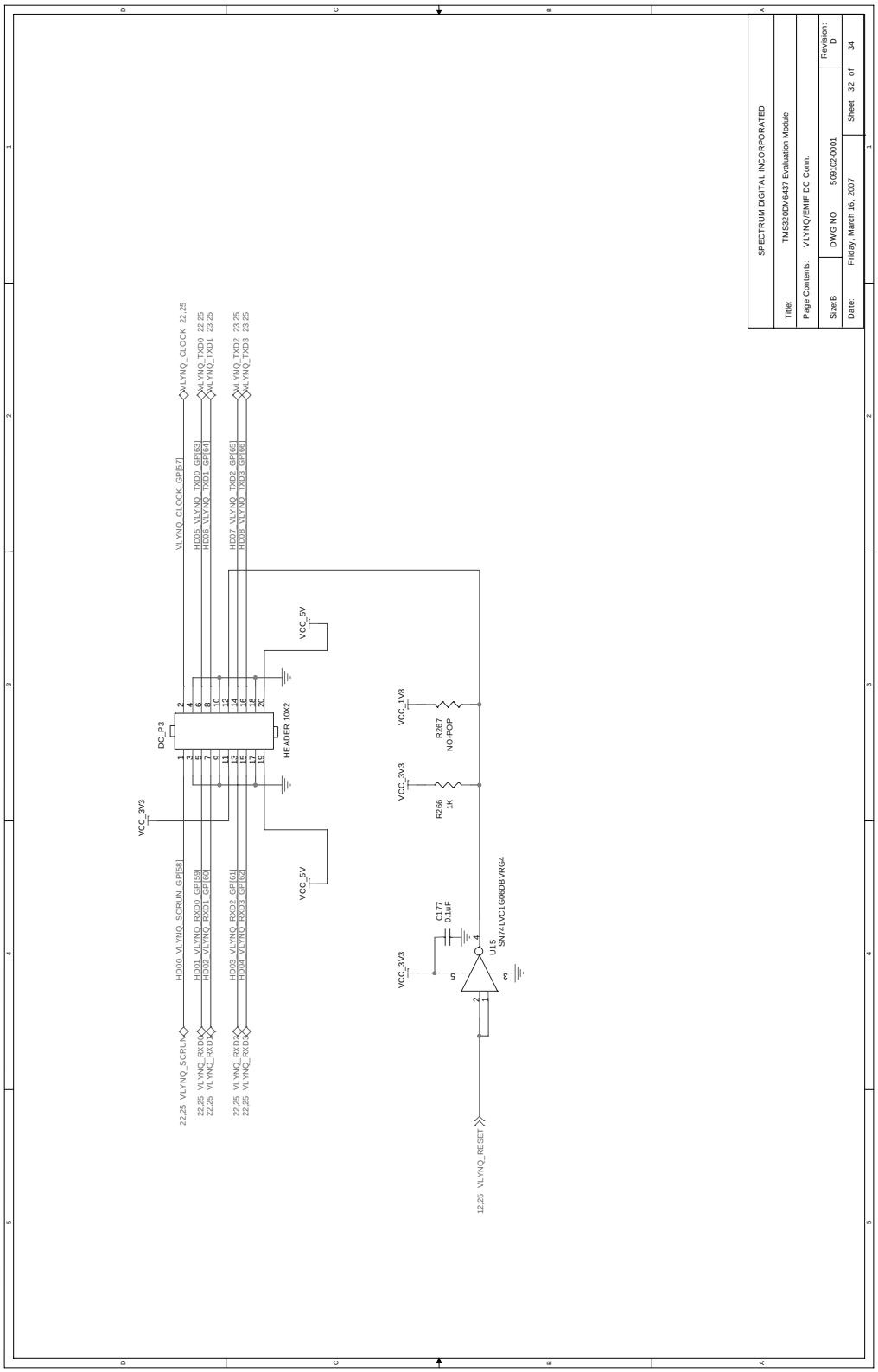

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: SPDIF/TVP5146-Switch
Size:B
DWG NO 509102-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 27 of 34
J10 RCA JACK
R225 100
R224 220
C250 0.1uF
C249 0.1uF
R226 0
U46 74LVC1G125DCKRG4
P14 TOTX141P
C253 0.1uF
C252 0.1uF
R228 0
U49 74LVC1G125DCKRG4
26 SPDIF_OUT
C248 0.1uF
U45 SN74CBTLV3384
C251 0.1uF
R248 0
U48 SN74CBTLV1G125
R186 10K
28 TVP5146YIN[7:0]
28 TVP5146_HS
28 TVP5146_VS
28 TVP5146_PCLK
30 TVP5146_ENABLEn
PCLK
DC3_PCLK
VCC_3V3

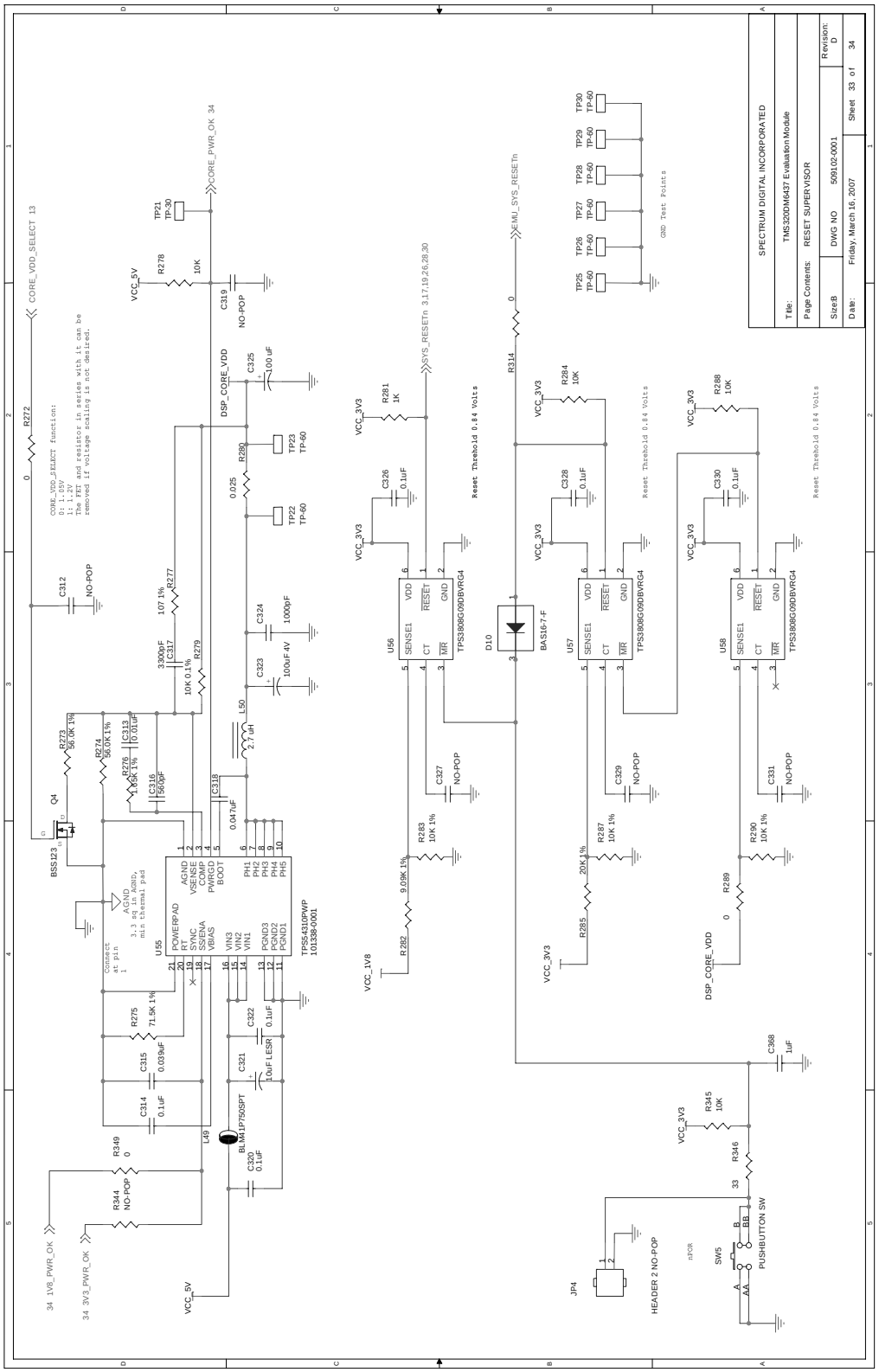

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: TVP5146
Size:B DWG NO 509102-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 28 of 34
S-VIDEO IN
VIDEO IN
U50
TVP5146M2

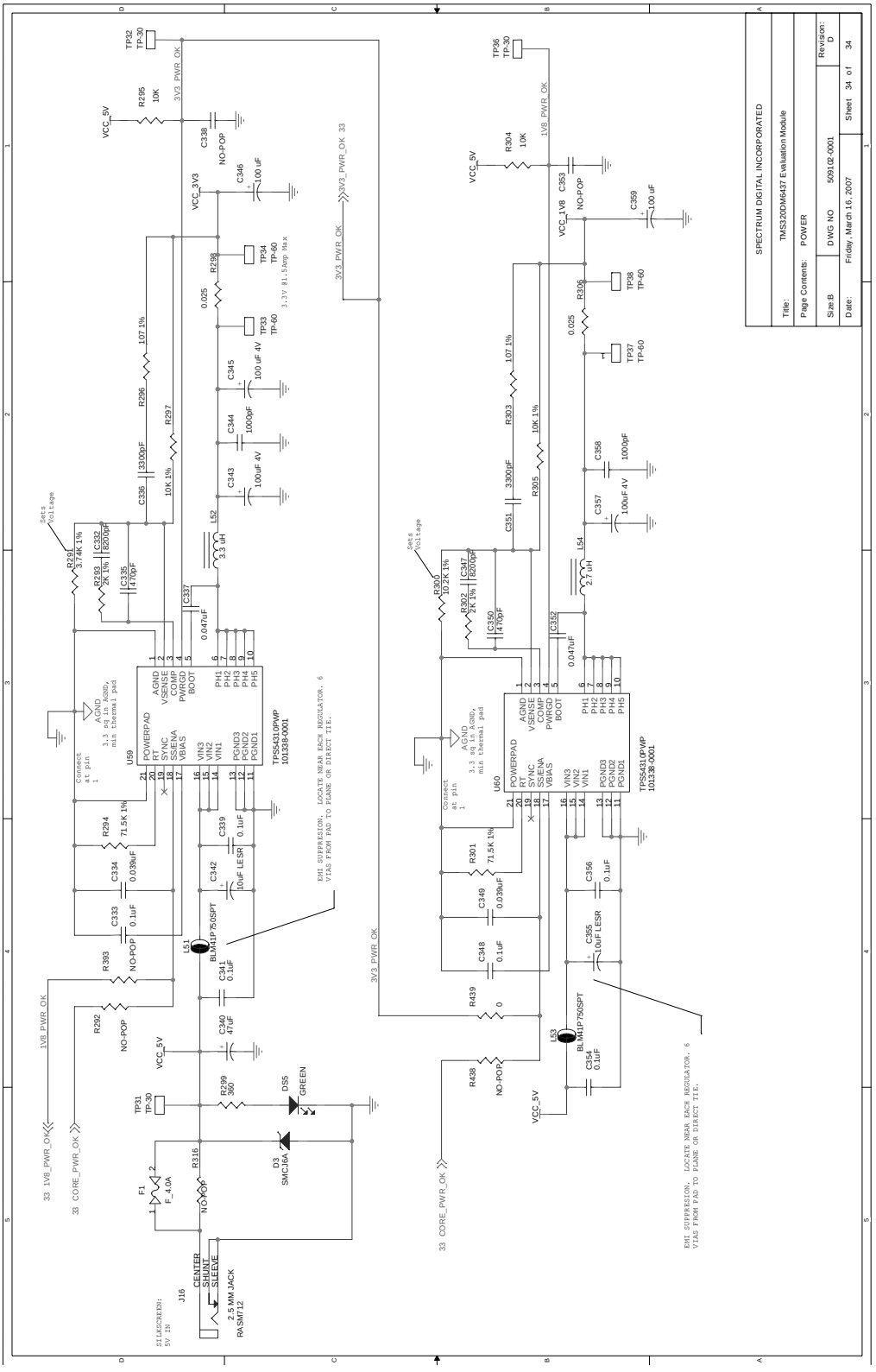

DAC A OUTPUT
DAC B OUTPUT
DAC C OUTPUT
DAC D OUTPUT
J1 NO-POP
J2 RCA JACK
J3 RCA JACK
J4 RCA JACK
S-VIDEO OUT
P1
TMS320DM6437 Evaluation Module
SPECTRUM DIGITAL INCORPORATED
U103
U104
U105
U106
OPA361AIDCKT
ENABLE
IN+
RSET
V+
OUT
GND
DAC_3V3
GND_DAC
VCC_3V3
3V3A_VOUT
BLM41P750SPT
NO-POP
DAC_IOUT_A
DAC_IOUT_B
DAC_IOUT_C
DAC_IOUT_D
DAC_RBIAS


SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: VIDEO DC Conn.
Size:B
DWG NO 5089102-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 30 of 34
DC_P1
CONNECTOR 50 X 2
R265
NO-POP
VCC_1V8
VCC_3V3
VCC_5V


SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: EMAC/MCBSP DC Conn.
Size:B DWG NO 509102-0001 Revision: D
Date: Friday, March 16, 2007 Sheet 31 of 34
CONNECTOR 45 X 2
DC_P2
VCC_3V3
VCC_5V
NO POP
R270


SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: VLYNQ/EMIF DC Conn.
Size:B
DWG NO 509102-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 32 of 34
DC_P3
HEADER 10X2
VCC_3V3
VCC_5V
VCC_1V8
R267 NO-POP
R266 1K
C177 0.1uF
U15 SN74LVC1G06DBVRG4
VLYNQ_CLOCK 22,25
VLYNQ_TXD0 22,25
VLYNQ_TXD1 23,25
VLYNQ_TXD2 23,25
VLYNQ_TXD3 23,25
VLYNQ_SCRUN
VLYNQ_RXD0
VLYNQ_RXD1
VLYNQ_RXD2
VLYNQ_RXD3
VLYNQ_RESET 12,25

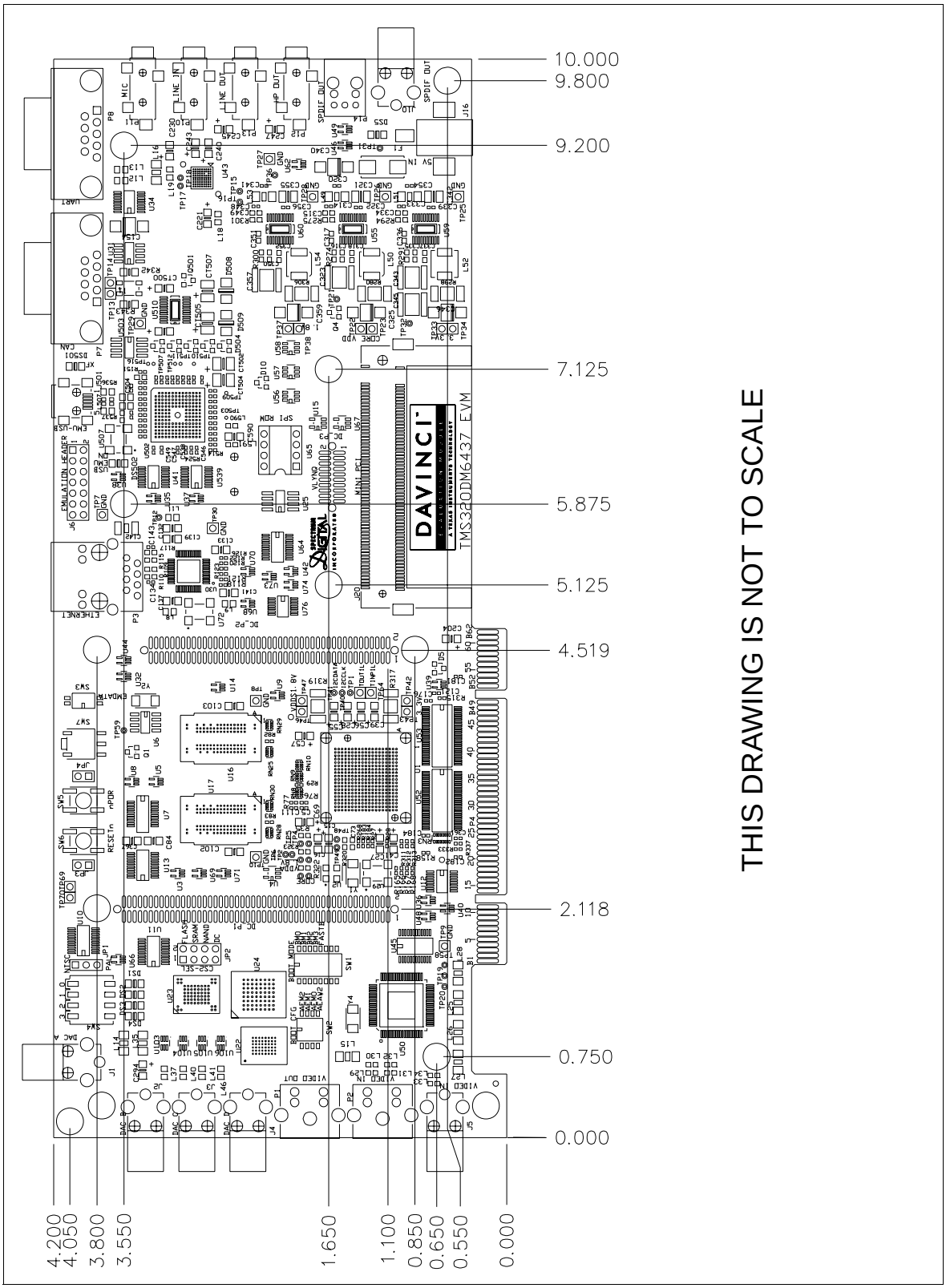

CORE_VDD_SELECT 13
CORE_PWR_OK 34
DSP_CORE_VDD
VCC_5V
VCC_3V3
VCC_1V8
EMU_SYS_RESETn
SYS_RESETn 3,17,19,26,28,30
34 1V8_PWR_OK
34 3V3_PWR_OK
SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: RESET SUPERVISOR
Size:B DWG NO 509102-0001 Revision: D
Date: Friday, March 16, 2007 Sheet 33 of 34


SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM6437 Evaluation Module
Page Contents: POWER
Size:B
DWG NO 5091 02-0001
Revision: D
Date: Friday, March 16, 2007
Sheet 34 of 34
TPS54310PWP
101338-0001
BLM41P750SPT
SMCJ36A
J16
2.5 MM JACK
RASM712
EMI SUPPRESION: LOCATE NEAR EACH REGULATOR. 6 VIAS FROM PAD TO PLANE OR DIRECT TIE.

Appendix B

Mechanical Information

This appendix contains the mechanical information about the DM6437 EVM produced by Spectrum Digital.


10.000
9.800
9.200
7.125
5.875
5.125
4.519
2.118
0.750
0.000
4.200
4.050
3.800
3.550
1.650
1.100
0.850
0.650
0.550
0.000
DAVINCI
TMS320DM6437 EVM
THIS DRAWING IS NOT TO SCALE

[redacted]

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509105-0001 Rev D